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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	37
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 14x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-TQFP
Supplier Device Package	48-TQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21g18b-aut

15. DSU - Device Service Unit

15.1. Overview

The Device Service Unit (DSU) provides a means to detect debugger probes. This enables the ARM Debug Access Port (DAP) to have control over multiplexed debug pads and CPU reset. The DSU also provides system-level services to debug adapters in an ARM debug system. It implements a CoreSight Debug ROM that provides device identification as well as identification of other debug components within the system. Hence, it complies with the ARM Peripheral Identification specification. The DSU also provides system services to applications that need memory testing, as required for IEC60730 Class B compliance, for example. The DSU can be accessed simultaneously by a debugger and the CPU, as it is connected on the High-Speed Bus Matrix. For security reasons, some of the DSU features will be limited or unavailable when the device is protected by the NVMCTRL security bit.

Related Links

NVMCTRL – Non-Volatile Memory Controller on page 489

Security Bit on page 497

15.2. Features

- CPU reset extension
- Debugger probe detection (Cold- and Hot-Plugging)
- Chip-Erase command and status
- 32-bit cyclic redundancy check (CRC32) of any memory accessible through the bus matrix
- ARM® CoreSight™ compliant device identification
- Two debug communications channels
- Debug access port security filter
- Onboard memory built-in self-test (MBIST)

21.8.6. External Multipurpose Crystal Oscillator (XOSC) Control

Name: XOSCCTRL
Offset: 0x10
Reset: 0x0080
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	STARTUP[3:0]				AMPGC	GAIN[2:0]		
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY				XTALEN	ENABLE	
Access	R/W	R/W				R/W	R/W	
Reset	1	0				0	0	

Bits 15:12 – STARTUP[3:0]: Start-Up Time
These bits select start-up time for the oscillator.

The OSCULP32K oscillator is used to clock the start-up counter.

Table 21-5. Start-Up Time for External Multipurpose Crystal Oscillator

STARTUP[3:0]	Number of OSCULP32K Clock Cycles	Number of XOSC Clock Cycles	Approximate Equivalent Time [µs]
0x0	1	3	31
0x1	2	3	61
0x2	4	3	122
0x3	8	3	244
0x4	16	3	488
0x5	32	3	977
0x6	64	3	1953
0x7	128	3	3906
0x8	256	3	7813
0x9	512	3	15625
0xA	1024	3	31250
0xB	2048	3	62500µs
0xC	4096	3	125000
0xD	8192	3	250000
0xE	16384	3	500000
0xF	32768	3	1000000

25.12.5. Interrupt Flag Status and Clear in Clock/Calendar mode (CTRLA.MODE=2)

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Clear (INTENCLR) register.

Name: INTFLAG
Offset: 0x0C
Reset: 0x0000
Property: -

Bit	15	14	13	12	11	10	9	8
	OVF							ALARM0
Access	R/W							R/W
Reset	0							0

Bit	7	6	5	4	3	2	1	0
	PER7	PER6	PER5	PER4	PER3	PER2	PER1	PER0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 15 – OVF: Overflow
This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after an overflow condition occurs, and an interrupt request will be generated if INTENCLR/SET.OVF is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Overflow interrupt flag.

Bit 8 – ALARM0: Alarm 0
This flag is cleared by writing a '1' to the flag.

This flag is set on the next CLK_RTC_CNT cycle after a match with the compare condition, and an interrupt request will be generated if INTENCLR/SET.ALARM0 is one.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Alarm 0 interrupt flag.

Bits 7:0 – PERn: Periodic Interval n [n = 7..0]
This flag is cleared by writing a '1' to the flag.

This flag is set on the 0-to-1 transition of prescaler bit [n+2], and an interrupt request will be generated if INTENCLR/SET.PERx is '1'.

Writing a '0' to this bit has no effect.

Writing a '1' to this bit clears the Periodic Interval n interrupt flag.

Value	Name	Description
0x3		Reserved

28.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection

Bit	15	14	13	12	11	10	9	8
	CMDEX[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
		CMD[6:0]						
Access		R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset		0	0	0	0	0	0	0

Bits 15:8 – CMDEX[7:0]: Command Execution
When this bit group is written to the key value 0xA5, the command written to CMD will be executed. If a value different from the key value is tried, the write will not be performed and the Programming Error bit in the Status register (STATUS.PROGE) will be set. PROGE is also set if a previously written command is not completed yet.

The key value must be written at the same time as CMD. If a command is issued through the APB bus on the same cycle as an AHB bus access, the AHB bus access will be given priority. The command will then be executed when the NVM block and the AHB bus are idle.

INTFLAG.READY must be '1' when the command is issued.

Bit 0 of the CMDEX bit group will read back as '1' until the command is issued.

Note: The NVM Address bit field in the Address register (ADDR.ADDR) uses 16-bit addressing.

Bits 6:0 – CMD[6:0]: Command
These bits define the command to be executed when the CMDEX key is written.

CMD[6:0]	Group Configuration	Description
0x00-0x01	-	Reserved
0x02	ER	Erase Row - Erases the row addressed by the ADDR register in the NVM main array.
0x03	-	Reserved
0x04	WP	Write Page - Writes the contents of the page buffer to the page addressed by the ADDR register.
0x05	EAR	Erase Auxiliary Row - Erases the auxiliary row addressed by the ADDR register. This command can be given only when the security bit is not set and only to the User Configuration Row.

29.8.7. Data Output Value Set

This register allows the user to set one or more output I/O pin drive levels high, without doing a read-modify-write operation. Changes in this register will also be reflected in the Data Output Value (OUT), Data Output Value Toggle (OUTTGL) and Data Output Value Clear (OUTCLR) registers.

Name: OUTSET
Offset: 0x18
Reset: 0x00000000
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
	OUTSET[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	OUTSET[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	OUTSET[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	OUTSET[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – OUTSET[31:0]: PORT Data Output Value Set
Writing '0' to a bit has no effect.

Writing '1' to a bit will set the corresponding bit in the OUT register, which sets the output drive level high for I/O pins configured as outputs via the Data Direction register (DIR). For pins configured as inputs via Data Direction register (DIR) with pull enabled via the Pull Enable register (PULLEN), these bits will set the input pull direction to an internal pull-up.

Value	Description
0	The corresponding I/O pin in the group will keep its configuration.
1	The corresponding I/O pin output is driven high, or the input is connected to an internal pull-up.

Value	Description
0	The peripheral is disabled or being disabled.
1	The peripheral is enabled.

Bit 0 – SWRST: Software Reset
Writing '0' to this bit has no effect.

Writing '1' to this bit resets all registers in the SERCOM, except DBGCTRL, to their initial state, and the SERCOM will be disabled.

Writing '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded. Any register write access during the ongoing reset will result in an APB error. Reading any register will return the reset value of the register.

Due to synchronization there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

This bit is not enable-protected.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

36.8.14. Counter Value

Note: Prior to any read access, this register must be synchronized by user by writing the according TCC Command value to the Control B Set register (CTRLBSET.CMD=READSYNC).

Name: COUNT
Offset: 0x34
Reset: 0x00000000
Property: PAC Write-Protection, Write-Synchronized, Read-Synchronized

Bit	31	30	29	28	27	26	25	24
	COUNT[31:24]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	23	22	21	20	19	18	17	16
	COUNT[23:16]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	15	14	13	12	11	10	9	8
	COUNT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	COUNT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 31:0 – COUNT[31:0]: Counter Value
These bits hold the value of the counter register.

Note: When the TCC is configured as 24- or 16-bit timer/counter, the excess bits are read zero.

Note: This bit field occupies the MSB of the register, [31:m]. m is dependent on the Resolution bit in the Control A register (CTRLA.RESOLUTION):

CTRLA.RESOLUTION	Bits [31:m]
0x0 - NONE	31:0 (depicted)
0x1 - DITH4	31:4
0x2 - DITH5	31:5
0x3 - DITH6	31:6

38.7. Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	CFBS[2:0]			AESMODE[2:0]			ENABLE	SWRST
0x01		15:8		XORKEY	KEYGEN	LOD	STARTMODE	CIPHER	KEYSIZE[1:0]	
0x02		23:16					CTYPE[3:0]			
0x03		31:24								
0x04	CTRLB	7:0					GFMUL	EOM	NEWMSG	START
0x05	INTENCLR	7:0							GFMCMP	ENCCMP
0x06	INTENSET	7:0							GFMCMP	ENCCMP
0x07	INTFLAG	7:0							GFMCMP	ENCCMP
0x08	DATABUFPTR	7:0							INDATAPTR[1:0]	
0x09	DBGCTRL	7:0								DBGRUN
0x0A ... 0x0B	Reserved									
0C	KEYWORDx0	7:0	KEYWORD[7:0]							
0D		15:8	KEYWORD[15:8]							
0E		23:16	KEYWORD[23:16]							
0F		31:24	KEYWORD[31:24]							
10	KEYWORDx1	7:0	KEYWORD[7:0]							
11		15:8	KEYWORD[15:8]							
12		23:16	KEYWORD[23:16]							
13		31:24	KEYWORD[31:24]							
14	KEYWORDx2	7:0	KEYWORD[7:0]							
15		15:8	KEYWORD[15:8]							
16		23:16	KEYWORD[23:16]							
17		31:24	KEYWORD[31:24]							
18	KEYWORDx3	7:0	KEYWORD[7:0]							
19		15:8	KEYWORD[15:8]							
1A		23:16	KEYWORD[23:16]							
1B		31:24	KEYWORD[31:24]							
1C	KEYWORDx4	7:0	KEYWORD[7:0]							
1D		15:8	KEYWORD[15:8]							
1E		23:16	KEYWORD[23:16]							
1F		31:24	KEYWORD[31:24]							
20	KEYWORDx5	7:0	KEYWORD[7:0]							
21		15:8	KEYWORD[15:8]							
22		23:16	KEYWORD[23:16]							
23		31:24	KEYWORD[31:24]							
24	KEYWORDx6	7:0	KEYWORD[7:0]							
25		15:8	KEYWORD[15:8]							
26		23:16	KEYWORD[23:16]							
27		31:24	KEYWORD[31:24]							

38.8.6. Data Buffer Pointer

Name: DATABUFPTR
Offset: 0x08
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
							INDATAPTR[1:0]	
Access							R/W	R/W
Reset							0	0

Bits 1:0 – INDATAPTR[1:0]: Input Data Pointer
Writing to this field changes the value of the input data pointer, which determines which of the four data registers is written to/read from when the next write/read to the DATA register address is performed.

Each OPAMP x can be configured to behave differently in different sleep modes. The behavior is determined by the individual Run in Standby and On Demand bits in the OPAMP Control x registers (OPAMPCTRLx.RUNSTDBY, and OPAMPCTRLx.ONDEMAND), as well as the common Enable bit in the Control A register (CTRLA.ENABLE).

Table 41-1. Individual OPAMP Sleep Mode Operation

OPAMPCTRLx.RUNSTDBY	OPAMPCTRLx.ONDEMAND	CTRLA.ENABLE	Sleep Behavior
-	-	0	Disabled
0	0	1	Always run in all sleep modes except STANDBY sleep mode
0	1	1	Only run in all sleep modes except STANDBY sleep mode if requested by a peripheral.
1	0	1	Always run in all sleep mode
1	1	1	Only run in all sleep modes if requested by a peripheral.

Note:
When OPAMPCTRLx.ONDEMAND=1, the analog block is powered off for the lowest power consumption if it is not requested.

When requested, a start-up time delay is necessary when the system returns from sleep. The start-up time is depending on the Bias Selection bits in the OPAMP Control x register (OPAMPCTRLx.BIAS) and the corresponding speed/current consumption requirements.

41.6.7. Synchronization

Not applicable.

41.6.8. Configuring the Operational Amplifiers

Each individual operational amplifier is configured by its respective Operational Amplifier Control x register (OPAMPCTRLx). These settings must be configured before the amplifier is started.

- Select the positive input in OPAMPCTRLx.MUXPOS.
- Select the negative input in OPAMPCTRLx.MUXNEG.
- Select RES1EN if resistor ladder is used.
- Select the input for the resistor ladder in OPAMPCTRLx.RES1MUX.
- Select the potentiometer selection of the resistor ladder in OPAMPCTRLx.POTMUX.
- Select the VCC input for the resistor ladder in OPAMPCTRLx.RES2VCC.
- Connect the operational amplifier output to the resistor ladder using OPAMPCTRLx.RES2OUT.
- Select the trade-off between speed and energy consumption in OPAMPCTRLx.BIAS.

41.8.2. Status

Name: STATUS
Offset: 0x02
Reset: 0x00
Property: –

Bit	7	6	5	4	3	2	1	0
						READY2	READY1	READY0
Access						R	R	R
Reset						0	0	0

Bits 2,1,0 – READYx: OPAMP x Ready

This bit is set when the OPAMPx output is ready.

This bit is cleared when the output of OPAMPx is not ready.

42.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
	ONDEMAND	RUNSTDBY					ENABLE	SWRST
Access	R/W	R/W					R/W	R/W
Reset	0	0					0	0

Bit 7 – ONDEMAND: On Demand Control
The On Demand operation mode allows the ADC to be enabled or disabled, depending on other peripheral requests.

In On Demand operation mode, i.e., if the ONDEMAND bit has been previously set, the ADC will only be running when requested by a peripheral. If there is no peripheral requesting the ADC will be in a disable state.

If On Demand is disabled the ADC will always be running when enabled.

In standby sleep mode, the On Demand operation is still active if the CTRLA.RUNSTDBY bit is '1'. If CTRLA.RUNSTDBY is '0', the ADC is disabled.

This bit is not synchronized.

Value	Description
0	The ADC is always on , if enabled.
1	The ADC is enabled, when a peripheral is requesting the ADC conversion. The ADC is disabled if no peripheral is requesting it.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the ADC behaves during standby sleep mode.

This bit is not synchronized.

Value	Description
0	The ADC is halted during standby sleep mode.
1	The ADC is not stopped in standby sleep mode. If CTRLA.ONDEMAND=1, the ADC will be running when a peripheral is requesting it. If CTRLA.ONDEMAND=0, the ADC will always be running in standby sleep mode.

Bit 1 – ENABLE: Enable
Due to synchronization there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the ENABLE bit in the SYNCBUSY register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

43.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection, Write-Synchronized

Bit	7	6	5	4	3	2	1	0
							ENABLE	SWRST
Access							R/W	W
Reset							0	0

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from updating the register until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the corresponding bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE is cleared when the peripheral is enabled/disabled.

Value	Description
0	The AC is disabled.
1	The AC is enabled. Each comparator must also be enabled individually by the Enable bit in the Comparator Control register (COMPCTRLn.ENABLE).

Bit 0 – SWRST: Software Reset
Writing a '0' to this bit has no effect.

Writing a '1' to this bit resets all registers in the AC to their initial state, and the AC will be disabled.

Writing a '1' to CTRLA.SWRST will always take precedence, meaning that all other writes in the same write-operation will be discarded.

Due to synchronization, there is a delay from writing CTRLA.SWRST until the reset is complete. CTRLA.SWRST and SYNCBUSY.SWRST will both be cleared when the reset is complete.

Value	Description
0	There is no reset operation ongoing.
1	The reset operation is ongoing.

44.7. Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0							ENABLE	SWRST
0x01	CTRLB	7:0						REFSEL[1:0]		DIFF
0x02	EVCTRL	7:0			INVEI1	INVEI0	EMPTYEO1	EMPTYEO0	STARTEI1	STARTEI0
0x03	Reserved									
0x04	INTENCLR	7:0					EMPTY1	EMPTY0	UNDERRUN1	UNDERRUN0
0x05	INTENSET	7:0					EMPTY1	EMPTY0	UNDERRUN1	UNDERRUN0
0x06	INTFLAG	7:0					EMPTY1	EMPTY0	UNDERRUN1	UNDERRUN0
0x07	STATUS	7:0					EOC1	EOC0	READY1	READY0
0x08	SYNCBUSY	7:0			DATABUF1	DATABUF0	DATA1	DATA0	ENABLE	SWRST
0x09		15:8								
0x0A		23:16								
0x0B		31:24								
0x0C	DACCTRL0	7:0	DITHER	RUNSTDBY			CCTRL[1:0]		ENABLE	LEFTADJ
0x0D		15:8					REFRESH[3:0]			
0x0E	DACCTRL1	7:0	DITHER	RUNSTDBY			CCTRL[1:0]		ENABLE	LEFTADJ
0x0F		15:8					REFRESH[3:0]			
0x10	DATA0	7:0	DATA[7:0]							
0x11		15:8	DATA[15:8]							
0x12	DATA1	7:0	DATA[7:0]							
0x13		15:8	DATA[15:8]							
0x14	DATABUF0	7:0	DATABUF[7:0]							
0x15		15:8	DATABUF[15:8]							
0x16	DATABUF1	7:0	DATABUF[7:0]							
0x17		15:8	DATABUF[15:8]							
0x18	DBGCTRL	7:0								DBGRUN

44.8. Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16- and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers are optionally write-protected by the Peripheral Access Controller (PAC). Optional PAC write-protection is denoted by the "PAC Write-Protection" property in each individual register description. For details, refer to Register Access Protection.

Some registers are synchronized when read and/or written. Synchronization is denoted by the "Write-Synchronized" or the "Read-Synchronized" property in each individual register description. For details, refer to Synchronization.

Some registers are enable-protected, meaning they can only be written when the peripheral is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

46.5. Maximum Clock Frequencies

Table 46-5. Maximum GCLK Generator Output Frequencies(1)

Symbol	Description	Conditions	Fmax		Units
			PL0	PL2	
$F_{gclkgen}[0:2]$	GCLK Generator output Frequency	-	24	96	MHz
$F_{gclkgen}[3:8]$		undivided	24	96	MHz
$F_{gclkgen}[3:8]$		divided	16	66	MHz

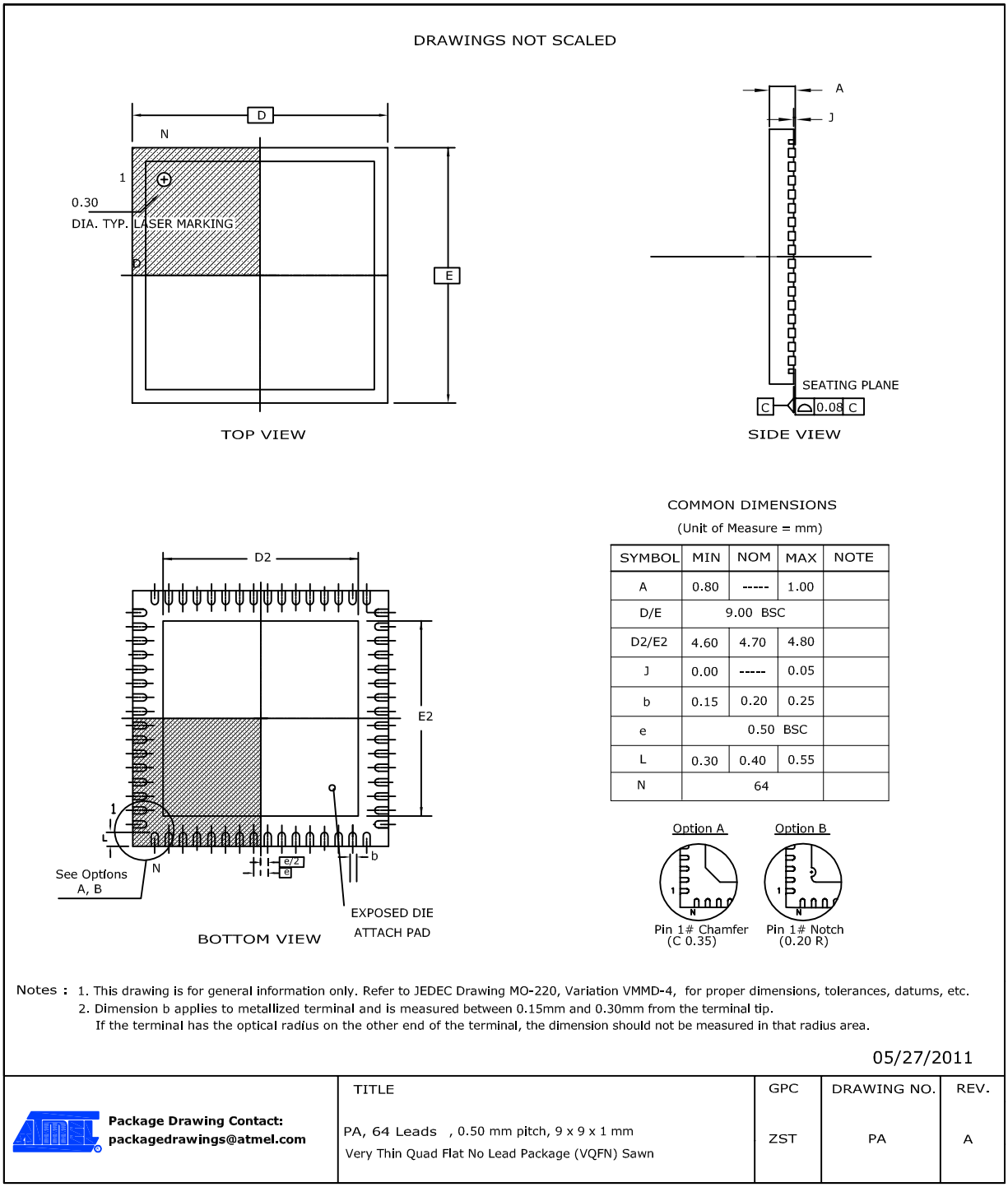
Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

Table 46-6. Maximum Peripheral Clock Frequencies(1)

Symbol	Description	Conditions	Max.		Units
			PL0	PL2	
f_{CPU}	CPU clock frequency	-	12	48	MHz
f_{AHB}	AHB clock frequency	-	12	48	MHz
f_{APBA}	APBA clock frequency	Bus clock domain = BACKUP	6	6	MHz
f_{APBA}	APBA clock frequency	Bus clock domain = Low Power	12	48	MHz
f_{APBB}	APBB clock frequency	-	12	48	MHz
f_{APBC}	APBC clock frequency	-			
f_{APBD}	APBD clock frequency	-			
f_{APBE}	APBE clock frequency	-			
$f_{GCLK\_DFLL48M\_REF}$	DFLL48M Reference clock frequency	-	NA	33	kHz
f_{GCLK_DPLL}	FDPLL96M Reference clock frequency	-	2	2	MHz
$f_{GCLK\_DPLL\_32K}$	FDPLL96M 32k Reference clock frequency	-	32	100	kHz
f_{GCLK_EIC}	EIC input clock frequency	-	12	48	MHz
f_{GCLK_USB}	USB input clock frequency	-	NA	60	MHz

48.2.3. 64 pin QFN



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	-----	1.00	
D/E		9.00 BSC		
D2/E2	4.60	4.70	4.80	
J	0.00	-----	0.05	
b	0.15	0.20	0.25	
e		0.50 BSC		
L	0.30	0.40	0.55	
N		64		

Notes : 1. This drawing is for general information only. Refer to JEDEC Drawing MO-220, Variation VMMD-4, for proper dimensions, tolerances, datums, etc.
2. Dimension b applies to metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
If the terminal has the optical radius on the other end of the terminal, the dimension should not be measured in that radius area.

05/27/2011

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	PA, 64 Leads , 0.50 mm pitch, 9 x 9 x 1 mm Very Thin Quad Flat No Lead Package (VQFN) Sawn	ZST	PA	A

Note: The exposed die attach pad is not connected electrically inside the device.

Table 48-8. Device and Package Maximum Weight

200	mg

Table 48-9. Package Charateristics

Moisture Sensitivity Level	MSL3

48.2.6. 32 pin TQFP

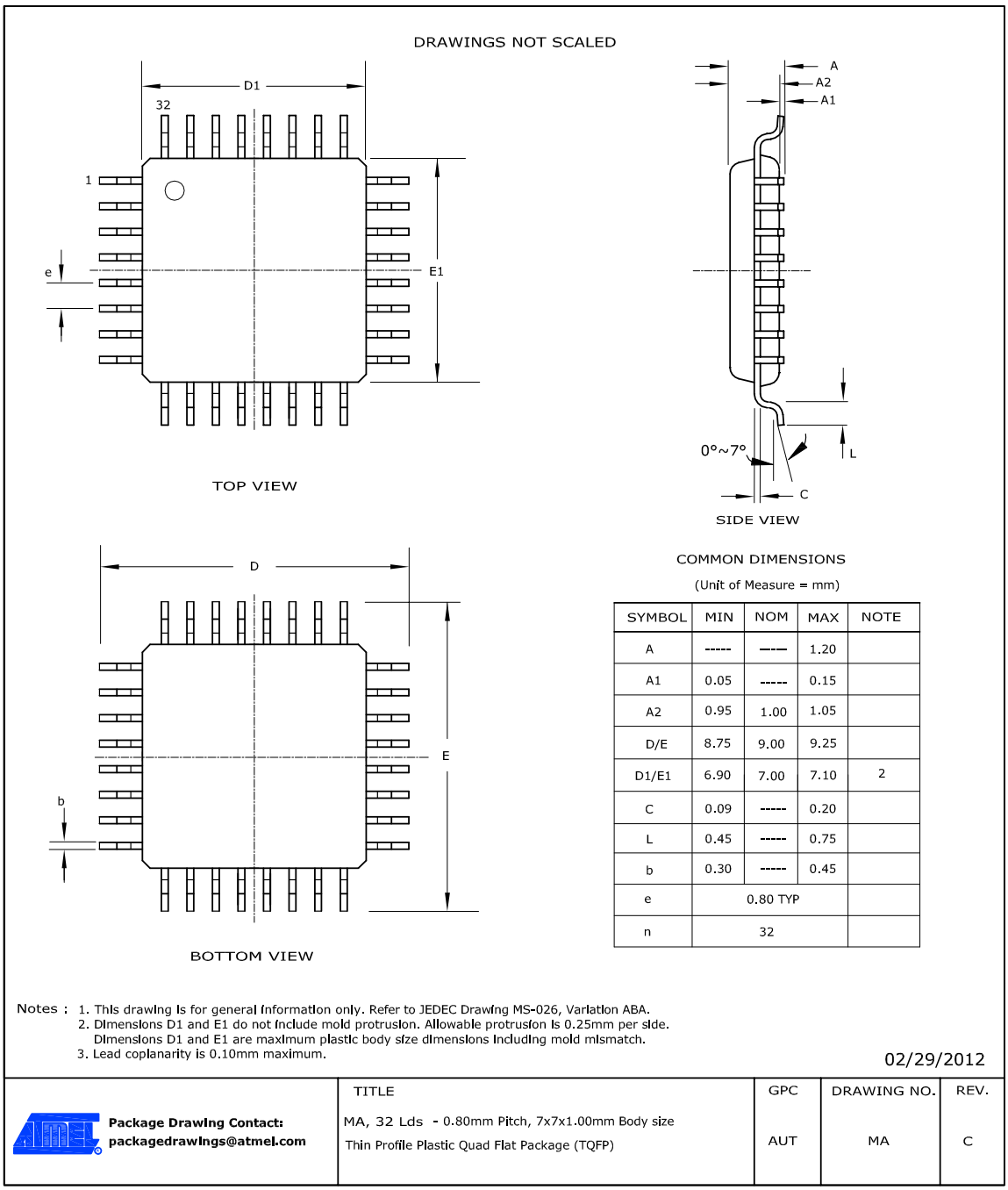


Table 48-17. Device and Package Maximum Weight

100	mg

Table 48-18. Package Charateristics

Moisture Sensitivity Level	MSL3

50.1.8. TRNG

1 – When TRNG is enabled with configuration CTRL.RUNSTDBY = 0, (disabled during sleep) it could still continue to operate resulting in over-consumption (~50uA) in standby mode.
Errata reference: 14827
Fix/Workaround:
Disable the TRNG before entering standby mode.

50.1.9. RSTC

1 – When a System Reset Request is applied, the OSC16MCTRL register is not reset.
Errata reference: 13416
Fix/Workaround:
None.

50.1.10. Device

1 – The H2LBRIDGE and H2LBRIDGE latency is high.
For a write the latency is 5-cycles (cycles needed for a transaction to propagate from the bridge slave endpoint to the master endpoint). As the bridge supports posted-write, no stall cycles is seen as long as the FIFO is not full.
For a read the latency is 4-cycles for the address phase and again 4-cycles for the data to propagate back leading to a total of 8-cycle stall when there is no LP clock division and the accessed slave does not stall.
Errata reference: 13414
Fix/Workaround:
None

2 – In Standby mode, when Power Domain 1 is power gated, devices can show higher consumption than expected.
Errata reference: 13599
Fix/Workaround:
Force the Power Domain 1 to remain active by setting PM.PDCFG to 0x2

3 – In IDLE sleep mode, the APB and AHB clocks are not stopped if the FDPLL is running as a GCLK clock source.
Errata reference: 13401
Fix/Workaround:
Disable the FDPLL before entering IDLE sleep mode.

4 – The low latency mode cannot be enabled by writing a one to address 0x41008120. This bit has no effect.
Errata reference: 13506
Fix/Workaround:
None

5 – XOSC32K contains load capacitor equivalent to Cload=7pf. External load capacitors must take this into account.
Errata reference: 13425
Fix/Workaround:
None

Electrical Characteristics (Oscillator sections)	• Crystal Oscillator (XOSC) Characteristics – Digital Clock Characteristics added – Values updated and added – Power Consumption added • External 32KHz Crystal Oscillator (XOSC32K) Characteristics – Digital Clock Characteristics added – Conditions updated, values added – Power Consumption added • 32.768kHz Internal Oscillator (OSC32K) Characteristics – Values updated and added – Power Consumption added • Internal Ultra Low Power 32KHz RC Oscillator (OSCULP32K) Characteristics – Title changed – Values updated and added – $T_{STARTUP}$ removed – Power Consumption added • Digital Frequency Locked Loop (DFLL48M) Characteristics – Values added – Power Consumption added • 16MHz RC Oscillator (OSC16M) Characteristics – Values and conditions added – Power Consumption added • Digital Phase Lock Loop (DPLL) Characteristics – Values for jitter, lock time updated and added – Power Consumption added
Errata	Added Errata: • **EVSYS**: CHSTATUS.CHBUSYn may be cleared too early under certain conditions. *Errata reference 14835* • **DAC**: Unexpected value of SYNCBUSY.ENABLE under certain conditions. *Errata reference 14885* • **DAC**: Unexpected value of SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1 under certain conditions. *Errata reference 14910*