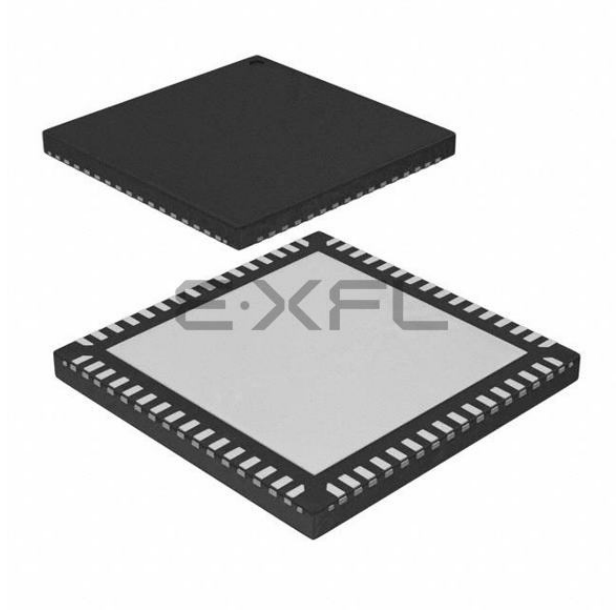

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21j16b-mut

9.4.1. Power-On Reset on VDDIN

VDDIN is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VDDIN goes below the threshold voltage, the entire chip is reset.

9.4.2. Power-On Reset on VSWOUT

VSWOUT is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VSWOUT goes below the threshold voltage, the entire chip is reset.

9.4.3. Power-On Reset on VDDIO

VDDIO is monitored by POR. Monitoring is always activated, including startup and all sleep modes. If VDDIO goes below the threshold voltage, all I/Os supplied by VSWOUT are reset.

9.4.4. Brown-Out Detector on VSWOUT/VBAT

BOD33 monitors VSWOUT or VBAT depending on configuration.

Related Links

SUPC – Supply Controller on page 292
Battery Backup Power Switch on page 297

9.4.5. Brown-Out Detector on VDDCORE

Once the device has started up, BOD12 monitors the internal VDDCORE.

Related Links

SUPC – Supply Controller on page 292
Battery Backup Power Switch on page 297

9.5. Performance Level Overview

By default, the device will start in Performance Level 0. This PL0 is aiming for the lowest power consumption by limiting logic speeds and the CPU frequency. As a consequence, all GCLK will have limited capabilities, and some peripherals and clock sources will not work or with limited capabilities:

List of peripherals/clock sources not available in PL0:

- USB (limited by logic frequency)
- DFLL48M

List of peripherals/clock sources with limited capabilities in PL0:

- All AHB/APB peripherals are limited by CPU frequency
- DPLL96M: may be able to generate 48MHz internally, but the output cannot be used by logic
- GCLK: the maximum frequency is by factor 4 compared to PL2
- SW interface: the maximum frequency is by factor 4 compared to PL2
- TC: the maximum frequency is by factor 4 compared to PL2
- TCC:the maximum frequency is by factor 4 compared to PL2
- SERCOM: the maximum frequency is by factor 4 compared to PL2

List of peripherals/clock sources with full capabilities in PL0:

- AC
- ADC
- DAC
- EIC

11.5. NVM Temperature Log Row

The NVM Temperature Log Row contains calibration data that are determined and written during production test. These calibration values are required for calculating the temperature from measuring the temperature sensor in the Supply Controller (SUPC) by the ADC.

The NVM Temperature Log Row can be read at address 0x00806030.

The NVM Temperature Log Row can not be written.

Table 11-6. Temperature Log Row Content

Bit Position	Name	Description
7:0	ROOM_TEMP_VAL_INT	Integer part of room temperature in °C
11:8	ROOM_TEMP_VAL_DEC	Decimal part of room temperature
19:12	HOT_TEMP_VAL_INT	Integer part of hot temperature in °C
23:20	HOT_TEMP_VAL_DEC	Decimal part of hot temperature
31:24	ROOM_INT1V_VAL	2's complement of the internal 1V reference drift at room temperature (versus a 1.0 centered value)
39:32	HOT_INT1V_VAL	2's complement of the internal 1V reference drift at hot temperature (versus a 1.0 centered value)
51:40	ROOM_ADC_VAL	Temperature sensor 12bit ADC conversion at room temperature
63:52	HOT_ADC_VAL	Temperature sensor 12bit ADC conversion at hot temperature

Related Links

Device Temperature Measurement on page 1042
Temperature Sensor Characteristics on page 1170

11.6. Serial Number

Each device has a unique 128-bit serial number which is a concatenation of four 32-bit words contained at the following addresses:

Word 0: 0x0080A00C

Word 1: 0x0080A040

Word 2: 0x0080A044

Word 3: 0x0080A048

The uniqueness of the serial number is guaranteed only when using all 128 bits.

17.5.2. Power Management

The GCLK can operate in all sleep modes, if required.

Related Links

PM – Power Manager on page 192

17.5.3. Clocks

The GCLK bus clock (CLK_GCLK_APB) can be enabled and disabled in the Main Clock Controller.

Related Links

Peripheral Clock Masking on page 157

OSC32KCTRL – 32KHz Oscillators Controller on page 273

17.5.4. DMA

Not applicable.

17.5.5. Interrupts

Not applicable.

17.5.6. Events

Not applicable.

17.5.7. Debug Operation

When the CPU is halted in debug mode the GCLK continues normal operation. If the GCLK is configured in a way that requires it to be periodically serviced by the CPU through interrupts or similar, improper operation or data loss may result during debugging.

17.5.8. Register Access Protection

All registers with write-access can be optionally write-protected by the Peripheral Access Controller (PAC).

Note: Optional write-protection is indicated by the "PAC Write-Protection" property in the register description.

When the CPU is halted in debug mode, all write-protection is automatically disabled. Write-protection does not apply for accesses through an external debugger.

Related Links

PAC - Peripheral Access Controller on page 59

17.5.9. Analog Connections

Not applicable.

17.6. Functional Description

17.6.1. Principle of Operation

The GCLK module is comprised of nine Generic Clock Generators (Generators) sourcing up to 64 Peripheral Channels and the Main Clock signal GCLK_MAIN.

A clock source selected as input to a Generator can either be used directly, or it can be prescaled in the Generator. A generator output is used by one or more Peripheral Channels to provide a peripheral generic clock signal (GCLK_PERIPH) to the peripherals.

Value	Description
0	The APBD clock for the AC is stopped.
1	The APBD clock for the AC is enabled.

Bit 3 – ADC: ADC APBD Clock Enable

Value	Description
0	The APBD clock for the ADC is stopped.
1	The APBD clock for the ADC is enabled.

Bit 2 – TC4: TC4 APBD Clock Enable

Value	Description
0	The APBD clock for the TC4 is stopped.
1	The APBD clock for the TC4 is enabled.

Bit 1 – SERCOM5: SERCOM5 APBD Clock Enable

Value	Description
0	The APBD clock for the SERCOM5 is stopped.
1	The APBD clock for the SERCOM5 is enabled.

Bit 0 – EVSYS: EVSYS APBD Clock Enable

Value	Description
0	The APBD clock for the EVSYS is stopped.
1	The APBD clock for the EVSYS is enabled.

Off State The power domain is entirely powered off. The logic context is lost.

20.6.2. Principle of Operation

In active mode, all clock domains and power domains are active, allowing software execution and peripheral operation. The PM Sleep Mode Controller allows to save power by choosing between different sleep modes depending on application requirements, see Sleep Mode Controller.

The PM Performance Level Controller allows to optimize either for low power consumption or high performance.

The PM Power Domain Controller allows to reduce the power consumption in standby mode even further.

20.6.3. Basic Operation

20.6.3.1. Initialization

After a power-on reset, the PM is enabled, the device is in ACTIVE mode, the performance level is PL0 (the lowest power consumption) and all the power domains are in active state.

20.6.3.2. Enabling, Disabling and Resetting

The PM is always enabled and can not be reset.

20.6.3.3. Sleep Mode Controller

A Sleep mode is entered by executing the Wait For Interrupt instruction (WFI). The Sleep Mode bits in the Sleep Configuration register (SLEEPCFG.SLEEPMODE) select the level of the sleep mode.

Note: A small latency happens between the store instruction and actual writing of the SLEEPCFG register due to bridges. Software must ensure that the SLEEPCFG register reads the desired value before issuing a WFI instruction.

Note: After power-up, the MAINVREG low power mode takes some time to stabilize. Once stabilized, the INTFLAG.SLEEPRDY bit is set. Before entering Standby or Backup mode, software must ensure that the INTFLAG.SLEEPRDY bit is set.

Table 20-1. Sleep Mode Entry and Exit Table

Mode	Mode Entry	Wake-Up Sources
IDLE	SLEEPCFG.SLEEPMODE = IDLE	Synchronous (2) (APB, AHB), asynchronous (1)
STANDBY	SLEEPCFG.SLEEPMODE = STANDBY	Synchronous(3), Asynchronous
BACKUP	SLEEPCFG.SLEEPMODE = BACKUP	Backup reset detected by the RSTC
OFF	SLEEPCFG.SLEEPMODE = OFF	External Reset

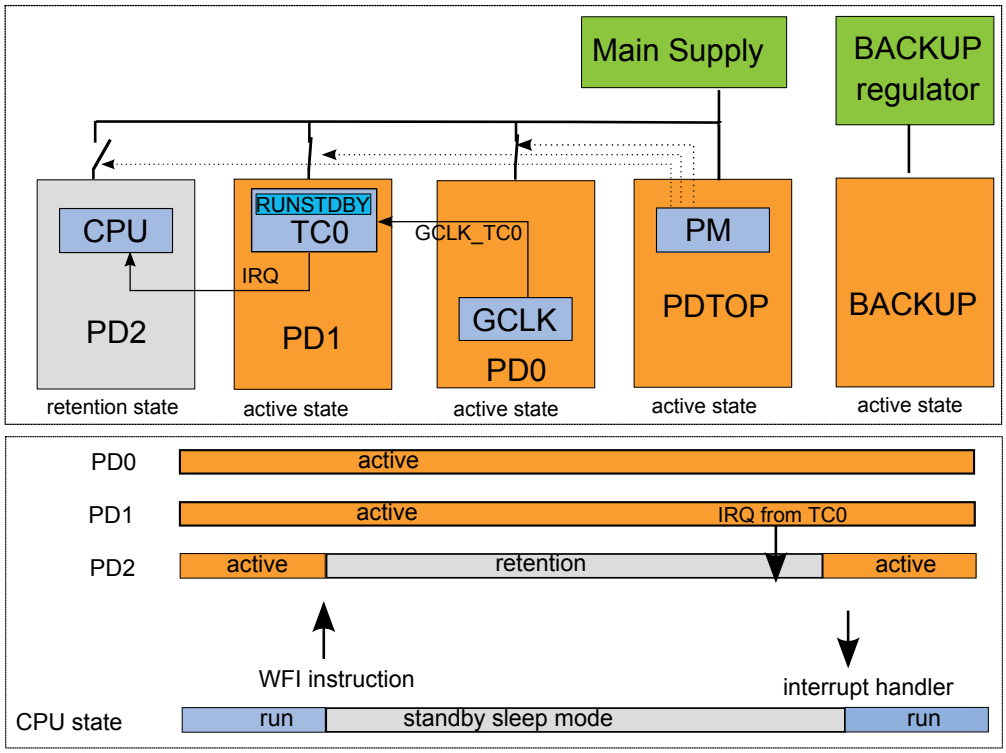
Note:

1. Asynchronous: interrupt generated on generic clock, external clock, or external event.
2. Synchronous: interrupt generated on the APB clock.
3. Synchronous interrupt only for peripherals configured to run in standby.

Note: The type of wake-up sources (synchronous or asynchronous) is given in each module interrupt section.

– In this case, the VDDCORE voltage is still supplied by the main voltage regulator, refer to Regulator Automatic Low Power Mode for details. Thus, global wake-up time is not affected by the regulator.

Figure 20-7. TC0 SleepWalking with Static PD Gating



EIC SleepWalking with Static PD Gating

In this example, EIC peripheral is used to detect an edge condition to generate interrupt to the CPU. An External interrupt pin is filtered by the CLK_ULP32K clock, GCLK peripheral is not used. Refer to Chapter EIC – External Interrupt Controller for details. The EIC peripheral is located in the power domain PDTOP (which is not switchable), and there is no RUNSTDBY bit in the EIC peripheral.

- Entering standby mode: As shown in Figure 20-8, all the switchable power domains are set in retention state by the Power Manager peripheral. The low power regulator supplies the VDDCORE voltage level.
- Exiting standby mode: When conditions are met, the EIC peripheral generates an interrupt to wake the device up. Successively, the PM peripheral sets PD0, PD1, and PD2 to active state, and the main voltage regulator restarts. Once PD2 is in active state and the main voltage regulator is ready, the CPU is able to operate normally and execute the EIC interrupt handler accordingly.
- Wake-up time:
  - The required time to set the switchable power domains to active state has to be considered for the global wake-up time, refer to Wake-Up Time for details.
  - When in standby sleep mode, the GCLK peripheral is not used, allowing the VDDCORE to be supplied by the low power regulator to reduce consumption, see Regulator Automatic Low Power Mode. Consequently, main voltage regulator wake-up time has to be considered for the global wake-up time as shown in Figure 20-8.

22.7. Register Summary

Offset	Name	Bit Pos.								
0x00	INTENCLR	7:0							OSC32KRDY	XOSC32KRDY
0x01		15:8								
0x02		23:16								
0x03		31:24								
0x04	INTENSET	7:0							OSC32KRDY	XOSC32KRDY
0x05		15:8								
0x06		23:16								
0x07		31:24								
0x08	INTFLAG	7:0							OSC32KRDY	XOSC32KRDY
0x09		15:8								
0x0A		23:16								
0x0B		31:24								
0x0C	STATUS	7:0							OSC32KRDY	XOSC32KRDY
0x0D		15:8								
0x0E		23:16								
0x0F		31:24								
0x10	RTCCTRL	7:0						RTCSEL[2:0]		
0x11		15:8								
0x12		23:16								
0x13		31:24								
0x14	XOSC32K	7:0	ONDEMAND	RUNSTDBY		EN1K	EN32K	XTALEN	ENABLE	
0x15		15:8				WRTLOCK		STARTUP[2:0]		
0x16		23:16								
0x17		31:24								
0x18	OSC32K	7:0	ONDEMAND	RUNSTDBY			EN1K	EN32K	ENABLE	
0x19		15:8				WRTLOCK		STARTUP[2:0]		
0x1A		23:16		CALIB[6:0]						
0x1B		31:24								
0x1C	OSCULP32K	7:0								
0x1D		15:8	WRTLOCK			CALIB[4:0]				

22.8. Register Description

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register and the 8-bit halves of a 16-bit register can be accessed directly.

All registers with write-access can be write-protected optionally by the peripheral access controller (PAC). Optional Write-Protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in the register description. Write-protection does not apply to accesses through an external debugger.

26.8.13. Pending Channels

Name: PENDCH
Offset: 0x2C
Reset: 0x00000000
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
	PENDCH15	PENDCH14	PENDCH13	PENDCH12	PENDCH11	PENDCH10	PENDCH9	PENDCH8
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	PENDCH7	PENDCH6	PENDCH5	PENDCH4	PENDCH3	PENDCH2	PENDCH1	PENDCH0
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – PENDCHn: Pending Channel n [n=15..0]
This bit is cleared when trigger execution defined by channel trigger action settings for DMA channel n is started, when a bus error for DMA channel n is detected or when DMA channel n is disabled. For details on trigger action settings, refer to CHCTRLB.TRIGACT.

This bit is set when a transfer is pending on DMA channel n.

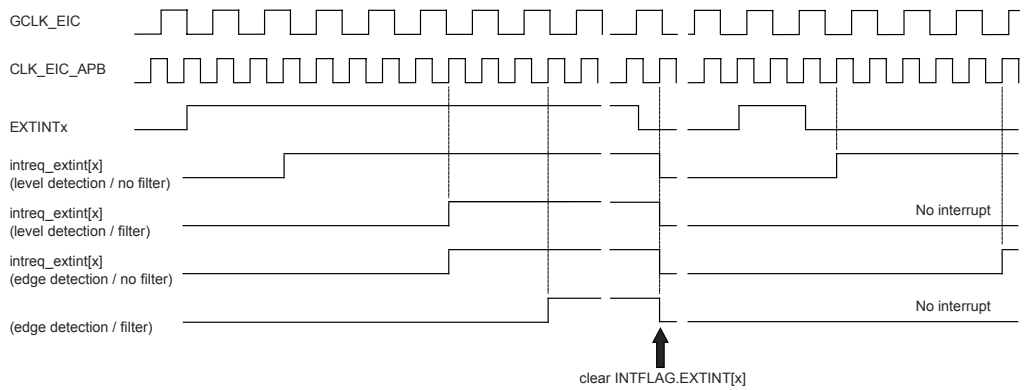
Table 27-1. Majority Vote Filter

Samples [0, 1, 2]	Filter Output
[0,0,0]	0
[0,0,1]	0
[0,1,0]	0
[0,1,1]	1
[1,0,0]	0
[1,0,1]	1
[1,1,0]	1
[1,1,1]	1

When an external interrupt is configured for level detection and when filtering is disabled, detection is done asynchronously. Asynchronuous detection does not require GCLK_EIC or CLK_ULP32K, but interrupt and events can still be generated.

If filtering or edge detection is enabled, the EIC automatically requests GCLK_EIC or CLK_ULP32K to operate. The selection between these two clocks is done by writing the Clock Selection bits in the Control A register (CTRLA.CKSEL). GCLK_EIC must be enabled in the GCLK module.

Figure 27-2. Interrupt Detections



The detection delay depends on the detection mode.

Table 27-2. Interrupt Latency

Detection mode	Latency (worst case)
Level without filter	Five CLK_EIC_APB periods
Level with filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods
Edge without filter	Four GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods
Edge with filter	Six GCLK_EIC/CLK_ULP32K periods + five CLK_EIC_APB periods

Related Links

GCLK - Generic Clock Controller on page 133

USERm	User Multiplexer	Description	Path Type
m = 42	Reserved	-	-
m = 43	MTB START	Tracing start	Asynchronous, synchronous, and resynchronized paths
m = 44	MTB STOP	Tracing stop	Asynchronous, synchronous, and resynchronized paths
others	Reserved	-	-

4. Set the Collision Detected bit (STATUS.COLL) along with the Error interrupt flag (INTFLAG.ERROR).
5. Set the Transmit Complete interrupt flag (INTFLAG.TXC), since the transmit buffer no longer contains data.

After a collision, software must manually enable the transmitter again before continuing, after assuring that the CTRLB Synchronization Busy bit (SYNCBUSY.CTRLB) is not set.

32.6.3.6. Loop-Back Mode

For loop-back mode, configure the Receive Data Pinout (CTRLA.RXPO) and Transmit Data Pinout (CTRLA.TXPO) to use the same data pins for transmit and receive. The loop-back is through the pad, so the signal is also available externally.

32.6.3.7. Start-of-Frame Detection

The USART start-of-frame detector can wake up the CPU when it detects a start bit. In standby sleep mode, the internal fast startup oscillator must be selected as the GCLK_SERCOMx_CORE source.

When a 1-to-0 transition is detected on RxD, the 8MHz Internal Oscillator is powered up and the USART clock is enabled. After startup, the rest of the data frame can be received, provided that the baud rate is slow enough in relation to the fast startup internal oscillator start-up time. Refer to *Electrical Characteristics* for details. The start-up time of this oscillator varies with supply voltage and temperature.

The USART start-of-frame detection works both in asynchronous and synchronous modes. It is enabled by writing '1' to the Start of Frame Detection Enable bit in the Control B register (CTRLB.SFDE).

If the Receive Start Interrupt Enable bit in the Interrupt Enable Set register (INTENSET.RXS) is set, the Receive Start interrupt is generated immediately when a start is detected.

When using start-of-frame detection without the Receive Start interrupt, start detection will force the 8MHz Internal Oscillator and USART clock active while the frame is being received. In this case, the CPU will not wake up until the Receive Complete interrupt is generated.

Related Links

Electrical Characteristics on page 1144

32.6.3.8. Sample Adjustment

In asynchronous mode (CTRLA.CMODE=0), three samples in the middle are used to determine the value based on majority voting. The three samples used for voting can be selected using the Sample Adjustment bit field in Control A register (CTRLA.SAMPA). When CTRLA.SAMPA=0, samples 7-8-9 are used for 16x oversampling, and samples 3-4-5 are used for 8x oversampling.

32.8.11. Debug Control

Name: DBGCTRL
Offset: 0x30
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								DBGSTOP
Access								R/W
Reset								0

Bit 0 – DBGSTOP: Debug Stop Mode
This bit controls the baud-rate generator functionality when the CPU is halted by an external debugger.

Value	Description
0	The baud-rate generator continues normal operation when the CPU is halted by an external debugger.
1	The baud-rate generator is halted when the CPU is halted by an external debugger.

33.7. Register Summary

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0	RUNSTDBY			MODE[2:0]			ENABLE	SWRST
0x01		15:8								IBON
0x02		23:16			DIPO[1:0]				DOPO[1:0]	
0x03		31:24		DORD	CPOL	CPHA	FORM[3:0]			
0x04	CTRLB	7:0		PLOADEN				CHSIZE[2:0]		
0x05		15:8	AMODE[1:0]		MSSEN				SSDE	
0x06		23:16							RXEN	
0x07		31:24								
0x08 ... 0x0B	Reserved									
0x0C	BAUD	7:0	BAUD[7:0]							
0x0D ... 0x13	Reserved									
0x14	INTENCLR	7:0	ERROR				SSL	RXC	TXC	DRE
0x15	Reserved									
0x16	INTENSET	7:0	ERROR				SSL	RXC	TXC	DRE
0x17	Reserved									
0x18	INTFLAG	7:0	ERROR				SSL	RXC	TXC	DRE
0x19	Reserved									
0x1A	STATUS	7:0						BUFOVF		
0x1B		15:8								
0x1C	SYNCBUSY	7:0						CTRLB	ENABLE	SWRST
0x1D		15:8								
0x1E		23:16								
0x1F		31:24								
0x20 ... 0x23	Reserved									
0x24	ADDR	7:0	ADDR[7:0]							
0x25		15:8								
0x26		23:16	ADDRMASK[7:0]							
0x27		31:24								
0x28	DATA	7:0	DATA[7:0]							
0x29		15:8								DATA[8:8]
0x2A ... 0x2F	Reserved									
0x30	DBGCTRL	7:0								DBGSTOP

Table 34-2. Module Request for SERCOM I²C Master

Condition	Request		
	DMA	Interrupt	Event
Data needed for transmit (TX) (Master transmit mode)	Yes (request cleared when data is written)		NA
Data needed for transmit (RX) (Master transmit mode)	Yes (request cleared when data is read)		
Master on Bus (MB)		Yes	
Stop received (SB)		Yes	
Error (ERROR)		Yes	

34.6.4.1. DMA Operation

Smart mode must be enabled for DMA operation in the Control B register by writing CTRLB.SMEN=1.

Slave DMA

When using the I²C slave with DMA, an address match will cause the address interrupt flag (INTFLAG.ADDRMATCH) to be raised. After the interrupt has been serviced, data transfer will be performed through DMA.

The I²C slave generates the following requests:

- Write data received (RX): The request is set when master write data is received. The request is cleared when DATA is read.
- Read data needed for transmit (TX): The request is set when data is needed for a master read operation. The request is cleared when DATA is written.

Master DMA

When using the I²C master with DMA, the ADDR register must be written with the desired address (ADDR.ADDR), transaction length (ADDR.LEN), and transaction length enable (ADDR.LENEN). When ADDR.LENEN is written to 1 along with ADDR.ADDR, ADDR.LEN determines the number of data bytes in the transaction from 0 to 255. DMA is then used to transfer ADDR.LEN bytes followed by an automatically generated NACK (for master reads) and a STOP.

If a NACK is received by the slave for a master write transaction before ADDR.LEN bytes, a STOP will be automatically generated and the length error (STATUS.LENERR) will be raised along with the INTFLAG.ERROR interrupt.

The I²C master generates the following requests:

- Read data received (RX): The request is set when master read data is received. The request is cleared when DATA is read.
- Write data needed for transmit (TX): The request is set when data is needed for a master write operation. The request is cleared when DATA is written.

34.6.4.2. Interrupts

The I²C slave has the following interrupt sources. These are asynchronous interrupts. They can wake-up the device from any sleep mode:

- Error (ERROR)

Value	Description
0	Time-out disabled
1	Time-out enabled

Bits 21:20 – SDAHOLD[1:0]: SDA Hold Time
These bits define the SDA hold time with respect to the negative edge of SCL.

These bits are not synchronized.

Value	Name	Description
0x0	DIS	Disabled
0x1	75NS	50-100ns hold time
0x2	450NS	300-600ns hold time
0x3	600NS	400-800ns hold time

Bit 16 – PINOUT: Pin Usage
This bit set the pin usage to either two- or four-wire operation:

This bit is not synchronized.

Value	Description
0	4-wire operation disabled.
1	4-wire operation enabled.

Bit 7 – RUNSTDBY: Run in Standby
This bit defines the functionality in standby sleep mode.

This bit is not synchronized.

Value	Description
0	GCLK_SERCOMx_CORE is disabled and the I^2C master will not operate in standby sleep mode.
1	GCLK_SERCOMx_CORE is enabled in all sleep modes.

Bits 4:2 – MODE[2:0]: Operating Mode
These bits must be written to 0x5 to select the I^2C master serial communication interface of the SERCOM.

These bits are not synchronized.

Bit 1 – ENABLE: Enable
Due to synchronization, there is delay from writing CTRLA.ENABLE until the peripheral is enabled/disabled. The value written to CTRL.ENABLE will read back immediately and the Synchronization Enable Busy bit in the Synchronization Busy register (SYNCBUSY.ENABLE) will be set. SYNCBUSY.ENABLE will be cleared when the operation is complete.

This bit is not enable-protected.

39.5.1. I/O Lines

The USB pins may be multiplexed with the I/O lines Controller. The user must first configure the I/O Controller to assign the USB pins to their peripheral functions.

A 1kHz SOF clock is available on an external pin. The user must first configure the I/O Controller to assign the 1kHz SOF clock to the peripheral function. The SOF clock is available for device and host mode.

39.5.2. Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

Related Links

PM – Power Manager on page 192

39.5.3. Clocks

The USB bus clock (CLK_USB_AHB) can be enabled and disabled in the Power Manager, and the default state of CLK_USB_AHB can be found in the *Peripheral Clock Masking*.

A generic clock (GCLK_USB) is required to clock the USB. This clock must be configured and enabled in the Generic Clock Controller before using the USB. Refer to *GCLK - Generic Clock Controller* for further details.

This generic clock is asynchronous to the bus clock (CLK_USB_AHB). Due to this asynchronicity, writes to certain registers will require synchronization between the clock domains. Refer to *GCLK Synchronization* for further details.

The USB module requires a GCLK_USB of 48 MHz ± 0.25% clock for low speed and full speed operation. To follow the USB data rate at 12Mbit/s in full-speed mode, the CLK_USB_AHB clock should be at minimum 8MHz.

Clock recovery is achieved by a digital phase-locked loop in the USB module, which complies with the USB jitter specifications. If crystal-less operation is used in USB device mode, refer to *USB Clock Recovery Module*.

Related Links

GCLK - Generic Clock Controller on page 133

Synchronization on page 140

USB Clock Recovery Module on page 233

39.5.4. DMA

The USB has a built-in Direct Memory Access (DMA) and will read/write data to/from the system RAM when a USB transaction takes place. No CPU or DMA Controller resources are required.

39.5.5. Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller on page 52

39.5.6. Events

Not applicable.

Note: The pin VOUT0 will be dedicated as internal input and cannot be configured as alternate function.

44.6.3.2. Output Buffer Current Control

Power consumption can be reduced by controlling the output buffer current, according to conversion rate. Writing to the Current Control bits in DAC Control x register (DACCTRLx.[1:0]) will select an output buffer current.

44.6.3.3. Conversion Refresh

The DAC can only maintain its output within one LSB of the desired value for approximately 100µs. When a DAC is used to generate a static voltage or at a rate less than 20kSPS, the conversion must be refreshed periodically. The OSCULP32K clock can start new conversions automatically after a specified period. Write a value to the Refresh bit field in the DAC Control x register (DACCTRLx.REFRESH[3:0]) to select the refresh period according to the formula:

$$T_{\mathrm{REFRESH}} = \mathrm{REFRESH} \times T_{\mathrm{OSCULP32K}}$$

The actual period will depend on the tolerance of the OSCULP32K (see Electrical Characteristics).

If DACCTRLx.REFRESH=0, there is no conversion refresh. DACCTRLx.REFRESH=1 is Reserved.

If no new conversion is started before the refresh period is completed, DACx will convert the DATAx value again.

In standby sleep mode, the refresh mode remains enabled if DACCTRLx.RUNSTDBY=1.

If DATAx is written while a refresh conversion is ongoing, the conversion of the new content of DATAx is postponed until DACx is ready to start the next conversion.

Related Links

Electrical Characteristics on page 1144

44.6.3.4. Differential Mode

DAC0 and DAC1 can be configured to operate in differential mode, i.e. the combined output is a voltage balanced around VREF/2, see also the figure below.

In differential mode, DAC0 and DAC1 are converting synchronously the DATA0 value. DATA0 must therefore be a signed value, represented in two's complement format with DATA0[11] as the signed bit. DATA0 has therefore the range [-2047:2047].

VOUT0 is the positive output and VOUT1 the negative output. The differential output voltage is therefore:

$$V_{\mathrm{OUT}} = \frac{\mathrm{DATA0}}{2047} \times \mathrm{VREF} = \left(V_{\mathrm{OUT0}} - V_{\mathrm{OUT1}}\right)$$

DACCTRL0 serves as the configuration register for both DAC0 and DAC1. Therefore DACCTRL1 does not need to be written.

The differential mode is enabled by writing a '1' to the Differential bit in the Control B register (CTRLB.DIFF).

44.8.4. Interrupt Enable Clear

This register allows the user to disable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Interrupt Enable Set register (INTENSET).

Name: INTENCLR
Offset: 0x04
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
					EMPTY1	EMPTY0	UNDERRUN1	UNDERRUN0
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bit 3 – EMPTY1: Data Buffer 1 Empty Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 1 Empty Interrupt Enable bit, which disables the Data Buffer 1 Empty interrupt.

Value	Description
0	The Data Buffer 1 Empty interrupt is disabled.
1	The Data Buffer 1 Empty interrupt is enabled.

Bit 2 – EMPTY0: Data Buffer 0 Empty Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 0 Empty Interrupt Enable bit, which disables the Data Buffer 0 Empty interrupt.

Value	Description
0	The Data Buffer 0 Empty interrupt is disabled.
1	The Data Buffer 0 Empty interrupt is enabled.

Bit 1 – UNDERRUN1: Underrun Interrupt Enable for DAC1
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 1 Underrun Interrupt Enable bit, which disables the Data Buffer 1 Underrun interrupt.

Value	Description
0	The Data Buffer 1 Underrun interrupt is disabled.
1	The Data Buffer 1 Underrun interrupt is enabled.

Bit 0 – UNDERRUN0: Underrun Interrupt Enable for DAC0
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will clear the Data Buffer 0 Underrun Interrupt Enable bit, which disables the Data Buffer 0 Underrun interrupt.

46.10.8. DETREF

Table 46-32. Reference Voltage Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
ADC/DAC Ref	ADC/DAC internal reference	nom. 1.0V, V_{CC}=3.0V, T= 25°C	0.967	1.0	1.017	V
		nom. 1.1V, V_{CC}=3.0V, T= 25°C	1.069	1.1	1.120	
		nom. 1.2V, V_{CC}=3.0V, T= 25°C	1.167	1.2	1.227	
		nom. 1.25V, V_{CC}=3.0V, T= 25°C	1.214	1.25	1.280	
		nom. 2.0V, V_{CC}=3.0V, T= 25°C	1.935	2.0	2.032	
		nom. 2.2V, V_{CC}=3.0V, T= 25°C	2.134	2.2	2.242	
		nom. 2.4V, V_{CC}=3.0V, T= 25°C	2.328	2.4	2.458	
		nom. 2.5V, V_{CC}=3.0V, T= 25°C	2.420	2.5	2.565	
	Ref Temperature coefficient	drift over [-40, +25]°C	-	-0.01/+0.015	-	%/°C
		drift over [+25, +85]°C	-	-0.01/0.005	-	
	Ref Supply coefficient	drift over [1.6, 3.6]V	-	+/-0.35	-	%/V
AC Ref	AC Ref Accuracy	V_{CC}=3.0V, T=25°C	1.073	1.1	1.123	V
	Ref Temperature coefficient	drift over [-40, +25]°C	-	+/-0.01		%/°C
		drift over [+25, +85]°C	-	-0.005/+0.001	-	%/°C
	Ref Supply coefficient	drift over [1.6, 3.6]V	-	-0.35/+0.35	-	%/V

Note: These values are based on characterization.

Related Links

Reference Voltages on page 36

46.10.9. Temperature Sensor Characteristics

Table 46-33. Temperature Sensor Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ts_{Vout}	Temperature sensor output voltage	T= 25°C, V_{CC}=3.0V	-	656	-	mV
Ts_{Slope}	Temperature sensor slope	V_{CC} = 3.0V	-	2.24	-	mV/°C
$Ts_{V_{OUT}OV_{DDANA}}$	Variation over V_{DDANA} voltage	T= 25°C	-	1.1	-	mV/V
ADCTsAcc	Accuracy ADC conversion over Temperature(2)	T<0°C	-12	-	14	°C
		T>0°C	-8	-	9	°C
		T >30°C	-5	-	5	°C

Note:

1. These values are based on characterization.

Table 46-59. Power Consumption(1)

Symbol	Parameter	Conditions	TA	Min.	Typ.	Max.	Units
I_{DD}	Current Consumption	Ck=48MHz (PL0)	Max.85°C Typ.25°C	-	454	548	µA
		Ck=96MHz (PL2)		-	934	1052	

Note:

1. These values are based on characterization.

46.13. Timing Characteristics

46.13.1. External Reset Pin

Table 46-60. External Reset Characteristics(1)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{EXT}	Minimum reset pulse width		1	-	-	µs