Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21j17b-ant

2. The PM starts, clocks are switched to the slow clock (Core Clock, System Clock, Flash Clock and any Bus Clocks that do not have clock gate control). Internal resets are maintained due to the external reset.
3. The debugger maintains a low level on SWCLK. $\overline{\text{RESET}}$ is released, resulting in a debugger Cold-Plugging procedure.
4. The debugger generates a clock signal on the SWCLK pin, the Debug Access Port (DAP) receives a clock.
5. The CPU remains in Reset due to the Cold-Plugging procedure; meanwhile, the rest of the system is released.
6. A Chip-Erase is issued to ensure that the Flash is fully erased prior to programming.
7. Programming is available through the AHB-AP.
8. After the operation is completed, the chip can be restarted either by asserting $\overline{\text{RESET}}$, toggling power, or writing a '1' to the Status A register CPU Reset Phase Extension bit (STATUSA.CRSTEXT). Make sure that the SWCLK pin is high when releasing $\overline{\text{RESET}}$ to prevent extending the CPU reset.

Related Links

Electrical Characteristics on page 1144

NVMCTRL – Non-Volatile Memory Controller on page 489

Security Bit on page 497

15.9. Intellectual Property Protection

Intellectual property protection consists of restricting access to internal memories from external tools when the device is protected, and this is accomplished by setting the NVMCTRL security bit. This protected state can be removed by issuing a Chip-Erase (refer to Chip Erase). When the device is protected, read/write accesses using the AHB-AP are limited to the DSU address range and DSU commands are restricted. When issuing a Chip-Erase, sensitive information is erased from volatile memory and Flash.

The DSU implements a security filter that monitors the AHB transactions generated by the ARM AHB-AP inside the DAP. If the device is protected, then AHB-AP read/write accesses outside the DSU external address range are discarded, causing an error response that sets the ARM AHB-AP sticky error bits (refer to the ARM Debug Interface v5 Architecture Specification on http://www.arm.com).

The DSU is intended to be accessed either:

- Internally from the CPU, without any limitation, even when the device is protected
- Externally from a debug adapter, with some restrictions when the device is protected

For security reasons, DSU features have limitations when used from a debug adapter. To differentiate external accesses from internal ones, the first 0x100 bytes of the DSU register map have been replicated at offset 0x100:

- The first 0x100 bytes form the internal address range
- The next 0x100 bytes form the external address range

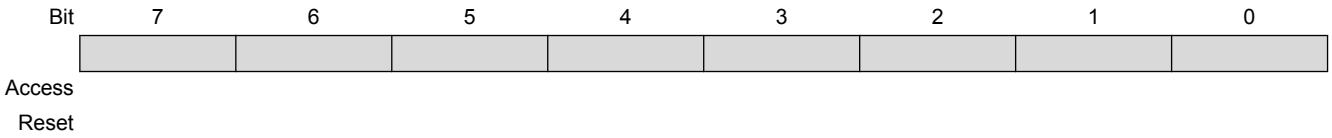
When the device is protected, the DAP can only issue MEM-AP accesses in the DSU address range limited to the 0x100- 0x2000 offset range.

The DSU operating registers are located in the 0x00-0xFF area and remapped in 0x100-0x1FF to differentiate accesses coming from a debugger and the CPU. If the device is protected and an access is issued in the region 0x100-0x1FF, it is subject to security restrictions. For more information, refer to the Table 15-1.

18.8.1. Control A

All bits in this register are reserved.

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection



18.8.10. APBC Mask

Name: APBCMASK
Offset: 0x1C
Reset: 0x0000 7FFF
Property: PAC Write-Protection

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
		TRNG	AES	DAC	TC3	TC2	TC1	TC0
Access		R	R	R	R	R	R	R
Reset		1	1	1	1	1	1	1

Bit	7	6	5	4	3	2	1	0
	TCC2	TCC1	TCC0	SERCOM4	SERCOM3	SERCOM2	SERCOM1	SERCOM0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	1	1	1	1	1	1	1

Bit 14 – TRNG: TRNG APBC Mask Clock Enable

Value	Description
0	The APBC clock for the TRNG is stopped.
1	The APBC clock for the TRNG is enabled.

Bit 13 – AES: AES APBC Mask Clock Enable

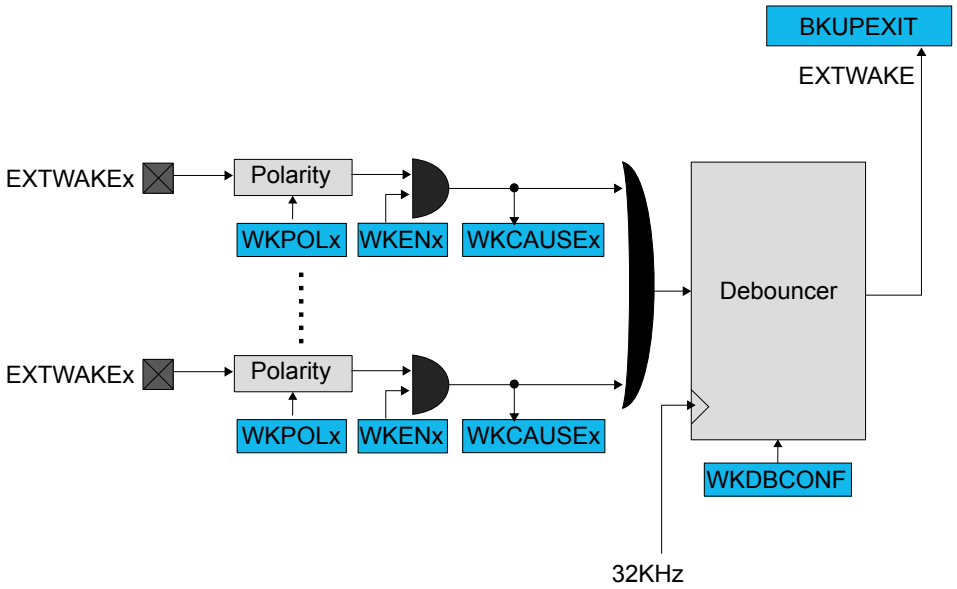
Value	Description
0	The APBC clock for the AES is stopped.
1	The APBC clock for the AES is enabled.

Bit 12 – DAC: DAC APBC Mask Clock Enable

Value	Description
0	The APBC clock for the DAC is stopped.
1	The APBC clock for the DAC is enabled.

Bit 11 – TC3: TC3 APBC Mask Clock Enable

Figure 19-2. External Wake-up Block Diagram



Related Links

OSC32KCTRL – 32KHz Oscillators Controller on page 273

19.6.2.4. Reset Causes and Effects

The latest Reset cause is available in RCAUSE register, and can be read during the application boot sequence in order to determine proper action.

These are the groups of Reset sources:

- Power supply Reset: Resets caused by an electrical issue. It covers POR and BODs Resets
- User Reset: Resets caused by the application. It covers external Resets, system Reset requests and watchdog Resets
- Backup reset: Resets caused by a Backup Mode exit condition

The following table lists the parts of the device that are reset, depending on the Reset type.

Table 19-1. Effects of the Different Reset Causes

	Power Supply Reset		User Reset		Backup Reset
	POR, BOD33	BOD12	External Reset	WDT Reset, System Reset Request	RTC, EXTWAKE, BBPS
RTC, OSC32KCTRL, RSTC, CTRLA.IORET bit of PM	Y	N	N	N	N
GCLK with WRTLOCK	Y	Y	N	N	Y
Debug logic	Y	Y	Y	N	Y
Others	Y	Y	Y	Y	Y

The external Reset is generated when pulling the $\overline{\text{RESET}}$ pin low.

19.8.1. Reset Cause

When a Reset occurs, the bit corresponding to the Reset source is set to '1' and all other bits are written to '0'.

Name: RCAUSE
Offset: 0x00
Reset: Latest Reset Source
Property: –

Bit	7	6	5	4	3	2	1	0
	BACKUP	SYST	WDT	EXT		BOD33	BOD12	POR
Access	R	R	R	R		R	R	R
Reset	x	x	x	x		x	x	x

Bit 7 – BACKUP: Backup Reset
This bit is set if a Backup Reset has occurred. Refer to BKUPEXIT register to identify the source of the Backup Reset.

Bit 6 – SYST: System Reset Request
This bit is set if a System Reset Request has occurred. Refer to the Cortex processor documentation for more details.

Bit 5 – WDT: Watchdog Reset
This bit is set if a Watchdog Timer Reset has occurred.

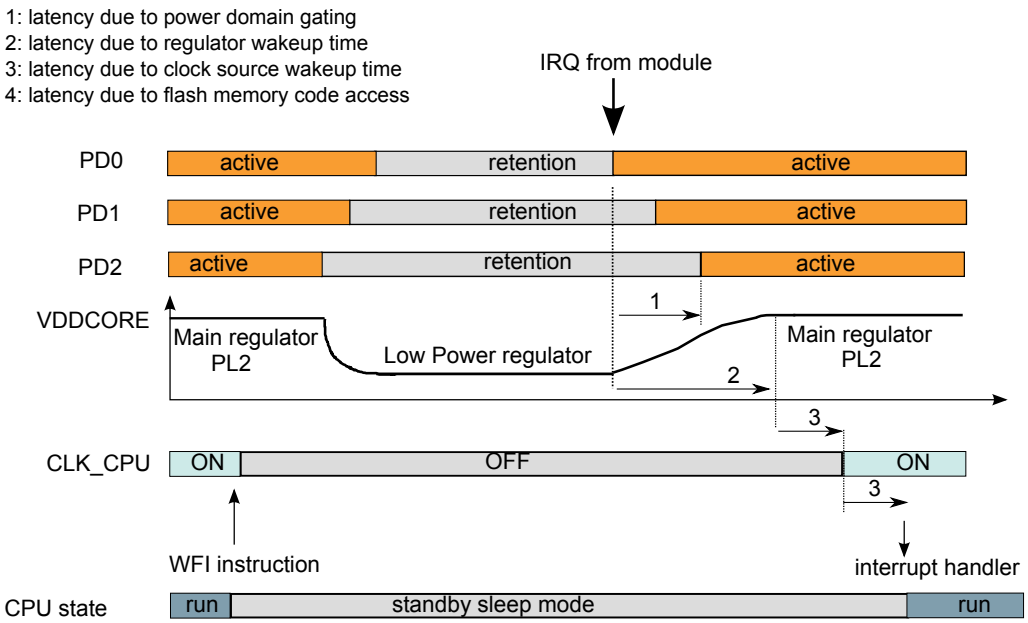
Bit 4 – EXT: External Reset
This bit is set if an external Reset has occurred.

Bit 2 – BOD33: Brown Out 33 Detector Reset
This bit is set if a BOD33 Reset has occurred.

Bit 1 – BOD12: Brown Out 12 Detector Reset
This bit is set if a BOD12 Reset has occurred.

Bit 0 – POR: Power On Reset
This bit is set if a POR has occurred.

Figure 20-5. Total Wake-up Time from Standby Sleep Mode



20.6.5. SleepWalking with Static Power Domain Gating in Details

In standby sleep mode, the switchable power domain (PD) of a peripheral can remain in active state in order to perform sleepwalking tasks, whereas the other power domains are in retention state to reduce power consumption. This SleepWalking with static Power Domain Gating is supported by all peripherals. For some peripherals it must be enabled by writing a Run in Standby bit in the respective Control A register (CTRLA.RUNSTDBY) to '1'. Refer to each peripheral chapter for details.

The following examples illustrate SleepWalking with static Power Domain Gating:

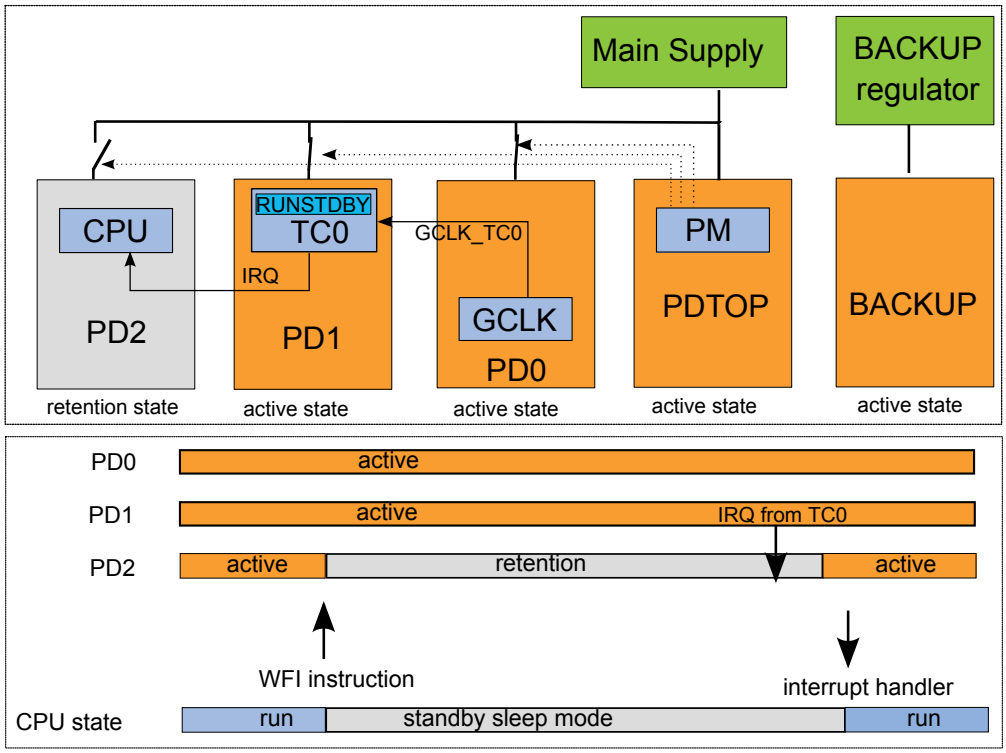
AC SleepWalking with Static PD Gating

The AC peripheral is used in continuous measurement mode to monitor voltage level on input pins. An AC interrupt is generated to wake up the device. To make the AC continue to run in standby sleep mode, the RUNSTDBY bit must be written to '1'.

- Entering standby mode: As shown in the next figure, PD0 (where the AC is located) remains active, whereas PD2 and PD1 are successively set to retention state by the Power Manager.

– In this case, the VDDCORE voltage is still supplied by the main voltage regulator, refer to Regulator Automatic Low Power Mode for details. Thus, global wake-up time is not affected by the regulator.

Figure 20-7. TC0 SleepWalking with Static PD Gating



EIC SleepWalking with Static PD Gating

In this example, EIC peripheral is used to detect an edge condition to generate interrupt to the CPU. An External interrupt pin is filtered by the CLK_ULP32K clock, GCLK peripheral is not used. Refer to Chapter EIC – External Interrupt Controller for details. The EIC peripheral is located in the power domain PDTOP (which is not switchable), and there is no RUNSTDBY bit in the EIC peripheral.

- Entering standby mode: As shown in Figure 20-8, all the switchable power domains are set in retention state by the Power Manager peripheral. The low power regulator supplies the VDDCORE voltage level.
- Exiting standby mode: When conditions are met, the EIC peripheral generates an interrupt to wake the device up. Successively, the PM peripheral sets PD0, PD1, and PD2 to active state, and the main voltage regulator restarts. Once PD2 is in active state and the main voltage regulator is ready, the CPU is able to operate normally and execute the EIC interrupt handler accordingly.
- Wake-up time:
  - The required time to set the switchable power domains to active state has to be considered for the global wake-up time, refer to Wake-Up Time for details.
  - When in standby sleep mode, the GCLK peripheral is not used, allowing the VDDCORE to be supplied by the low power regulator to reduce consumption, see Regulator Automatic Low Power Mode. Consequently, main voltage regulator wake-up time has to be considered for the global wake-up time as shown in Figure 20-8.

Value	Description
0	XOSC is not switched and provides the external clock or crystal oscillator clock.
1	XOSC is switched and provides the safe clock.

Bit 1 – CLKFAIL: XOSC Clock Failure

Value	Description
0	No XOSC failure detected.
1	A XOSC failure was detected.

Bit 0 – XOSCRDY: XOSC Ready

Value	Description
0	XOSC is not ready.
1	XOSC is stable and ready to be used as a clock source.

Note:

1. Actual startup time is 1 OSCULP32K cycle + 3 XOSC cycles.
2. The given time neglects the three XOSC cycles before OSCULP32K cycle.

Bit 11 – AMPGC: Automatic Amplitude Gain Control
Note: This bit must be set only after the XOSC has settled, indicated by the XOSC Ready flag in the Status register (STATUS.XOSCRDY).

Value	Description
0	The automatic amplitude gain control is disabled.
1	The automatic amplitude gain control is enabled. Amplitude gain will be automatically adjusted during Crystal Oscillator operation.

Bits 10:8 – GAIN[2:0]: Oscillator Gain
These bits select the gain for the oscillator. The listed maximum frequencies are recommendations, and might vary based on capacitive load and crystal characteristics. Those bits must be properly configured even when the Automatic Amplitude Gain Control is active.

Value	Recommended Max Frequency [MHz]
0x0	2
0x1	4
0x2	8
0x3	16
0x4	30
0x5-0x7	Reserved

Bit 7 – ONDEMAND: On Demand Control
The On Demand operation mode allows the oscillator to be enabled or disabled, depending on peripheral clock requests.

If the ONDEMAND bit has been previously written to '1', the oscillator will be running only when requested by a peripheral. If there is no peripheral requesting the oscillator's clock source, the oscillator will be in a disabled state.

If On Demand is disabled, the oscillator will always be running when enabled.

In standby sleep mode, the On Demand operation is still active.

Value	Description
0	The oscillator is always on, if enabled.
1	The oscillator is enabled when a peripheral is requesting the oscillator to be used as a clock source. The oscillator is disabled if no peripheral is requesting the clock source.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the XOSC behaves during standby sleep mode, together with the ONDEMAND bit:

STARTUP[2:0]	Number of OSCULP32K Clock Cycles	Number of XOSC32K Clock Cycles	Approximate Equivalent Time [s]
0x4	65536	3	2
0x5	131072	3	4
0x6	262144	3	8
0x7	-	-	Reserved

Note:

1. Actual Start-Up time is 1 OSCULP32K cycle + 3 XOSC32K cycles.
2. The given time assumes an XTAL frequency of 32.768kHz.

Bit 7 – ONDEMAND: On Demand Control
This bit controls how the XOSC32K behaves when a peripheral clock request is detected. For details, refer to XOSC32K Sleep Behavior.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the XOSC32K behaves during standby sleep mode. For details, refer to XOSC32K Sleep Behavior.

Bit 4 – EN1K: 1KHz Output Enable

Value	Description
0	The 1KHz output is disabled.
1	The 1KHz output is enabled.

Bit 3 – EN32K: 32KHz Output Enable

Value	Description
0	The 32KHz output is disabled.
1	The 32KHz output is enabled.

Bit 2 – XTALEN: Crystal Oscillator Enable
This bit controls the connections between the I/O pads and the external clock or crystal oscillator.

Value	Description
0	External clock connected on XIN32. XOUT32 can be used as general-purpose I/O.
1	Crystal connected to XIN32/XOUT32.

Bit 1 – ENABLE: Oscillator Enable

Value	Description
0	The oscillator is disabled.
1	The oscillator is enabled.

Offset	Name	Bit Pos.								
0x44	GP1	7:0	GP[7:0]							
0x45		15:8	GP[15:8]							
0x46		23:16	GP[23:16]							
0x47		31:24	GP[31:24]							

25.12. Register Description - CLOCK

This Register Description section is valid if the RTC is in Clock/Calendar mode (CTRLA.MODE=2).

Registers can be 8, 16, or 32 bits wide. Atomic 8-, 16-, and 32-bit accesses are supported. In addition, the 8-bit quarters and 16-bit halves of a 32-bit register, and the 8-bit halves of a 16-bit register can be accessed directly.

Some registers require synchronization when read and/or written. Synchronization is denoted by the "Read-Synchronized" and/or "Write-Synchronized" property in each individual register description.

Optional write-protection by the Peripheral Access Controller (PAC) is denoted by the "PAC Write-Protection" property in each individual register description.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

Value	Name	Description
0x0	NO_EVT_OUTPUT	No event output when using the resynchronized or synchronous path
0x1	RISING_EDGE	Event detection only on the rising edge of the signal from the event generator
0x2	FALLING_EDGE	Event detection only on the falling edge of the signal from the event generator
0x3	BOTH_EDGES	Event detection on rising and falling edges of the signal from the event generator

Bits 9:8 – PATH[1:0]: Path Selection
These bits are used to choose which path will be used by the selected channel.

The path choice can be limited by the channel source, see the table in USERm.

Value	Name	Description
0x0	SYNCHRONOUS	Synchronous path
0x1	RESYNCHRONIZED	Resynchronized path
0x2	ASYNCHRONOUS	Asynchronous path
0x3	-	Reserved

Bits 6:0 – EVGEN[6:0]: Event Generator
These bits are used to choose the event generator to connect to the selected channel.

Value	Event Generator	Description
0x00	NONE	No event generator selected
0x01	RTC CMP0	Compare 0 (mode 0 and 1) or Alarm 0 (mode 2)
0x02	RTC CMP1	Compare 1
0x03	RTC OVF	Overflow
0x04	RTC PER0	Period 0
0x05	RTC PER1	Period 1
0x06	RTC PER2	Period 2
0x07	RTC PER3	Period 3
0x08	RTC PER4	Period 4
0x09	RTC PER5	Period 5
0x0A	RTC PER6	Period 6
0x0B	RTC PER7	Period 7
0x0C	EIC EXTINT0	External Interrupt 0
0x0D	EIC EXTINT1	External Interrupt 1
0x0E	EIC EXTINT2	External Interrupt 2

Refer to *I/O Multiplexing and Considerations* for details on the pin mapping for this peripheral. One signal can be mapped on several pins.

Related Links

I/O Multiplexing and Considerations on page 30

36.5. Product Dependencies

In order to use this peripheral, other parts of the system must be configured correctly, as described below.

36.5.1. I/O Lines

In order to use the I/O lines of this peripheral, the I/O pins must be configured using the I/O Pin Controller (PORT).

Related Links

PORT: IO Pin Controller on page 512

36.5.2. Power Management

This peripheral can continue to operate in any sleep mode where its source clock is running. The interrupts can wake up the device from sleep modes. Events connected to the event system can trigger other operations in the system without exiting sleep modes.

36.5.3. Clocks

The TCC bus clock (CLK_TCCx_APB, with x instance number of the TCCx) is enabled by default, and can be enabled and disabled in the Main Clock.

A generic clock (GCLK_TCCx) is required to clock the TCC. This clock must be configured and enabled in the generic clock controller before using the TCC. Note that TCC0 and TCC1 share a peripheral clock generator.

The generic clocks (GCLK_TCCx) are asynchronous to the bus clock (CLK_TCCx_APB). Due to this asynchronicity, writing certain registers will require synchronization between the clock domains. Refer to Synchronization for further details.

Related Links

Peripheral Clock Masking on page 157

GCLK - Generic Clock Controller on page 133

36.5.4. DMA

The DMA request lines are connected to the DMA Controller (DMAC). In order to use DMA requests with this peripheral the DMAC must be configured first. Refer to *DMAC – Direct Memory Access Controller* for details.

Related Links

DMAC – Direct Memory Access Controller on page 406

36.5.5. Interrupts

The interrupt request line is connected to the Interrupt Controller. In order to use interrupt requests of this peripheral, the Interrupt Controller (NVIC) must be configured first. Refer to *Nested Vector Interrupt Controller* for details.

Related Links

Nested Vector Interrupt Controller on page 52

Table 36-8. Fault n Capture Action

Value	Name	Description
0x0	DISABLE	Capture on valid recoverable Fault n is disabled
0x1	CAPT	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each new captured value.
0x2	CAPTMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is lower than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local minimum detection.
0x3	CAPTMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0], if COUNT value is higher than the last stored capture value (CC). INTFLAG.FAULTn flag rises on each local maximun detection.
0x4	LOCMIN	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local minimum value detection.
0x5	LOCMAX	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun detection.
0x6	DERIV0	On rising edge of a valid recoverable Fault n, capture counter value on channel selected by CHSEL[1:0]. INTFLAG.FAULTn flag rises on each local maximun or minimum detection.

Bits 11:10 – CHSEL[1:0]: Recoverable Fault n Capture Channel
These bits select the channel for capture operation triggered by recoverable Fault n.

Value	Name	Description
0x0	CC0	Capture value stored into CC0
0x1	CC1	Capture value stored into CC1
0x2	CC2	Capture value stored into CC2
0x3	CC3	Capture value stored into CC3

Bits 9:8 – HALT[1:0]: Recoverable Fault n Halt Operation
These bits select the halt action for recoverable Fault n.

Value	Description
0	Overflow/underflow counter event is disabled and will not be generated.
1	Overflow/underflow counter event is enabled and will be generated for every counter overflow/underflow.

Bits 7:6 – CNTSEL[1:0]: Timer/Counter Interrupt and Event Output Selection
These bits define on which part of the counter cycle the counter event output is generated.

Value	Name	Description
0x0	BEGIN	An interrupt/event is generated at begin of each counter cycle
0x1	END	An interrupt/event is generated at end of each counter cycle
0x2	BETWEEN	An interrupt/event is generated between each counter cycle.
0x3	BOUNDARY	An interrupt/event is generated at begin of first counter cycle, and end of last counter cycle.

Bits 5:3 – EVACT1[2:0]: Timer/Counter Event Input 1 Action
These bits define the action the TCC will perform on TCE1 event input.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start restart or re-trigger TC on event
0x2	DIR (asynch)	Direction control
0x3	STOP	Stop TC on event
0x4	DEC	Decrement TC on event
0x5	PPW	Period captured into CC0 Pulse Width on CC1
0x6	PWP	Period captured into CC1 Pulse Width on CC0
0x7	FAULT	Non-recoverable Fault

Bits 2:0 – EVACT0[2:0]: Timer/Counter Event Input 0 Action
These bits define the action the TCC will perform on TCE0 event input 0.

Value	Name	Description
0x0	OFF	Event action disabled.
0x1	RETRIGGER	Start restart or re-trigger TC on event
0x2	COUNTEV	Count on event.
0x3	START	Start TC on event
0x4	INC	Increment TC on EVENT
0x5	COUNT (async)	Count on active state of asynchronous event
0x6	STAMP	Capture overflow times (Max value)
0x7	FAULT	Non-recoverable Fault

When PFREEZE bit is set while a transaction is in progress on the USB bus, this transaction will be properly completed. PFREEZE bit will be read as “1” only when the ongoing transaction will have been completed.

Value	Description
0	The Pipe operates in normal operation.
1	The Pipe is frozen and no additional requests will be sent to the device on this pipe address.

Bit 2 – CURBK: Current Bank

Value	Description
0	The bank0 is the bank that will be used in the next single/multi USB packet.
1	The bank1 is the bank that will be used in the next single/multi USB packet.

Bit 0 – DTGL: Data Toggle Sequence
Writing a one to the bit EPSTATUSCLR.DTGL will clear this bit.

Writing a one to the bit EPSTATUSSET.DTGL will set this bit.

This bit is toggled automatically by hardware after a data transaction.

This bit will reflect the data toggle in regards of the token type (IN/OUT/SETUP).

Value	Description
0	The PID of the next expected transaction will be zero: data 0.
1	The PID of the next expected transaction will be one: data 1.

42.8.3. Reference Control

Name: REFCTRL
Offset: 0x02
Reset: 0x00
Property: PAC Write-Protection, Enable-Protected

Bit	7	6	5	4	3	2	1	0
	REFCOMP				REFSEL[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit 7 – REFCOMP: Reference Buffer Offset Compensation Enable
The gain error can be reduced by enabling the reference buffer offset compensation. This will decrease the input impedance and thus increase the start-up time of the reference.

Value	Description
0	Reference buffer offset compensation is disabled.
1	Reference buffer offset compensation is enabled.

Bits 3:0 – REFSEL[3:0]: Reference Selection
These bits select the reference for the ADC.

Value	Name	Description
0x0	INTREF	internal variable reference voltage
x01	INTVCC0	1/1.6 VDDANA
0x2	INTVCC1	1/2 VDDANA (only for VDDANA > 2.0V)
0x3	VREFA	External reference
0x4	VREFB	External reference
0x5	INTVCC2	VDDANA
0x6 - 0xF		Reserved

Value	Name	Description
0x2	CC12M	6MHz < GCLK_DAC <= 12MHz (1MSPS)
0x3		Reserved

Bit 1 – ENABLE: Enable DAC1
This bit enables DAC1 when DAC Controller is enabled (CTRLA.ENABLE).

Value	Description
0	DAC1 is disabled.
1	DAC1 is enabled.

Bit 0 – LEFTADJ: Left Adjusted Data
This bit controls how the 12-bit conversion data is adjusted in the Data and Data Buffer registers.

Value	Description
0	DATA1 and DATABUF1 registers are right-adjusted.
1	DATA1 and DATABUF1 registers are left-adjusted.

Symbol	Parameters	Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference input	REFCOMP=1	1	-	V_{DDANA}-0.6	V
		REFCOMP=0	V_{DDANA}	-	V_{DDANA}	
V_{IN}	Input channel range	-	0	-	V_{DDANA}	V
V_{CMIN}	Input common mode voltage	For V_{REF} > 1.0V	0.7	-	V_{REF}-0.7	V
		For V_{REF}=1.0V	0.3	-	V_{REF}-0.3	
CSAMPLE(1)	Input sampling capacitance	-	-	2.8	3.2	pF
RSAMPLE(1)	Input sampling on-resistance	-	-	-	1715	Ω
Rref(1)	Reference input source resistance	REFCOMP=1	-	-	5	kΩ

Note:

1. These values are based on simulation. They are not covered by production test limits or characterization.

SERCOM I2C – SERCOM Inter-Integrated Circuit	• Editorial updates
OSCCTRL – Oscillators Controller	• Register XOSCCTRL.AMPGC must be set only when XOSC is ready • Editorial updates
OSC32KCTRL – 32KHz Oscillators Controller	• The XOSC32K signal may affect jitter of neighboring pads • Editorial updates
Packaging Information	• QFN center pad notes added
Schematic Checklist	• V_{SW}: recommended inductor with saturation current *above 150mA*.
ERRATA	Added new errata: • **ADC**: When window monitor is enabled and its output is 0, GCLK_ADC is kept running. Power consumption will be higher than expected in sleep modes. *Erratum reference: 14449* • **ADC**: The LSB bit of ADC result is stuck '0' in unipolar mode for 8-bit and 10-bit resolution. *Erratum reference: 14431* • **Device**: In IDLE sleep mode, the APB and AHB clocks are not stopped if the FDPLL is running as a GCLK clock source. *Erratum reference: 13401* Changed errata: • **Device**: The low latency mode cannot be enabled by writing '1' to 0x41008120. *Erratum reference: 13506* Removed errata: • Erratum 13918

53.8. Rev C - 03/2015

Configuration Summary	• Two ACs
NVM User Row Mapping	• 'BOD12 Enable' renamed to 'BOD12 Disable' • 'BOD33 Enable' renamed to 'BOD33 Disable'
Multiplexed Signals	• Editorial updates • PTC pins updated for die rev.B • OPAMP pins updated for die rev.B
PAC - Peripheral Access Controller	• No RFCTRL, ATW, TAL functionality