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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, LINbus, SCI, SPI, UART/USART, USB
Peripherals	DMA, POR, PWM, WDT
Number of I/O	51
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.62V ~ 3.63V
Data Converters	A/D 20x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/atsaml21j17b-aut

14. Peripherals Configuration Summary

Table 14-1. Peripherals Configuration Summary

Peripheral name	Base address	IRQ line	AHB clock		APB clock		Bus Clock Domain	Generic Clock	PAC		Events		DMA		Power domain
			Index	Enabled at Reset	Index	Enabled at Reset	Name	Index	Index	Prot at Reset	User	Generator	Index	Sleep Walking	Name
AHB-APB Bridge A	0x40000000	—	0	Y	—	—	Low Power	—	—	—	—	—	—	N/A	PD1
PM	0x40000000	0	—	—	0	Y	Backup	—	0	N	—	—	—	N/A	PDBACKUP
MCLK	0x40000400	0	—	—	1	Y	Low Power	—	1	N	—	—	—	Y	PD0
RSTC	0x40000800	—	—	—	2	Y	Backup	—	2	N	—	—	—	N/A	PDBACKUP
OSCCTRL	0x40000C00	0	—	—	3	Y	Low Power	0: DFLL48M reference 1: FDPLL96M clk source 2: FDPLL96M 32kHz	3	N	—	—	—	Y	PD0
OSC32KCTRL	0x40001000	0	—	—	4	Y	Backup	—	4	N	—	—	—	—	PDBACKUP
SUPC	0x40001400	0	—	—	5	Y	Backup	—	5	N	—	—	—	N/A	PDBACKUP
GCLK	0x40001800	—	—	—	6	Y	Low Power	—	6	N	—	—	—	N/A	PD0
WDT	0x40001C00	1	—	—	7	Y	Low Power	—	7	N	—	—	—	Y	PDTOP
RTC	0x40002000	2	—	—	8	Y	Backup	—	8	N	—	1: CMP0/ ALARM0 2: CMP1 3: OVF 4-11: PER0-7	—	Y	PDBACKUP
EIC	0x40002400	3, NMI	—	—	9	Y	Low Power	3	9	N	—	12-27: EXTINT0-15	—	Y	PDTOP
PORT	0x40002800	—	—	—	10	Y	Low Power	—	10	N	0-3 : EV0-3	—	—	Y	PDTOP
AHB-APB Bridge B	0x41000000	—	1	Y	—	—	CPU	—	—	—	—	—	—	N/A	PD2
USB	0x41000000	6	12	Y	0	Y	CPU	4	0	N	—	—	—	Y	PD2
DSU	0x41002000	—	5	Y	1	Y	CPU	—	1	Y	—	—	—	N/A	PD2
NVMCTRL	0x41004000	4	8	Y	2	Y	CPU	—	2	N	—	—	—	Y	PD2
MTB	0x41006000	—	—	—	—	—	CPU	—	—	—	43,44: Start, Stop	—	—	N/A	PD2
AHB-APB Bridge C	0x42000000	—	2	Y	—	—	Low Power	—	—	—	—	—	—	N/A	PD1
SERCOM0	0x42000000	8	—	—	0	Y	Low Power	18: CORE 17: SLOW	0	N	—	—	1: RX 2: TX	Y	PD1
SERCOM1	0x42000400	9	—	—	1	Y	Low Power	19: CORE 17: SLOW	1	N	—	—	3: RX 4: TX	Y	PD1
SERCOM2	0x42000800	10	—	—	2	Y	Low Power	20: CORE 17: SLOW	2	N	—	—	5: RX 6: TX	Y	PD1

15.13.21. Component Identification 2

Name: CID2
Offset: 0x1FF8
Reset: 0x00000005
Property: -

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

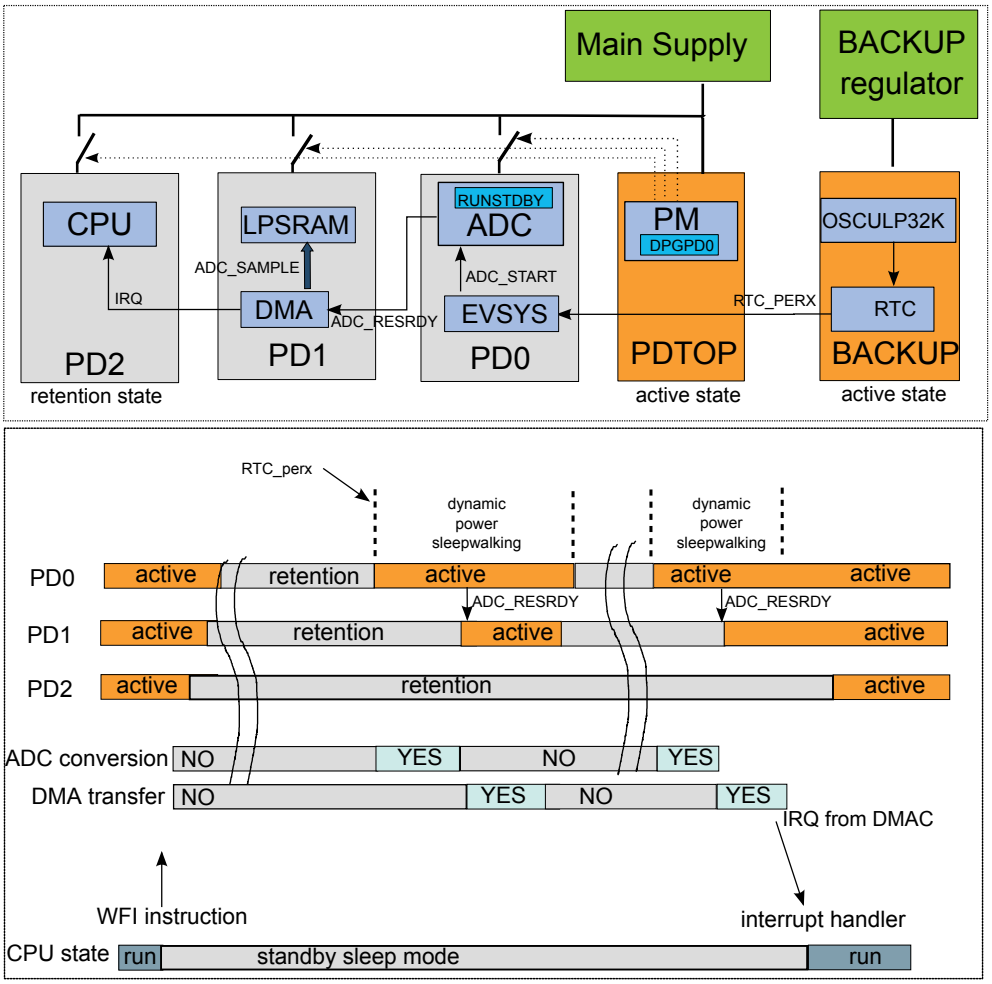
Bit	23	22	21	20	19	18	17	16
Access								
Reset								

Bit	15	14	13	12	11	10	9	8
Access								
Reset								

Bit	7	6	5	4	3	2	1	0
	PREAMBLEB2[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	1	0	1

Bits 7:0 – PREAMBLEB2[7:0]: Preamble Byte 2
These bits will always return 0x05 when read.

Figure 20-11. Dynamic Sleepwalking based on Peripheral DMA Trigger



The Analog to Digital Converter (ADC) peripheral is used in one shot measurement mode to periodically convert a voltage level on input pins, and move the conversion result to RAM by DMA. After N conversions, an interrupt is generated by the DMA to wake up the device. In the GCLK module, the ADC generic clock (GCLK_ADC) source is routed to OSCULP32K. RTC and EVSYS modules are configured to generate periodic events to the ADC.

To make the ADC continue to run in standby sleep mode, its Run in Standby (RUNSTDBY) bit is written to '1'. The DMAC is configured to operate in standby sleep mode as well by using its respective RUNSTDBY bit. A DMAC channel is configured to enable peripheral-to-memory transfer from the ADC to the LPSRAM and to generate an interrupt when the block transfer is completed (after N beat transfers). The Run in Standby bit of this DMAC channel is written to '1' to allow it running in standby sleep mode.

Entering Standby mode: The Power Manager peripheral sets PD0 (where the ADC peripheral is located), PD1 (the DMAC is located here) and PD2 (CPU) to retention state. The ADC channels are OFF. The GCLK_ADC clock is stopped. The VDDCORE is supplied by the low power regulator.

Dynamic SleepWalking: based on RTC conditions, a RTC event (RTC_PERX) is routed by the Event System to the ADC controller to trigger a single-shot measurement.

This event is detected by the Power Manager which sets the PD0 power domain to active state and starts the main voltage regulator.

Hours can be represented in either 12- or 24-hour format, selected by the Clock Representation bit in the Control A register (CTRLA.CLKREP). This bit can be changed only while the RTC is disabled.

The date is represented in this form:

- Day as the numeric day of the month (starting at 1)
- Month as the numeric month of the year (1 = January, 2 = February, etc.)
- Year as a value from 0x00 to 0x3F. This value must be added to a user-defined reference year. The reference year must be a leap year (2016, 2020 etc). Example: the year value 0x2D, added to a reference year 2016, represents the year 2061.

The RTC will increment until it reaches the top value of 23:59:59 December 31 of year value 0x3F, and then wrap to 00:00:00 January 1 of year value 0x00. This will set the Overflow Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.OVF).

The clock value is continuously compared with the 32-bit Alarm register (ALARM0). When an alarm match occurs, the Alarm 0 Interrupt flag in the Interrupt Flag Status and Clear registers (INTFLAG.ALARM0) is set on the next 0-to-1 transition of CLK_RTC_CNT.

A valid alarm match depends on the setting of the Alarm Mask Selection bits in the Alarm 0 Mask register (MASK0.SEL). These bits determine which time/date fields of the clock and alarm values are valid for comparison and which are ignored.

If the Clear on Match bit in the Control A register (CTRLA.MATCHCLR) is set, the counter is cleared on the next counter cycle when an alarm match with ALARM0 occurs. This allows the RTC to generate periodic interrupts or events with longer periods than it would be possible with the prescaler events only (see Periodic Intervals).
Note: When CTRLA.MATCHCLR is 1, INTFLAG.ALARM0 and INTFLAG.OVF will both be set simultaneously on an alarm match with ALARM0.

25.6.3. DMA Operation

Not applicable.

25.6.4. Interrupts

The RTC has the following interrupt sources:

- Overflow (OVF): Indicates that the counter has reached its top value and wrapped to zero.
- Compare (CMPn): Indicates a match between the counter value and the compare register.
- Alarm (ALARM): Indicates a match between the clock value and the alarm register.
- Period n (PERn): The corresponding bit in the prescaler has toggled. Refer to Periodic Intervals for details.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by setting the corresponding bit in the Interrupt Enable Set register (INTENSET=1), and disabled by setting the corresponding bit in the Interrupt Enable Clear register (INTENCLR=1).

An interrupt request is generated when the interrupt flag is raised and the corresponding interrupt is enabled. The interrupt request remains active until either the interrupt flag is cleared, the interrupt is disabled or the RTC is reset. See the description of the INTFLAG registers for details on how to clear interrupt flags.

All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. Refer to the Nested Vector Interrupt Controller for details. The user must read the INTFLAG register to determine which interrupt condition is present.

25.10.1. Control A in COUNT16 mode (CTRLA.MODE=1)

Name: CTRLA
Offset: 0x00
Reset: 0x0000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	COUNTSYNC				PRESCALER[3:0]			
Access	R/W				R/W	R/W	R/W	R/W
Reset	0				0	0	0	0

Bit	7	6	5	4	3	2	1	0
					MODE[1:0]		ENABLE	SWRST
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

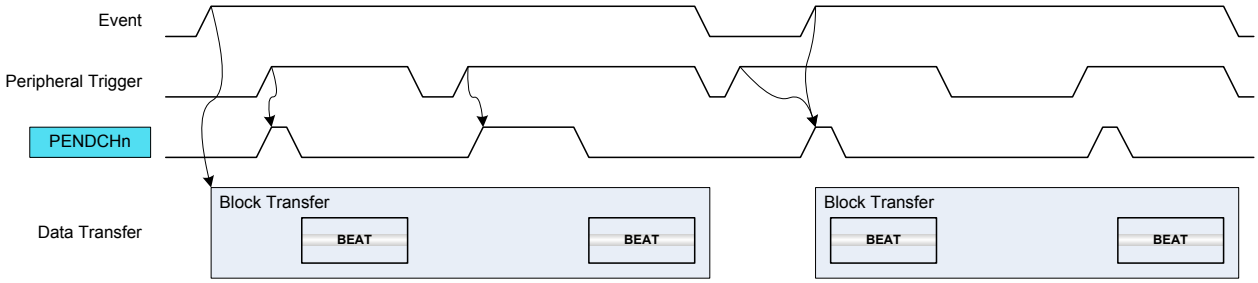
Bit 15 – COUNTSYNC: COUNT Read Synchronization Enable
The COUNT register requires synchronization when reading. Disabling the synchronization will prevent reading valid values from the COUNT register.
This bit is not enable-protected.

Value	Description
0	COUNT read synchronization is disabled
1	COUNT read synchronization is enabled

Bits 11:8 – PRESCALER[3:0]: Prescaler
These bits define the prescaling factor for the RTC clock source (GCLK_RTC) to generate the counter clock (CLK_RTC_CNT). Periodic events and interrupts are not available when the prescaler is off. These bits are not synchronized.

Value	Name	Description
0x0	OFF	CLK_RTC_CNT = GCLK_RTC/1
0x1	DIV1	CLK_RTC_CNT = GCLK_RTC/1
0x2	DIV2	CLK_RTC_CNT = GCLK_RTC/2
0x3	DIV4	CLK_RTC_CNT = GCLK_RTC/4
0x4	DIV8	CLK_RTC_CNT = GCLK_RTC/8
0x5	DIV16	CLK_RTC_CNT = GCLK_RTC/16
0x6	DIV32	CLK_RTC_CNT = GCLK_RTC/32
0x7	DIV64	CLK_RTC_CNT = GCLK_RTC/64
0x8	DIV128	CLK_RTC_CNT = GCLK_RTC/128
0x9	DIV256	CLK_RTC_CNT = GCLK_RTC/256
0xA	DIV512	CLK_RTC_CNT = GCLK_RTC/512

Figure 26-14. Conditional Block Transfer with Beat Peripheral Triggers



Channel Suspend

The event input is used to suspend an ongoing channel operation. The event is acknowledged when the current AHB access is completed. For further details on Channel Suspend, refer to Channel Suspend.

Channel Resume

The event input is used to resume a suspended channel operation. The event is acknowledged as soon as the event is received and the Channel Suspend Interrupt Flag (CHINTFLAG.SUSP) is cleared. For further details refer to Channel Suspend.

Skip Next Block Suspend

This event can be used to skip the next block suspend action. If the channel is suspended before the event rises, the channel operation is resumed and the event is acknowledged. If the event rises before a suspend block action is detected, the event is kept until the next block suspend detection. When the block transfer is completed, the channel continues the operation (not suspended) and the event is acknowledged.

26.6.3.5. Event Output Selection

Event output selection is available only for the least significant DMA channels. The pulse width of an event output from a channel is one AHB clock cycle.

The output of channel events is enabled by writing a '1' to the Channel Event Output Enable bit in the Control B register (CHCTRLB.EVOE). The event output cause is selected by writing to the Event Output Selection bits in the Block Transfer Control register (BTCTRL.EVOSEL). It is possible to generate events after each block transfer (BTCTRL.EVOSEL=0x1) or beat transfer (BTCTRL.EVOSEL=0x3). To enable an event being generated when a transaction is complete, the block event selection must be set in the last transfer descriptor only.

The figure Figure 26-15 shows an example where the event output generation is enabled in the first block transfer, and disabled in the second block.

26.8.21. Channel Interrupt Enable Set

This register allows the user to enable an interrupt without doing a read-modify-write operation. Changes in this register will also be reflected in the Channel Interrupt Enable Clear (CHINTENCLR) register.
This register affects the DMA channel that is selected in the Channel ID register (CHID.ID).

Name: CHINTENSET
Offset: 0x4D
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
						SUSP	TCMPL	TERR
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – SUSP: Channel Suspend Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Suspend Interrupt Enable bit, which enables the Channel Suspend interrupt.

Value	Description
0	The Channel Suspend interrupt is disabled.
1	The Channel Suspend interrupt is enabled.

Bit 1 – TCMPL: Channel Transfer Complete Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Transfer Complete Interrupt Enable bit, which enables the Channel Transfer Complete interrupt.

Value	Description
0	The Channel Transfer Complete interrupt is disabled.
1	The Channel Transfer Complete interrupt is enabled.

Bit 0 – TERR: Channel Transfer Error Interrupt Enable
Writing a '0' to this bit has no effect.

Writing a '1' to this bit will set the Channel Transfer Error Interrupt Enable bit, which enables the Channel Transfer Error interrupt.

Value	Description
0	The Channel Transfer Error interrupt is disabled.
1	The Channel Transfer Error interrupt is enabled.

Some registers are enable-protected, meaning they can only be written when the module is disabled. Enable-protection is denoted by the "Enable-Protected" property in each individual register description.

28.8.9. Lock Section

Name: LOCK
Offset: 0x20
Reset: 0xXXXX
Property: –

Bit	15	14	13	12	11	10	9	8
	LOCK[15:8]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	LOCK[7:0]							
Access	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	x

Bits 15:0 – LOCK[15:0]: Region Lock Bits
In order to set or clear these bits, the CMD register must be used.

Default state after erase will be unlocked (0x0000).

Value	Description
0	The corresponding lock region is locked.
1	The corresponding lock region is not locked.

30.8.1. Control A

Name: CTRLA
Offset: 0x00
Reset: 0x00
Property: PAC Write-Protection

Bit	7	6	5	4	3	2	1	0
								SWRST
Access								W
Reset								0

Bit 0 – SWRST: Software Reset
Writing '0' to this bit has no effect.
Writing '1' to this bit resets all registers in the EVSYS to their initial state.

Note: Before applying a Software Reset it is recommended to disable the event generators.

32.8.2. Control B

Name: CTRLB
Offset: 0x04
Reset: 0x00000000
Property: PAC Write-Protection, Enable-Protected, Write-Synchronized

Bit	31	30	29	28	27	26	25	24
Access								
Reset								

Bit	23	22	21	20	19	18	17	16
							RXEN	TXEN
Access							R/W	R/W
Reset							0	0

Bit	15	14	13	12	11	10	9	8
			PMODE			ENC	SFDE	COLDEN
Access			R/W			R/W	R/W	R/W
Reset			0			0	0	0

Bit	7	6	5	4	3	2	1	0
		SBMODE				CHSIZE[2:0]		
Access		R/W				R/W	R/W	R/W
Reset		0				0	0	0

Bit 17 – RXEN: Receiver Enable
Writing '0' to this bit will disable the USART receiver. Disabling the receiver will flush the receive buffer and clear the FERR, PERR and BUFOVF bits in the STATUS register.

Writing '1' to CTRLB.RXEN when the USART is disabled will set CTRLB.RXEN immediately. When the USART is enabled, CTRLB.RXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the receiver is enabled. When the receiver is enabled, CTRLB.RXEN will read back as '1'.

Writing '1' to CTRLB.RXEN when the USART is enabled will set SYNCBUSY.CTRLB, which will remain set until the receiver is enabled, and CTRLB.RXEN will read back as '1'.

This bit is not enable-protected.

Value	Description
0	The receiver is disabled or being enabled.
1	The receiver is enabled or will be enabled when the USART is enabled.

Bit 16 – TXEN: Transmitter Enable
Writing '0' to this bit will disable the USART transmitter. Disabling the transmitter will not become effective until ongoing and pending transmissions are completed.

Writing '1' to CTRLB.TXEN when the USART is disabled will set CTRLB.TXEN immediately. When the USART is enabled, CTRLB.TXEN will be cleared, and SYNCBUSY.CTRLB will be set and remain set until the transmitter is enabled. When the transmitter is enabled, CTRLB.TXEN will read back as '1'.

Value	Description
0	Transmit Complete interrupt is disabled.
1	Transmit Complete interrupt is enabled.

Bit 0 – DRE: Data Register Empty Interrupt Enable
Writing '0' to this bit has no effect.

Writing '1' to this bit will clear the Data Register Empty Interrupt Enable bit, which disables the Data Register Empty interrupt.

Value	Description
0	Data Register Empty interrupt is disabled.
1	Data Register Empty interrupt is enabled.

When PFREEZE bit is set while a transaction is in progress on the USB bus, this transaction will be properly completed. PFREEZE bit will be read as “1” only when the ongoing transaction will have been completed.

Value	Description
0	The Pipe operates in normal operation.
1	The Pipe is frozen and no additional requests will be sent to the device on this pipe address.

Bit 2 – CURBK: Current Bank

Value	Description
0	The bank0 is the bank that will be used in the next single/multi USB packet.
1	The bank1 is the bank that will be used in the next single/multi USB packet.

Bit 0 – DTGL: Data Toggle Sequence
Writing a one to the bit EPSTATUSCLR.DTGL will clear this bit.

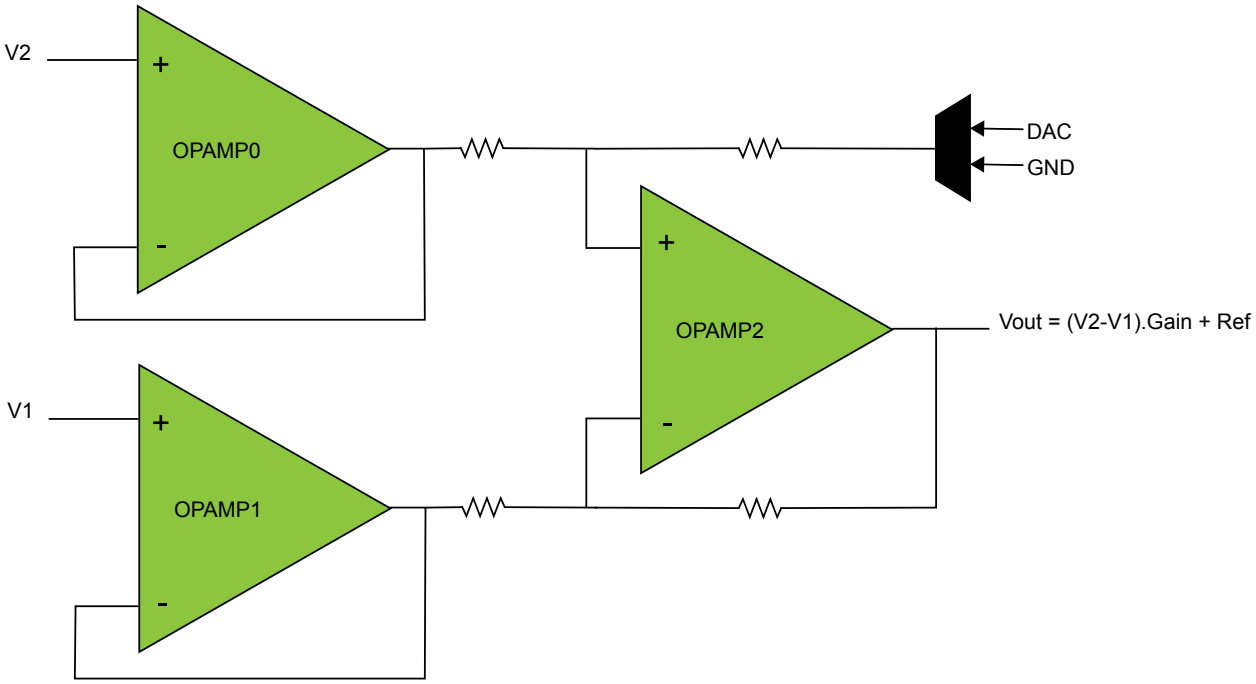
Writing a one to the bit EPSTATUSSET.DTGL will set this bit.

This bit is toggled automatically by hardware after a data transaction.

This bit will reflect the data toggle in regards of the token type (IN/OUT/SETUP).

Value	Description
0	The PID of the next expected transaction will be zero: data 0.
1	The PID of the next expected transaction will be one: data 1.

Figure 41-8. Instrumentation amplifier



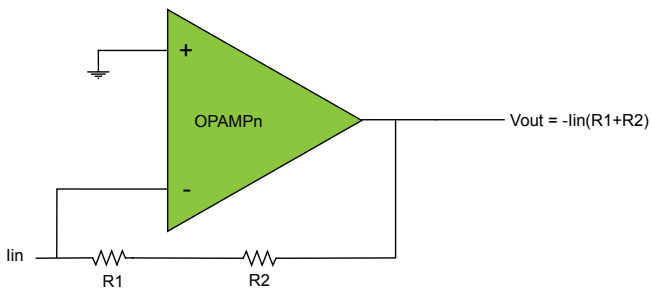
41.6.10.8. Transimpedance amplifier

Each OPAMP can be configured as a transimpedance amplifier (current to voltage converter). In this mode the positive input is connected to ground. The negative input is connected to the output through the resistor ladder. The OPAMPCTRLx register can be configured as follows:

Table 41-11. Transimpedance Amplifier

	MUXPOS	MUXNEG	RES1MUX	POTMUX	RES2VCC	RES2OUT	RES1EN	ANAOUT
OPAMP0	011	000	01	000	0	1	1	0
OPAMP1	011	000	01	000	0	1	1	0
OPAMP2	011	000	01	000	0	1	1	0

Figure 41-9. Transimpedance Amplifier



41.6.10.9. Programmable Hysteresis

Each OPAMP can be configured as an inverting or non-inverting comparator with programmable hysteresis. Applying hysteresis will prevent constant toggling of the output, caused by noise when the input signals are close to each other.

Value	OPAMPx	Name	Description
0x2	x=0	DAC	DAC output
	x=1	OA0OUT	OPAMP0 output
	x=2	OA1OUT	OPAMP1 output
0x3	x=0,1,2	GND	

Bit 10 – RES1EN: Resistor 1 Enable

Value	Description
0	R1 disconnected from RES1MUX.
1	R1 connected to RES1MUX.

Bit 9 – RES2VCC: Resistor ladder To VCC

Value	Description
0	Swith open.
1	Switch closed.

Bit 8 – RES2OUT: Resistor ladder To Output

Value	Description
0	Swith open.
1	Switch closed.

Bit 7 – ONDEMAND: On Demand Control
The On Demand operation mode allows the OPAMPx to be enabled or disabled, depending on other peripheral requests.

Value	Description
0	The OPAMPx is always on, if enabled.
1	The OPAMPx is enabled when a peripheral is requesting the OPAMPx to be used as an input. The OPAMPx is disabled if no peripheral is requesting it as an input.

Bit 6 – RUNSTDBY: Run in Standby
This bit controls how the OPAMPx behaves during standby sleep mode:

Value	Description
0	The OPAMPx is disabled in standby sleep mode.
1	The OPAMPx is not stopped in standby sleep mode. If OPAMPCTRLx.ONDEMAND=1, the OPAMPx will be running when a peripheral is requesting it as an input. If OPAMPCTRLx.ONDEMAND=0, OPAMPx will always be running in standby sleep mode.

Bits 4:3 – BIAS[1:0]: Bias Selection
These bits are used to select the bias mode.

42.8.13. Window Monitor Lower Threshold

Name: WINLT
Offset: 0x0E
Reset: 0x0000
Property: PAC Write-Protection, Write-Synchronized

Bit	15	14	13	12	11	10	9	8
	WINLT[15:8]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit	7	6	5	4	3	2	1	0
	WINLT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 15:0 – WINLT[15:0]: Window Lower Threshold
If the window monitor is enabled, these bits define the lower threshold value.

These bits are not synchronized.

Value	Description
0	The output of MUXPOS connects to the positive input, and the output of MUXNEG connects to the negative input.
1	The output of MUXNEG connects to the positive input, and the output of MUXPOS connects to the negative input.

Bits 14:12 – MUXPOS[2:0]: Positive Input Mux Selection
These bits select which input will be connected to the positive input of comparator n. COMPCTRLn.MUXPOS can be written only while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	VSCALE	VDD scaler
0x5–0x7	-	Reserved

Bits 10:8 – MUXNEG[2:0]: Negative Input Mux Selection
These bits select which input will be connected to the negative input of comparator n. COMPCTRLn.MUXNEG can only be written while COMPCTRLn.ENABLE is zero.

These bits are not synchronized.

Value	Name	Description
0x0	PIN0	I/O pin 0
0x1	PIN1	I/O pin 1
0x2	PIN2	I/O pin 2
0x3	PIN3	I/O pin 3
0x4	GND	Ground
0x5	VSCALE	VDD scaler
0x6	BANDGAP	Internal bandgap voltage
0x7	DAC / OPAMP	DAC0 output (COMP0) OPAMP2 output (COMP1)

Bit 6 – RUNSTDBY: Run in Standby
This bit controls the behavior of the comparator during standby sleep mode.

This bit is not synchronized

- Data Buffer 1 Empty (EMPTY1): The request is set when data is transferred from DATABUF1 or DATA1 to the internal data buffer of DAC1. The request is cleared when either DATA0 register or DATABUF1 register is written, or by writing a one to the EMPTY1 bit in the Interrupt Flag register (INTFLAG.EMPTY1).

In differential mode (CTRLB.DIFF=1), DAC Controller generates the following DMA request:

- Data Buffer 0 Empty (EMPTY0): The request is set when data is transferred from DATABUF0 or DATA0 to the internal data buffer of DAC1. The request is cleared when either DATA0 register or DATABUF0 register is written, or by writing a one to the EMPTY0 bit in the Interrupt Flag register (INTFLAG.EMPTY0).

If the CPU accesses the registers which are source of DMA request set/clear condition, the DMA request can be lost or the DMA transfer can be corrupted, if enabled.

44.6.6. Interrupts

The DAC Controller has the following interrupt sources:

- DAC0 Data Buffer Empty (EMPTY0): Indicates that the internal data buffer of DAC0 is empty.
- DAC1 Data Buffer Empty (EMPTY1): Indicates that the internal data buffer of DAC1 is empty.
- DAC0 Underrun (UNDERRUN0): Indicates that the internal data buffer of DAC0 is empty and a DAC0 start of conversion event occurred. Refer to Events for details.
- DAC1 Underrun (UNDERRUN1): Indicates that the internal data buffer of DAC1 is empty and a DAC1 start of conversion event occurred. Refer to Events for details.

These interrupts are asynchronous wake-up sources. See *Sleep Mode Controller* for details.

Each interrupt source has an interrupt flag associated with it. The interrupt flag in the Interrupt Flag Status and Clear (INTFLAG) register is set when the interrupt condition occurs. Each interrupt can be individually enabled by writing a '1' to the corresponding bit in the Interrupt Enable Set (INTENSET) register, and disabled by writing a '1' to the corresponding bit in the Interrupt Enable Clear (INTENCLR) register.

An interrupt request is generated when the interrupt flag is set and the corresponding interrupt is enabled. The interrupt request remains active until the interrupt flag is cleared, the interrupt is disabled, or the DAC Controller is reset. See INTFLAG for details on how to clear interrupt flags.

All interrupt requests from the peripheral are ORed together on system level to generate one combined interrupt request to the NVIC. Refer to *Nested Vector Interrupt Controller* for details. The user must read the INTFLAG register to determine which interrupt condition is present.

Note that interrupts must be globally enabled for interrupt requests to be generated. Refer to *Nested Vector Interrupt Controller* for details.

44.6.7. Events

The DAC Controller can generate the following output events:

- Data Buffer 0 Empty (EMPTY0): Generated when the internal data buffer of DAC0 is empty. Refer to DMA Operation for details.
- Data Buffer 1 Empty (EMPTY1): Generated when the internal data buffer of DAC1 is empty. Refer to DMA Operation for details.

Writing a '1' to an Event Output bit in the Event Control Register (EVCTRL.EMPTYEOx) enables the corresponding output event. Writing a '0' to this bit disables the corresponding output event. Refer to the Event System chapter for details on configuring the event system.

The DAC Controller can take the following actions on an input event:

Errata reference: 15264
Fix/Workaround:
Enable the main voltage regulator in standby mode (SUPC.VREG.RUNSTDBY=1) and set the Standby in PL0 bit to one (SUPC.VREG.STDBYPL0=1).

50.3.2. TC

1 – When clearing STATUS.xxBUFV flag, SYNCBUSY is released before the register is restored to its appropriate value.
Errata reference: 15056
Fix/Workaround:
To ensure that the register value is properly restored before updating this same register through xx or xxBuf with a new value, the STATUS.xxBUFV flag must be cleared successively two times.

50.3.3. DAC

1 – For specific DAC configurations, the SYNCBUSY.DATA1 and SYNCBUSY.DATABUF1 may be stuck at 1.
Errata reference: 14910
Fix/Workaround:
Don't use the Refresh mode and Events at the same time for DAC1. If event is used, write data to DATABUF1 with no refresh. DAC0 is not limited by this restriction.

2 – The SYNCBUSY.ENABLE bit is stuck at 1 after disabling and enabling the DAC when refresh is used.
Errata reference: 14885
Fix/Workaround:
After the DAC is disabled in refresh mode, wait for at least 30us before re-enabling the DAC.

50.3.4. TRNG

1 – When TRNG is enabled with configuration CTRL.RUNSTDBY = 0, (disabled during sleep) it could still continue to operate resulting in over-consumption (~50uA) in standby mode.
Errata reference: 14827
Fix/Workaround:
Disable the TRNG before entering standby mode.

50.3.5. DFLL48M

1 – The DFLL clock must be requested before being configured otherwise a write access to a DFLL register can freeze the device.
Errata reference: 9905
Fix/Workaround:
Write a zero to the DFLL ONDEMAND bit in the DFLLCTRL register before configuring the DFLL module.

2 – If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if

53. Datasheet Revision History

53.1. Rev J - 06/2016

Document	• Editorial updates.
Configuration Summary Ordering Information	• Ordering Code ATSAML21J17B-UUT (128KB Flash/ 16KB SRAM in WLCSP64) added.
I/O Multiplexing and Considerations	• Footnote (5) also applies for PB08.
NVM User Row Mapping	• Updated. • NVM Temperature Log Row added. • Factory settings added. • BODCORE not configurable.
DSU - Device Service Unit	• MBIST not available when device is operated from external address range and device is protected.
GCLK - Generic Clock Controller	• Editorial updates.
RTC – Real-Time Counter	• General Purpose (GPn) registers available. • Editorial updates.
DMAC – Direct Memory Access Controller	• Register properties updated. • Editorial updates
EIC – External Interrupt Controller	• Register properties updated.
OSC32KCTRL – 32KHz Oscillators Controller	• Editorial updates.
SUPC – Supply Controller	• Editorial updates.
WDT – Watchdog Timer	• Register properties updated.
SERCOM USART – SERCOM Universal Synchronous and Asynchronous Receiver and Transmitter	• Editorial updates.
TCC – Timer/Counter for Control Applications	• TCC configuration summary moved to TCC Configurations.
AES – Advanced Encryption Standard	• Register address offsets corrected.
AC – Analog Comparators	• Register properties updated. • Editorial updates.