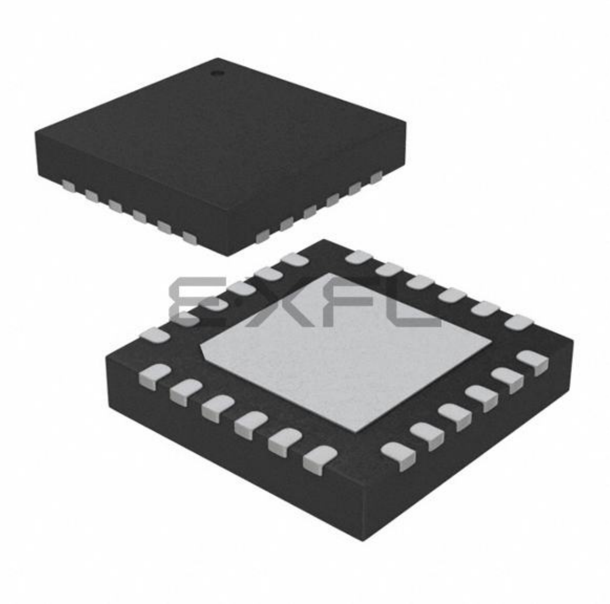


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	AVR
Core Size	8-Bit
Speed	20MHz
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PWM, WDT
Number of I/O	22
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 24x10b; D/A 3x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-VQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/attiny3217-mnr

6.10.4.9 Lockbits

Name: LOCKBIT
Offset: 0x0A
Reset: -
Property: -

Bit	7	6	5	4	3	2	1	0
	LOCKBIT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – LOCKBIT[7:0] Lockbits
When the part is locked, UPDI cannot access the system bus, so it cannot read out anything but CS-space.

Value	Description
`0xC5`	Valid key - the device is open
`other`	Invalid - the device is locked

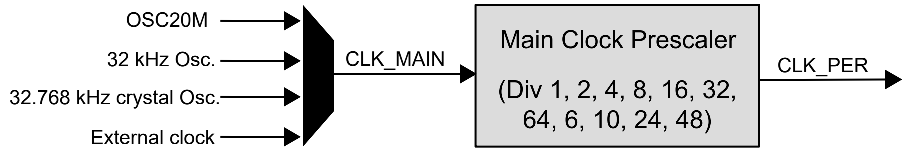
Related Links
6.9 Memory Section Access from CPU and UPDI on Locked Device

30. ADC - Analog-to-Digital Converter

7.3 System Configuration (SYSCFG)

The system configuration contains the revision ID of the part. The revision ID is readable from the CPU, making it useful for implementing application changes between part revisions.

Figure 10-2. Main Clock and Prescaler



The Main Clock and Prescaler configuration registers (CLKCTRL.MCLKCTRLA, CLKCTRL.MCLKCTRLB) are protected by the Configuration Change Protection Mechanism, employing a timed write procedure for changing these registers.

Related Links

8.5.7 Configuration Change Protection (CCP)

10.3.3 Main Clock After Reset

After any Reset, CLK_MAIN is provided by the 16/20 MHz Oscillator (OSC20M) and with a prescaler division factor of 6. Since the actual frequency of the OSC20M is determined by the Frequency Select bits (FREQSEL) of the Oscillator Configuration fuse (FUSE.OSCCFG), these frequencies are possible after Reset:

Table 10-1. Peripheral Clock Frequencies After Reset

CLK_MAIN as Per FREQSEL in FUSE.OSCCFG	Resulting CLK_PER
16 MHz	2.66 MHz
20 MHz	3.3 MHz

See the OSC20M description for further details.

Related Links

10.3.4.1.1 16/20 MHz Oscillator (OSC20M)

10.3.4 Clock Sources

All internal clock sources are enabled automatically when they are requested by a peripheral. The crystal oscillator, based on an external crystal, must be enabled by writing a '1' to the ENABLE bit in the 32 KHz Crystal Oscillator Control A register (CLKCTRL.XOSC32KCTRLA) before it can serve as a clock source.

The respective Oscillator Status bits in the Main Clock Status register (CLKCTRL.MCLKSTATUS) indicate whether the clock source is running and stable.

Related Links

6.10 Configuration and User Fuses (FUSE)
8.5.7 Configuration Change Protection (CCP)

10.3.4.1 Internal Oscillators

The internal oscillators do not require any external components to run. See the related links for accuracy and electrical characteristics.

Related Links

37. Electrical Characteristics

12. RSTCTRL - Reset Controller

12.1 Features

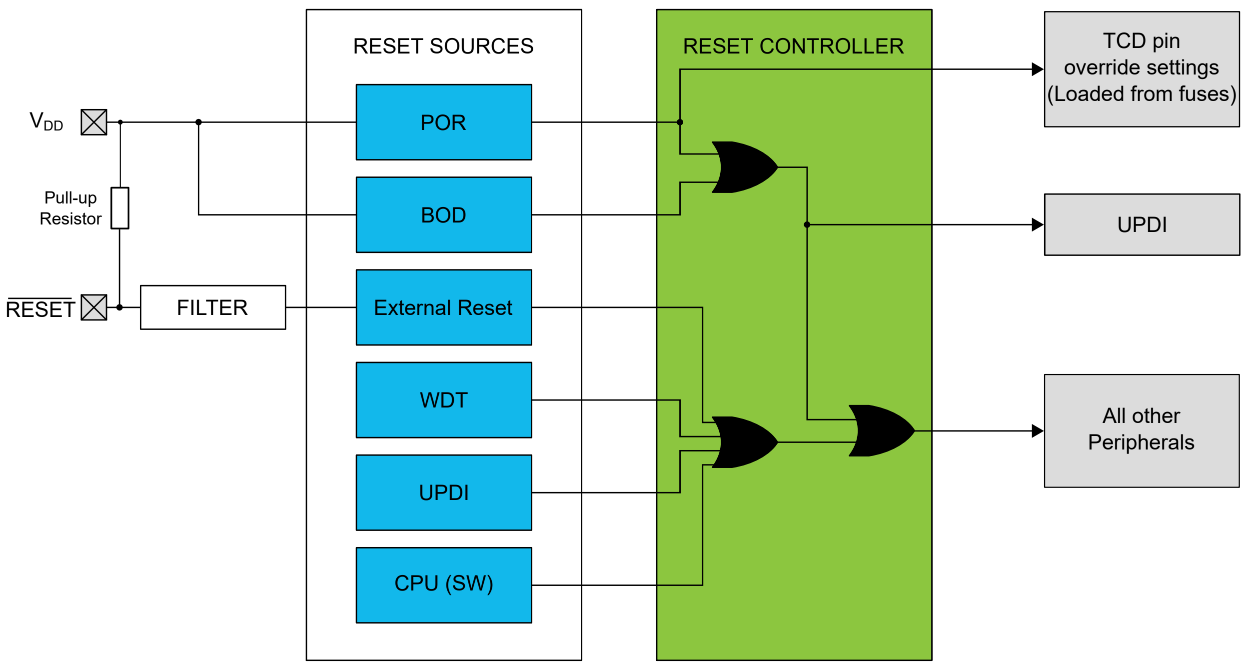
- Reset the device and set it to an initial state
- Reset Flag register for identifying the Reset source in the software
- Multiple Reset sources:
  – Power supply Reset sources: Brown-out Detect (BOD), Power-on Reset (POR)
  – User Reset sources: External Reset pin ($\overline{\text{RESET}}$), Watchdog Reset (WDT), Software Reset (SW), and UPDI Reset

12.2 Overview

The Reset Controller (RSTCTRL) manages the Reset of the device. It issues a device Reset, sets the device to its initial state, and allows the Reset source to be identified by the software.

12.2.1 Block Diagram

Figure 12-1. Reset System Overview



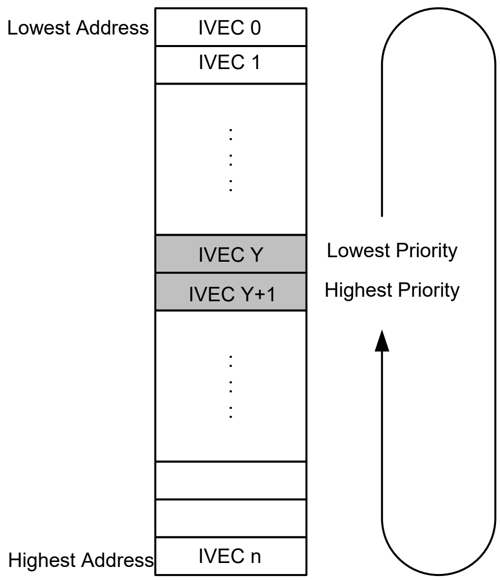
12.2.2 Signal Description

Signal	Description	Type
$\overline{\text{RESET}}$	External Reset (active-low)	Digital input

CPUINT.LVL0PRI, so that interrupt vector Y+1 has the highest priority. Note that in this case, the priorities will "wrap" so that IVEC0 has lower priority than IVECn.

Refer to the Interrupt Vector Mapping of the device for available interrupt requests and their interrupt vector number.

Figure 13-4. Static Scheduling when CPUINT.LVL0PRI is Different From Zero



Related Links

7.2 Interrupt Vector Mapping

13.3.2.5.3 Round Robin Scheduling

Static scheduling may cause starvation, i.e. some interrupts might never be serviced. To avoid this, the CPUINT offers round robin scheduling for normal priority (LVL0) interrupts. In round robin scheduling, CPUINT.LVL0PRI contains the number of the vector number in IVEC with the lowest priority. This register is automatically updated by hardware with the interrupt vector number for the last acknowledged LVL0 interrupt. This interrupt vector will, therefore, have the lowest priority next time one or more LVL0 interrupts are pending. Figure 13-5 explains the new priority ordering after IVEC Y was the last interrupt to be acknowledged, and after IVEC Y+1 was the last interrupt to be acknowledged.

Round robin scheduling for LVL0 interrupt requests is enabled by writing a ‘1’ to the Round Robin Priority Enable bit (LVL0RR) in the Control A register (CPUINT.CTRLA).

16.5.9 Input Value

Name: IN
Offset: 0x08
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
	IN[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – IN[7:0] Input Value
This register shows the value present on the pins if the digital input driver is enabled. IN[n] shows the value of pin n of the port. The input is not sampled and cannot be read if the digital input buffers are disabled.
Writing to a bit of PORT.IN will toggle the corresponding bit in PORT.OUT.

16.7.2 Output Value

Name: OUT
Offset: 0x01
Reset: 0x00
Property: -

Writing to the Virtual PORT registers has the same effect as writing to the regular registers, but allows for memory-specific instructions, such as bit-manipulation instructions, which are not valid for the extended I/O memory space where the regular PORT registers reside.

Bit	7	6	5	4	3	2	1	0
	OUT[7:0]							
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bits 7:0 – OUT[7:0] Output Value
This bit field selects the data output value for the individual pins in the port.

20.3.2 Initialization

To start using the timer/counter in a basic mode, follow these steps:

- Write a TOP value to the Period register (TCAn.PER)
- Enable the peripheral by writing a '1' to the ENABLE bit in the Control A register (TCAn.CTRLA). The counter will start counting clock ticks according to the prescaler setting in the Clock Select bit field (CLKSEL) in TCAn.CTRLA.
- Optional: By writing a '1' to the Enable Count on Event Input bit (CNTEI) in the Event Control register (TCAn.EVCTRL), event inputs are counted instead of clock ticks.
- The counter value can be read from the Counter bit field (CNT) in the Counter register (TCAn.CNT).

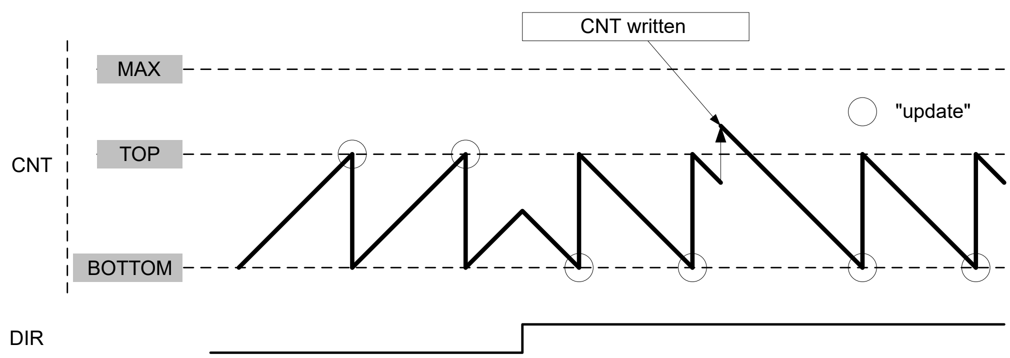
20.3.3 Operation

20.3.3.1 Normal Operation

In normal operation, the counter is counting clock ticks in the direction selected by the Direction bit (DIR) in the Control E register (TCAn.CTRLE), until it reaches TOP or BOTTOM. The clock ticks are from the peripheral clock CLK_PER, optionally prescaled, depending on the Clock Select bit field (CLKSEL) in the Control A register (TCAn.CTRLA).

When up-counting and TOP are reached, the counter will wrap to zero at the next clock tick. When down-counting, the counter is reloaded with the Period register value (TCAn.PER) when BOTTOM is reached.

Figure 20-4. Normal Operation



It is possible to change the counter value in the Counter register (TCAn.CNT) when the counter is running. The write access to TCAn.CNT has higher priority than count, clear, or reload, and will be immediate. The direction of the counter can also be changed during normal operation by writing to DIR in TCAn.CTRLE.

20.3.3.2 Double Buffering

The Period register value (TCAn.PER) and the Compare n register values (TCAn.CMPn) are all double-buffered (TCAn.PERBUF and TCAn.CMPnBUF).

Each buffer register has a Buffer Valid flag (PERBV, CMPnBV) in the Control F register (TCAn.CTRLF), which indicates that the buffer register contains a valid, i.e. new, value that can be copied into the corresponding Period or Compare register. When the Period register and Compare n registers are used for a compare operation, the BV flag is set when data is written to the buffer register and cleared on an UPDATE condition. This is shown for a Compare register (CMPn) below.

20.5.3 Control C - Normal Mode

Name: CTRLC
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
						CMP2OV	CMP1OV	CMP0OV
Access						R/W	R/W	R/W
Reset						0	0	0

Bit 2 – CMP2OV Compare Output Value 2
See CMP0OV.

Bit 1 – CMP1OV Compare Output Value 1
See CMP0OV.

Bit 0 – CMP0OV Compare Output Value 0
The CMPnOV bits allow direct access to the waveform generator's output compare value when the timer/counter is not enabled. This is used to set or clear the WG output value when the timer/counter is not running.

20.5.5 Control Register E Clear - Normal Mode

Name: CTRLECLR
Offset: 0x04
Reset: 0x00
Property: -

The individual Status bit can be cleared by writing a '1' to its bit location. This allows each bit to be cleared without the use of a read-modify-write operation on a single register.
Each Status bit can be read out either by reading TCAn.CTRLESET or TCAn.CTRLECLR.

Bit	7	6	5	4	3	2	1	0
					CMD[1:0]		LUPD	DIR
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:2 – CMD[1:0] Command
These bits are used for software control of update, restart, and reset of the timer/counter. The command bits are always read as '0'.

Value	Name	Description
0x0	NONE	No command
0x1	UPDATE	Force update
0x2	RESTART	Force restart
0x3	RESET	Force hard Reset (ignored if TC is enabled)

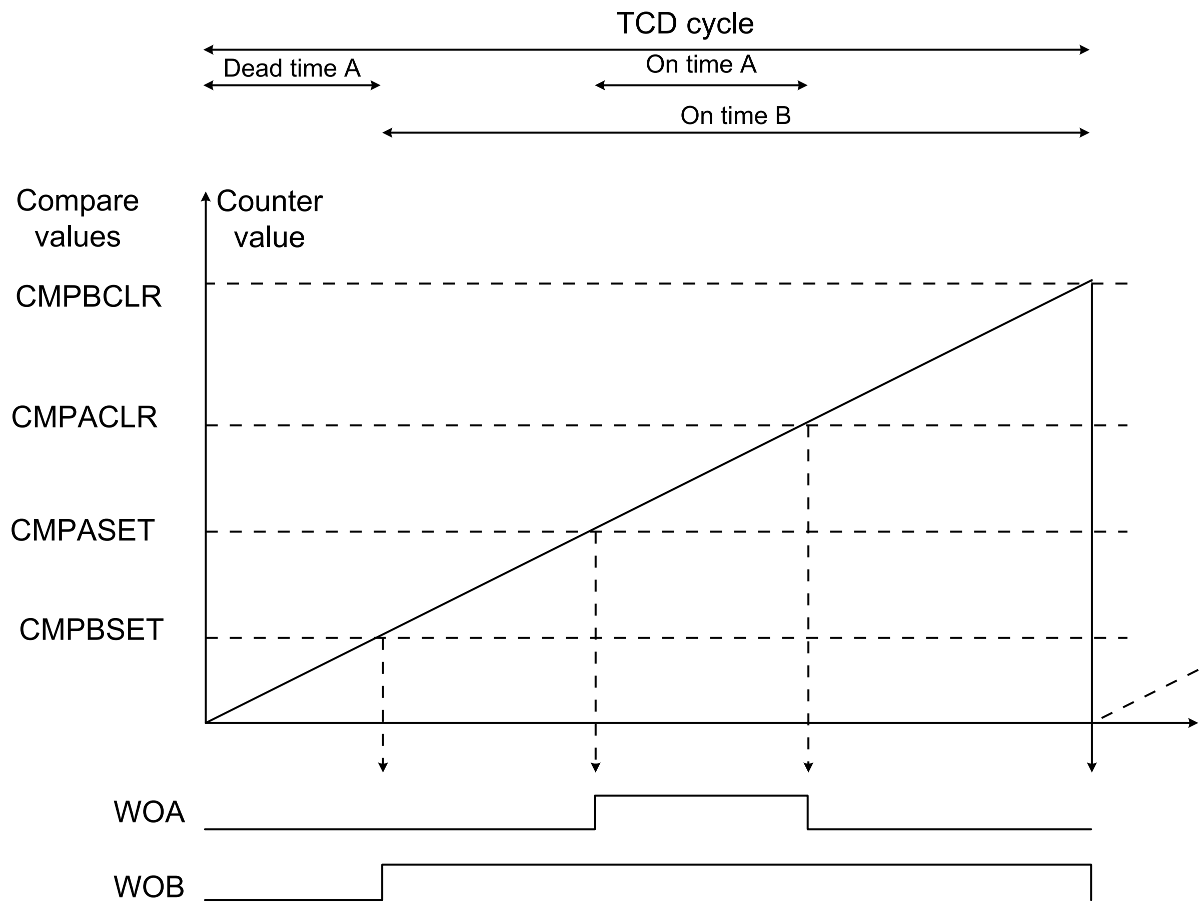
Bit 1 – LUPD Lock Update
Lock update can be used to ensure that all buffers are valid before an update is performed.

Value	Description
0	The buffered registers are updated as soon as an UPDATE condition has occurred.
1	No update of the buffered registers is performed, even though an UPDATE condition has occurred.

Bit 0 – DIR Counter Direction
Normally this bit is controlled in hardware by the Waveform Generation mode or by event actions, but this bit can also be changed from software.

Value	Description
0	The counter is counting up (incrementing)
1	The counter is counting down (decrementing)

Figure 22-4. One Ramp Mode with *CMPBSET < CMPASET*



If any of the other compare values are bigger than CMPBCLR it will never be triggered when running in One Ramp mode, and if the CMPACLR is smaller than the CMPASET value, the clear value will not have any effect.

22.3.2.3.2 Two Ramp Mode

In Two Ramp mode the TCD counter counts up until it reaches the CMPACLR value, then it Resets and counts up until it reaches the CMPBCLR value. Then, the TCD cycle is done and the counter restarts from 0x000, beginning a new TCD cycle. The TCD cycle period is given by:

$$T_{\mathrm{TCD\_cycle}} = \frac{(\mathrm{CMPACLR} + 1 + \mathrm{CMPBCLR} + 1)}{f_{\mathrm{CLK\_TCD\_CNT}}}$$

22.5.15 Dither Value

Name: DITVAL
Offset: 0x19
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
					DITHER[3:0]			
Access					R/W	R/W	R/W	R/W
Reset					0	0	0	0

Bits 3:0 – DITHER[3:0] Dither Value
These bits configure the fractional adjustment of the on-time or off-time according to Dither Selection bits (DITHERSEL) in the Dither Control register (TCDn.DITCTRL). The DITHER value is added to a 4-bit accumulator at the end of each TCD cycle. When the accumulator overflows the frequency adjustment will occur.

The DITHER bits are double-buffered so the new value is copied in at an update condition.

USARTn.DATA are moved from the transmit buffer to the Shift register when the Shift register is ready to send a new frame.

The transmitter and receiver interrupt flags and corresponding USART interrupts used in Master SPI mode are identical in function to their use in normal USART operation. The receiver error status flags are not in use and are always read as zero.

Disabling of the USART transmitter or receiver in Master SPI mode is identical to their disabling in normal USART operation.

Related Links

24.5.9 CTRLC

24.3.2.5.1 USART SPI vs. SPI

The USART in Master SPI mode is fully compatible with the stand-alone SPI module in that:

- Timing diagrams are the same
- UCPHA bit functionality is identical to that of the SPI CPHA bit
- UDORD bit functionality is identical to that of the SPI DORD bit

When the USART is set in Master SPI mode, configuration and use are in some cases different from those of the stand-alone SPI module. In addition, the following difference exists:

- The USART in Master SPI mode does not include the SPI Write Collision feature

The USART in Master SPI mode does not include the SPI Double-Speed mode feature, but this can be achieved by configuring the Baud Rate Generator accordingly:

- Interrupt timing is not compatible
- Pin control differs due to the master-only operation of the USART in SPI Master mode

A comparison of the USART in Master SPI mode and the SPI pins is shown in Table 24-8.

Table 24-8. Comparison of USART in Master SPI Mode and SPI Pins

USART	SPI	Comment
TxD	MOSI	Master out only
RxD	MISO	Master in only
XCK	SCK	Functionally identical
-	SS	Not supported by USART in Master SPI mode

Related Links

24.5.9 CTRLC

24.3.2.6 RS-485 Mode of Operation

The RS-485 feature enables the support of external components to comply with the RS-485 standard.

Either an external line driver is supported as shown in the figure below (RS485=0x1 in USARTn.CTRLA), or control of the transmitter driving the TxD pin is provided (RS485=0x2).

While operating in RS-485 mode, the Transmit Direction pin (XDIR) is driven high when the transmitter is active.

26.4 Register Summary - TWI

Offset	Name	Bit Pos.								
0x00	CTRLA	7:0				SDASETUP	SDAHOLD[1:0]		FMPEN	
0x01	Reserved									
0x02	DBGCTRL	7:0								DBGRUN
0x03	MCTRLA	7:0	RIEN	WIEN		QCEN	TIMEOUT[1:0]		SMEN	ENABLE
0x04	MCTRLB	7:0					FLUSH	ACKACT	MCMD[1:0]	
0x05	MSTATUS	7:0	RIF	WIF	CLKHOLD	RXACK	ARBLOST	BUSERR	BUSSTATE[1:0]	
0x06	MBAUD	7:0	BAUD[7:0]							
0x07	MADDR	7:0	ADDR[7:0]							
0x08	MDATA	7:0	DATA[7:0]							
0x09	SCTRLA	7:0	DIEN	APIEN	PIEN			PMEN	SMEN	ENABLE
0x0A	SCTRLB	7:0						ACKACT	SCMD[1:0]	
0x0B	SSTATUS	7:0	DIF	APIF	CLKHOLD	RXACK	COLL	BUSERR	DIR	AP
0x0C	SADDR	7:0	ADDR[7:0]							
0x0D	SDATA	7:0	DATA[7:0]							
0x0E	SADDRMASK	7:0	ADDRMASK[6:0]							ADDREN

26.5 Register Description

Both TWI Master Interrupt Flags are cleared automatically if this register is read while ACKACT is set to either ACK or NACK. However, arbitration lost and bus error flags are left unchanged.

30.5.3 Control C

Name: CTRLC
Offset: 0x02
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
		SAMPCAP	REFSEL[1:0]			PRESC[2:0]		
Access	R	R/W	R/W	R/W	R	R/W	R/W	R/W
Reset	0	0	0	0	0	0	0	0

Bit 6 – SAMPCAP Sample Capacitance Selection
This bit selects the sample capacitance, and hence, the input impedance. The best value is dependent on the reference voltage and the application's electrical properties.

Value	Description
0	Recommended for reference voltage values below 1V.
1	Reduced size of sampling capacitance. Recommended for higher reference voltages.

Bits 5:4 – REFSEL[1:0] Reference Selection
These bits select the voltage reference for the ADC.

Note: Do not force the internal reference enabled (ADCnREFEN=1 in VREF.CTRLB) when the ADC is using the external reference (REFSEL bits in ADC.CTRLC).

Value	Name	Description
0x0	INTERNAL	Internal reference
0x1	VDD	V_{DD}
0x2	VREFA	External reference V_{REFA}
Other	-	Reserved.

Bits 2:0 – PRESC[2:0] Prescaler
These bits define the division factor from the peripheral clock (CLK_PER) to the ADC clock (CLK_ADC).

Value	Name	Description
0x0	DIV2	CLK_PER divided by 2
0x1	DIV4	CLK_PER divided by 4
0x2	DIV8	CLK_PER divided by 8
0x3	DIV16	CLK_PER divided by 16
0x4	DIV32	CLK_PER divided by 32
0x5	DIV64	CLK_PER divided by 64
0x6	DIV128	CLK_PER divided by 128
0x7	DIV256	CLK_PER divided by 256

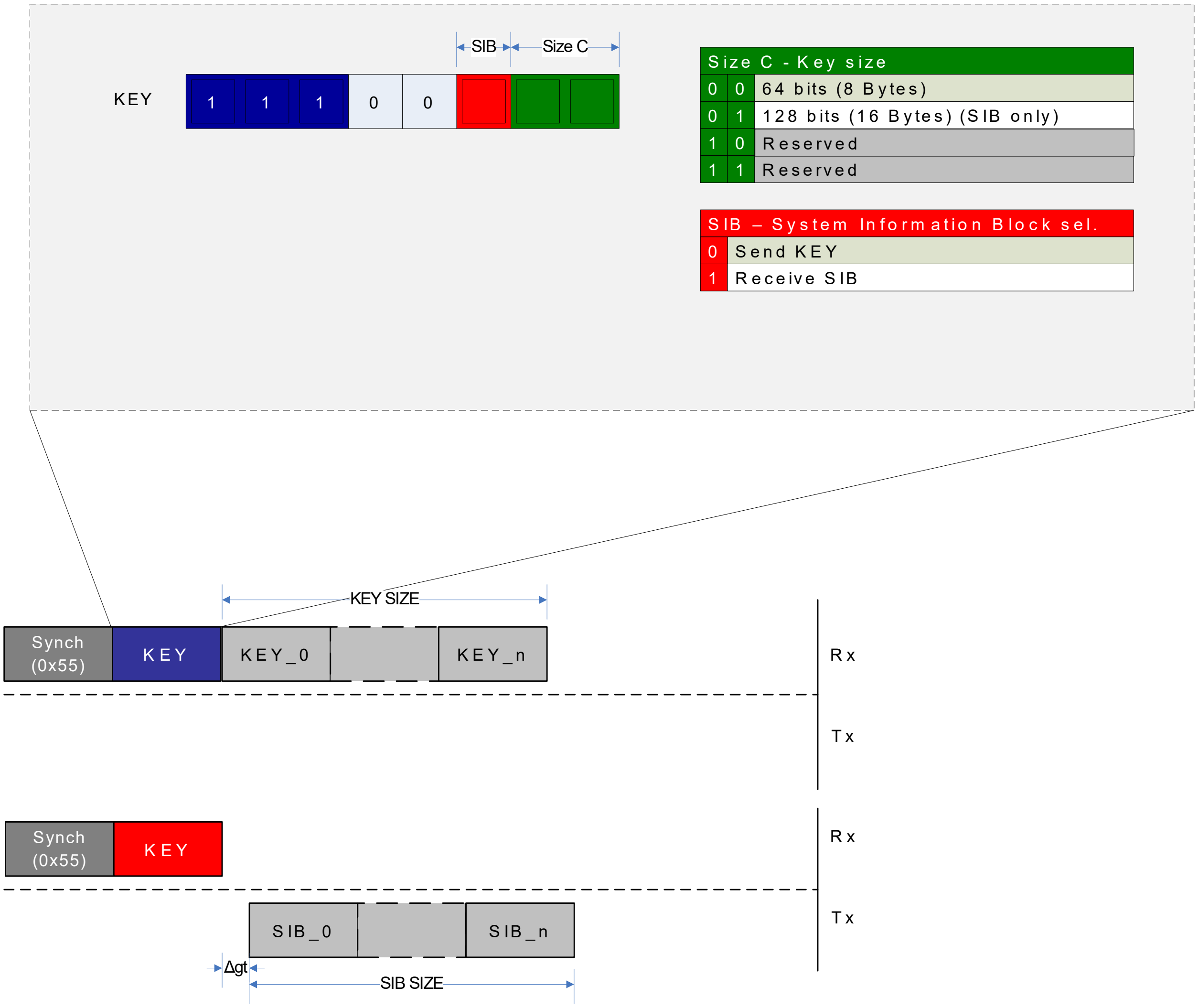
30.5.9 Event Control

Name: EVCTRL
Offset: 0x09
Reset: 0x00
Property: -

Bit	7	6	5	4	3	2	1	0
								STARTEI
Access								R/W
Reset								0

Bit 0 – STARTEI Start Event Input
This bit enables using the event input as trigger for starting a conversion.

Figure 33-16. KEY Instruction Operation



The figure above shows the transmission of a KEY and the reception of a SIB. In both cases, the `SIZE_C` field in the opcode determines the number of frames being sent or received. There is no response after sending a `KEY` to the UPDI. When requesting the SIB, data will be transmitted from the UPDI according to the current Guard Time setting.

33.3.4 System Clock Measurement with UPDI

It is possible to use the UPDI to get an accurate measurement of the system clock frequency, by using the UPDI event connected to TCB with Input Capture capabilities. A recommended setup flow for this feature is given by the following steps:

- Set up TCBn.CTRLB with setting CNTMODE=0x3, Input Capture Frequency Measurement mode.
- Write CAPTEI=1 in TCBn.EVCTRL to enable Event Interrupt. Keep EDGE = 0 in TCBn.EVCTRL.
- Configure the Event System as described in 33.3.8 Events.
- For the SYNCH character used to generate the UPDI events, it is recommended to use a slow baud rate in the range of 10 kbps - 50 kbps to get a more accurate measurement on the value captured by the timer between each UPDI event. One particular thing is that if the capture is set up to trigger an interrupt, the first captured value should be ignored. The second captured value based

35. Conventions

35.1 Numerical Notation

Table 35-1. Numerical Notation

Symbol	Description
165	Decimal number
0b0101	Binary number (example 0b0101 = 5 decimal)
'0101'	Binary numbers are given without prefix if unambiguous
0x3B24	Hexadecimal number
X	Represents an unknown or do not care value
Z	Represents a high-impedance (floating) state for either a signal or a bus

35.2 Memory Size and Type

Table 35-2. Memory Size and Bit Rate

Symbol	Description
KB	kilobyte (2^{10} = 1024)
MB	megabyte (2^{20} = 1024*1024)
GB	gigabyte (2^{30} = 1024*1024*1024)
b	bit (binary '0' or '1')
B	byte (8 bits)
1 kbit/s	1,000 bit/s rate (not 1,024 bit/s)
1 Mbit/s	1,000,000 bit/s rate
1 Gbit/s	1,000,000,000 bit/s rate
word	16-bit

35.3 Frequency and Time

Table 35-3. Frequency and Time

Symbol	Description
kHz	1 kHz = 10^3 Hz = 1,000 Hz
KHz	1 KHz = 1,024 Hz, 32 KHz = 32,768 Hz
MHz	1 MHz = 10^6 Hz = 1,000,000 Hz

Table 37-14. Internal Oscillator (OSC20M) Characteristics

Symbol	Description	Condition		Min.	Typ.	Max.	Unit
f_{OSC20M}	Accuracy with 16 MHz and 20 MHz frequency selection relative to the factory-stored frequency value	Factory calibrated V_{DD}=3V(1)	T=[0, 70]°C, V_{DD}=[1.8, 4.5]V(3)	-2.0	-	2.0	%
		Factory calibrated V_{DD}=5V(1)	T=[0, 70]°C, V_{DD}=[4.5, 5.5]V(3)	-2.0	-	2.0	
	Accuracy with 16 MHz and 20 MHz frequency selection	Factory calibrated	T=25°C, 3.0V	-3.0	-	3.0	%
			T=[0, 70]°C, V_{DD}=[1.8, 3.6]V(3)	-4.0	-	4.0	
			Full operation range(3)	-5.0	-	5.0	
f_{CAL}	User calibration range	OSC20M(2) = 16 MHz		14.5	-	17.5	MHz
		OSC20M(2) = 20 MHz		18.5	-	21.5	
%CAL	Calibration step size			-	1.5	-	%
DC	Duty cycle			-	50	-	%
T_{start}	Start-up time	Within 2% accuracy		-	8	-	µs

Note:
1. See the description of OSC20M on calibration.
2. Oscillator frequencies above speed specification must be divided so that CPU clock always is within specification.
3. These values are based on characterization and not covered by production test limits.

Table 37-15. 32.768 kHz Internal Oscillator (OSCULP32K) Characteristics

Symbol	Description	Condition	Condition	Min.	Typ.	Max.	Unit
$f_{OSCULP32K}$	Accuracy	Factory calibrated	T=25°C, 3.0V	-3	-	3	%
			T=[0, 70]°C, V_{DD}=[1.8, 3.6]V(1)	-10	-	10	
			Full operation range(1)	-30	-	30	
DC	Duty cycle			-	50	-	%
T_{start}	Start-up time			-	250	-	µs

Note:
1. These values are based on characterization and not covered by production test limits.