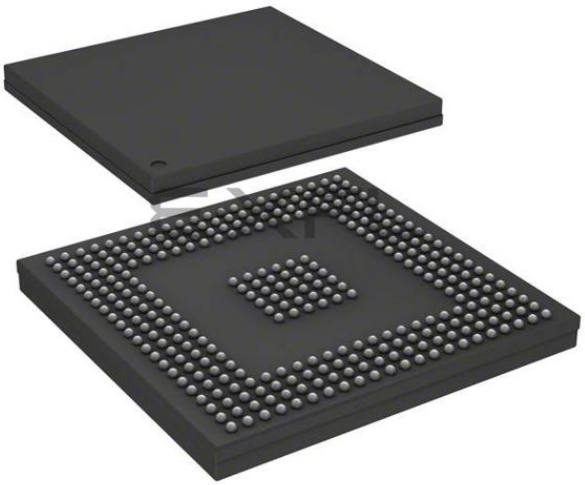

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a74b4cfar

GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

1.5.8 Flash memory

The SPC564A80 provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128- and 256-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support

12	13	14	15	16	17	18	19	20	21	22	
AN27	AN28	AN35	VSSA1	AN12_ SDS	MDO11_ ETPUA29_O	MDO10_ ETPUA27_O	MDO8_ ETPUA21_O	VDD	VRC33	VSS	A
AN26	AN31	AN32	VSSA1	AN13_ SDO	MDO9_ ETPUA25_O	MDO7_ ETPUA19_O	MDO4_ ETPUA2_O	MDO0	VSS	NIC(1),(2)	B
AN25	AN30	AN33	VDDA1	AN14_ SDI	MDO5_ ETPUA4_O	MDO2	MDO1	VSS	NIC(1),(2)	VDD	C
AN24	AN29	AN34	VDDEH7	AN15_ FCK	MDO6_ ETPUA13_O	MDO3	VSS	NIC(1),(2)	TCK	TDI	D
							NIC(1),(2)	TMS	TDO	NIC(1)	E
							NIC(1),(2)	JCOMP	EVTI	EVTO	F
							RDY	MCKO	MSEO0	MSEO1	G
							VDDEH6AB	GPIO203	GPIO204	DSPI_B_ SIN	H
VSS	VSS	NIC(1),(2)					DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ PCS0	DSPI_B_ PCS1	J
VSS	VSS	VSS					GPIO99	DSPI_B_ PCS4	DSPI_B_ SCK	DSPI_B_ PCS2	K
VSS	VSS	VSS					DSPI_B_ PCS5	DSPI_A_ SOUT	DSPI_A_ SIN	DSPI_A_ SCK	L

1. Pins marked “NIC” have no internal connection.
2. Balls B22, C21, D20, E19, F19 and J14 are shorted together inside the package.

Figure 6. 324-pin PBGA package ballmap (northeast, viewed from above)

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	T3
ADDR13 $\overline{WE}$[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U3
ADDR14 $\overline{WE}$[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U4
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	V3
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P1
ADDR17 $\overline{FR\_A\_TX\_EN}$ DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P2
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 $\overline{FR\_B\_TX\_EN}$ DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	37	H4	F4
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	36	J2	G2
ETPUA20 $\overline{\text{IRQ}}$[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B Flexray TX data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	35	J1	G1
ETPUA21 $\overline{\text{IRQ}}$[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C Flexray RX channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	34	G4	E4
ETPUA22 $\overline{\text{IRQ}}$[10] ETPUA17_O[8] GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	32	H2	F2
ETPUA23 $\overline{\text{IRQ}}$[11] ETPUA21_O[8] $\overline{\text{FR\_A\_TX\_EN}}$ GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) Flexray ch. A TX enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	30	H1	F1

Table 5. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV(1),(2)	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1. Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.
2. VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 6. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	SPC564A80 clock output for the external/calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode. On the 324BGA package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with previous devices . For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected. 1: XTAL oscillator mode is selected For the 324 ball BGA package: If RSTCFG is 0: 0: External reference clock is selected. 1: XTAL oscillator mode is selected. If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS- DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS- DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission

Table 6. Signal details (continued)

Signal	Module or Function	Description
BOOTCFG[0:1]	SIU - Configuration	Two BOOTCFG signals are implemented in SPC564A80 MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode See the *SPC564A80 Microcontroller Reference Manual* for more information. The following values are for BOOTCFG[0:1}: 00:Boot from internal flash memory 01:FlexCAN/eSCI boot 10:Boot from external memory using EBI 11:Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU - Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled 4 clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0:Weak pulldown applied to eTPU and eMIOS pins at reset 1:Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx

board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International

3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 15. PMC Operating Conditions and External Regulators Supply Voltage

ID	Name			Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage V_{DDREG}	4.75	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)(1)	1.26(2)	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum required DC output current	445	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)(3)	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1. An internal regulator controller can be used to regulate core supply.
2. The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.
3. An internal regulator can be used to regulate 3.3 V supply.

Table 16. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm/°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm/V	

Table 16. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
9	Por5V_r	CC	C	Nominal POR for rising 5 V V_{DDREG} supply	—	2.67	—	V	
9a	—	CC	C	Variation of POR for rising 5 V V_{DDREG} supply	Por5V_r - 35%	Por5V_r	Por5V_r + 50%	V	
9b	Por5V_f	CC	C	Nominal POR for falling 5 V V_{DDREG} supply	—	2.47	—	V	
9c	—	CC	C	Variation of POR for falling 5 V V_{DDREG} supply	Por5V_f - 35%	Por5V_f	Por5V_f + 50%	V	

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal Vdd regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum Vdd DC target respectively.
5. Minimum loading (<10 mA) for reading trim values from flash, powering internal RC oscillator, and IO consumption during POR.
6. No external load is allowed, except for use as a reference for an external tool.
7. This value is valid only when the internal regulator is bypassed. When the internal regulator is enabled, the maximum external load allowed on the Nexus pads is 30 pF at 40 MHz.
8. Lvi3p3 tracks DC target variation of internal Vdd33 regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum Vdd33 DC target respectively.

3.6.1 Regulator Example

In designs where the SPC564A80 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

3.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200 – 600(1)	mV
V_{BE}	Base-to-emitter voltage	0.4 – 1.0	V

1. Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}.

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes the state of the I/O pins during power up/down varies according to *Table 19* for all pins with fast pads, and *Table 20* for all pins with medium, slow, and multi-voltage pads.

Table 19. Power sequence pin states (fast pads)

V_{DDE}	V_{RC33}	V_{DD}	Pad State
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 20. Power sequence pin states (medium, slow, and multi-voltage pads)

V_{DDEH}	V_{DD}	Pad State
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H) (continued)

Symbol		C	Parameter		Conditions	Value		Unit
						min	max	
C_{JITTER}	CC	T	CLKOUT period jitter[6],[7],[8],[9]	Peak-to-peak (clock edge to clock edge)	f_{SYS} maximum	–5	5	% f_{CLKOUT}
		T		Long-term jitter (avg. over 2 ms interval)		–6	6	ns
t_{cst}	CC	T	Crystal start-up time [10], [11]		—	—	10	ms
V_{IHEXT}	CC	T	EXTAL input high voltage		Crystal Mode[12]	Vxtal + 0.4	—	V
		T			External Reference[12], [13]	V_{RC33} /2 + 0.4	V_{RC33}	
V_{ILEXT}	CC	T	EXTAL input low voltage		Crystal Mode[12]	—	Vxtal - 0.4	V
		T			External Reference[12], [13]	0	V_{RC33} /2 - 0.4	
—	CC	T	XTAL load capacitance[10]		4 MHz	5	30	pF
					8 MHz	5	26	
					12 MHz	5	23	
					16 MHz	5	19	
					20 MHz	5	16	
					40 MHz	5	8	
t_{lpll}	CC	P	PLL lock time [10], [14]		—	—	200	µs
t_{dc}	CC	T	Duty cycle of reference		—	40	60	%
f_{LCK}	CC	T	Frequency LOCK range		—	–6	6	% f_{sys}
f_{UL}	CC	T	Frequency un-LOCK range		—	–18	18	% f_{sys}
f_{CS} f_{DS}	CC	D	Modulation Depth		Center spread	±0.25	±4.0	% f_{sys}
		D			Down Spread	–0.5	–8.0	
f_{MOD}	CC	D	Modulation frequency[15]		—	—	100	kHz

1. Considering operation with PLL not bypassed.
2. All internal registers retain data at 0 Hz.
3. “Loss of Reference Frequency” window is the reference frequency range outside of which the PLL is in self clocked mode.
4. Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls outside the f_{LOR} window.

5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. Proper PC board layout procedures must be followed to achieve specifications.
12. This parameter is guaranteed by design rather than 100% tested.
13. V_{IHEXT} cannot exceed V_{RC33} in external reference mode.
14. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
15. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.11 Temperature sensor electrical characteristics

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range		–40	—	150	°C
—	CC	C	Sensitivity		—	6.3	—	mV/°C
—	CC	P	Accuracy	T_J = –40 to 150 °C	–10	—	10	°C

3.12 eQADC electrical characteristics

Table 28. eQADC conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	MHz
CC	CC	D	Conversion cycles	2+13	128+14	ADCLK cycles
T_{SR}	CC	C	Stop mode recovery time(1)	—	10	µs
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	mV

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)(1)

Name		C	Output Delay (ns)(2),(3) Low-to-High / High-to-Low		Rise/Fall Edge (ns)(3),(4)		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5),(6),(7)	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11(8)
	N/A							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7),(10)	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11(8)
	N/A							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	N/A							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	N/A							
pad_i_hv(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
7. Output delay is shown in *Figure 9: Pad output delay*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
11. Selectable high/low swing IO pad with selectable slew in high swing mode only.
12. Fast pads are 3.3 V pads.
13. Stand alone input buffer. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications (V_{DDE} = 3.3 V)[1]

Pad Type		C	Output Delay (ns)[2],[3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3],[4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5],[6],[7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7],[10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7],[11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							
Fast	CC	D		2.5/2.5		1.2/1.2	10	00
	CC	D		2.5/2.5		1.2/1.2	20	01
	CC	D		2.5/2.5		1.2/1.2	30	10
	CC	D		2.5/2.5		1.2/1.2	50	11[8]
pad_i_hv[12]	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.

3.17.9 eQADC SSI timing

Table 49. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency (2), (3)	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	-7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	-7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1. SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
3. FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

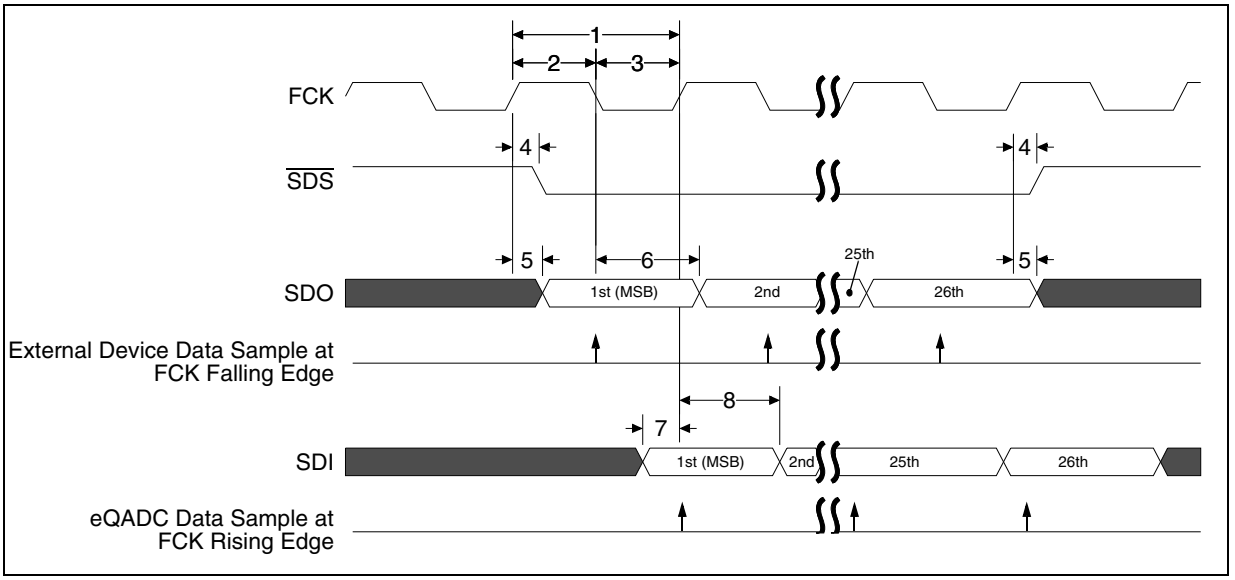

Figure 32. eQADC SSI timing

Table 53. LBGA208 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	16.80	17.00	17.20	0.6614	0.6693	0.6772
D1		15.00			0.5906	
E	16.80	17.00	17.20	0.6614	0.6693	0.6772
E1		15.00			0.5906	
e		1.00			0.0394	
F		1.00			0.0394	
ddd			0.20			0.0079
eee[4]			0.25			0.0098
fff[5]			0.10			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   —Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   —The maximum total package height is calculated by the following methodology:
   A2 Typ+A1 Typ +√ ($A1^2$+$A3^2$+$A4^2$ tolerance values)
   — Low profile: 1.20mm < A ≤ 1.70mm
3. The typical ball diameter before mounting is 0.60mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

4.2.3 PBGA324

Table 56. Revision history (continued)

Date	Revision	Changes
09-Dec-2009	2	– C4 is VDD (was VDDEH1A) – C15 is VDDA (was VDDA0) – C16 is AN14_SDI (was AN14) – C17 is MDO5_ETPUA4O (was MDO5) – C21 is NIC1 (was VDDE7) – D15 is VDDEH7 (was VDDEH9) – D16 is AN15_FCK (was AN15) – D17 is MDO6_ETPUA13O (was MDO6) – D20 is NIC (was VDDE7) – E19 is NIC (was VDDE7) – E22 is NIC (was NC) – F19 is NIC (was VDDE7) – H4 is VDDEH1AB (was VDDEH1A) – H19 is VDDEH6AB (was VDDEH10) – J14 is NIC (was VDDE7) – K19 is GPIO99 (was PCSA3) – M9 is VDDE2 (was VDD2) – M21 is GPIO98 (was PCSA2) – M22 is VDDREG (was NC) – N22 is NIC (was NC) – P2 is ADDR17 (was ADD17) – P4 is VRC33 (was VDD33) – R3 is VDDE-EH (was VDDE2) – T21 is VSS (was VRCVSS) – T22 is VSS (was VSSPLL) – U19 is VDDEH6AB (was VDDEH6A) – W2 is VDDE-EH (was VDDE2) – W7 is VRC33 (was VDD33) – W14 is VDDEH4AB (was VDDEH4B) – W21 is NIC (was VRC33) – Y22 is VRC33 (was VDD33) – AB22 is VSS (was VSSPLL) Recommended operating characteristics for power transistor updated Pad current specifications updated LVDS pad specifications updated. SRC does not apply to common mode voltage. Temperature sensor electrical characteristics added eQADC electrical characteristics updated with VGA gain specs Pad AC specifications updated Definition for RDY signal added to signal details V_{STBY} maximum is 5.5 V (was listed incorrectly as 6.0 V) I_{MAXA} maximum is 5 mA (was TBD) Analog differential input functions added to AN0–AN7 in signal summary

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010 (cont)	3 (cont)	Added information to AC timings section: – New section added: Reset and configuration pin timing – New section added: External interrupt timing (IRQ pin) – New section added: eTPU timing – Added Nexus debug port operating frequency table to Nexus timings section – Added external bus interface maximum operating frequency table and calibration bus interface maximum operation frequency table – Added FlexCAN system clock source section Changes to Power management control (PMC) and power on reset (POR) electrical specifications: – Max value for parameter 2 (vddreg) is 5.25 V (was 5.5 V) Updated “Core voltage regulator controller external components preferred configuration” diagram. Changes to DC electrical specifications table: – Slew rate on power supply pins (system requirement) changed to 25 V/ms (was 50 V/ms) Throughout the document the maximum frequency is now 150 MHz (was 145 MHz) Changes to DC electrical specifications: – Parameter classifications added – V_{DDREG} max value changed to 5.25 V (was 5.5 V) – V_{OH_LS} min value changed to 2.0 V (was 2.7 V) with a load current of 0.5 mA – V_{OL_LS} max value changed to 0.6 V (was 0.2*V_{DDEH}) with load current of 2 mA – V_{INDC} min value changed to V_{SSA}-0.3 (was V_{SSA}-1.0) – V_{INDC} max value changed to V_{DDA}+0.3 (was V_{DDA}+1.0) Added new section: Configuring SRAM wait states – VRCCTL external circuit updated.
01-Oct-2010	4	Updates to Nexus timings: – t_{MDOV} max value changed to 0.35 (was 0.2) – t_{MSEOV} max value changed to 0.35 (was 0.2) – t_{EVTOV} max value changed to 0.35 (was 0.2) Updates to DC electrical specifications: – V_{STBY} min value changed to 0.95 V (was 0.9 V) – V_{STBY} has two ranges—for regulated mode and unregulated mode Correction to PLLMRFM electrical specifications: – V_{DDPLL} range is from 1.08 V to 3.6 V (was 3.0 V to 3.6 V. Updates to pad AC specifications: – Specs with drive load = 200 pF deleted. DSC (drive strength control) values range from 10 – 50 pF. – I/O pad average I_{DDE} specifications updated (fast pad specs only) – I/O pad V_{RC33} average I_{DDE} specifications (fast pad specs only) Updates to Reset and configuration pin timings: – Footnote added: $\overline{\text{RESET}}$ pulse width is measured from 50% of the falling edge to 50% of the rising edge. – Timings are specified at V_{DD} = 1.14 V to 1.32 V (was 1.08 V to 1.32 V).

Table 56. Revision history (continued)

Date	Revision	Changes
10-Feb-2011 (cont)	5 (cont)	– Added DATA[0:15] to V_{DDE5} in the “signal properties” table. – Updated VSTBY parameters in the “Power/ground segmentation” table. – Updated the parameter symbols and classifications throughout the document. – Updated footnote instances in the “Absolute maximum ratings“ table. – Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. – Updated the format of the “EMI (electromagnetic interference) characteristics” table. – Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications“ table. – Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. – Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. – Removed the “VRC electrical specifications” table as it contained redundant information. – Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. – Updated V_{IH_LS} in the “DC electrical specifications” table. – Updated the V_{OH_LS} min value in the “DC electrical specifications” table. – Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. – Updated the I_{DDA}/I_{REF}/I_{DDREG} max value in the “DC electrical specifications” table. – Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. – Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. – Updated values for V_{OD} in the “DSPI LVDS pad specification“ table. – Removed the footnotes from the “DSPI LVDS pad specifications“ table. – Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. – Updated footnotes in the “PLLMRFM electrical specifications” table. – Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)“ table. – Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. – Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. – Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Updated the Typical values for $T_{dwprogram}$,, $T_{pprogram}$, and $T_{16kpperase}$, and updated the Initial Max values for $T_{128kpperase}$ and $T_{256kpperase}$ in the “Flash program and erase specifications” table. – Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. – Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)“ table.