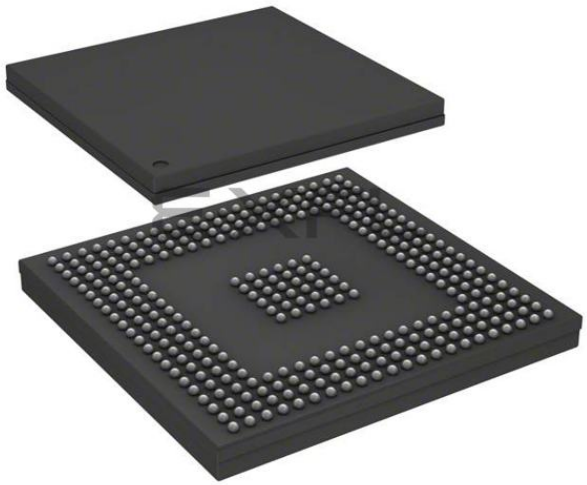

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a74b4cfay

1.5 Feature details

1.5.1 e200z4 core

SPC564A80 devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New ‘Wait for Interrupt’ instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.5.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
  - External Bus Interface

- 4 slave ports
  - Flash
  - Calibration and EBI bus
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By

GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

1.5.8 Flash memory

The SPC564A80 provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128- and 256-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support

  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.12 Reaction module

The reaction module provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The reaction module has the following features:

- Six reaction channels
- Each channel output is a bus of three signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions

1.5.13 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features

1.5.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

1.5.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the SPC564A80 Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

1.5.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

1.5.27 Development Trigger Semaphore (DTS)

SPC564A80 devices include a system development feature, the Development Trigger Semaphore (DTS) module, that enables software to signal an external tool by driving a persistent (affected only by reset or an external tool) signal on an external device pin. There

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	T3
ADDR13 $\overline{WE}$[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U3
ADDR14 $\overline{WE}$[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U4
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	V3
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P1
ADDR17 $\overline{FR\_A\_TX\_EN}$ DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P2
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 $\overline{FR\_B\_TX\_EN}$ DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration read/write enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[0]/$\overline{BE}$[0]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[1]/$\overline{BE}$[1]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A	01 10	343	O O	VDDE12 Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[7] / —	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_MDO[8]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[8] / —	—	—	—
CAL_MDO[9]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[9] / —	—	—	—
CAL_MDO[10]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[10] / —	—	—	—
CAL_MDO[11]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[11] / —	—	—	—
NEXUS											
$\overline{\text{EVTI}}$	Nexus event in	P	01	231	I	VDDEH7 MultiV[12],[14]	— / Up	$\overline{\text{EVTI}}$ / Up	116	E15	F21
$\overline{\text{EVTO}}$	Nexus event out	P	01	227	O	VDDEH7 MultiV[12],[14], [15]	—	$\overline{\text{EVTO}}$ / —	120	D15	F22
MCKO	Nexus message clock out	P	—	219[11]	O	VRC33 Fast	—	MCKO / —	14	F15	G20
MDO0[16]	Nexus message data out	P	01	220	O	VRC33 Fast	—	MDO[0] / —	17	A14	B20
MDO1[16]	Nexus message data out	P	01	221	O	VRC33 Fast	—	MDO[1] / —	18	B14	C19
MDO2[16]	Nexus message data out	P	01	222	O	VRC33 Fast	—	MDO[2] / —	19	A13	C18
MDO3[16]	Nexus message data out	P	01	223	O	VRC33 Fast	—	MDO[3] / —	20	B13	D18
MDO4[16] ETPUA2_O[8] GPIO[75]	Nexus message data out eTPU A channel (output only) GPIO	P A1 G	01 10 00	75	O O I/O	VDDEH7 MultiV[12],[14]	—	— / —	126	P10	B19

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
T_J	SR	Maximum operating temperature range - die junction temperature		–40.0	150.0	°C
T_{STG}	SR	Storage temperature range		–55.0	150.0	°C
T_{SDR}	SR	Maximum solder temperature(13)		—	260.0	°C
MSL	SR	Moisture sensitivity level(14)		—	3	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V +10%.
3. The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.
4. Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%.
5. Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V +10%.
6. All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.
7. AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).
8. Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.
9. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.
10. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.
11. Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
12. Total injection current for all analog input pins must not exceed 15 mA.
13. Solder profile per IPC/JEDEC J-STD-020D.
14. Moisture sensitivity per JEDEC test method A112.

3.3 Thermal characteristics

Table 10. Thermal characteristics for 176-pin QFP(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board(3)		20	°C/W

Table 10. Thermal characteristics for 176-pin QFP(1) (continued)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JCtop}$	CC	D	Junction-to-Case(4)		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin LBGA(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2),(3)	One layer board - 1s	39	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2),(4)	Four layer board - 2s2p	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2),(4)	at 200 ft./min., one layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2),(4)	at 200 ft./min., four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(5)	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case(6)		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection(7)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200 – 600(1)	mV
V_{BE}	Base-to-emitter voltage	0.4 – 1.0	V

1. Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}.

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes the state of the I/O pins during power up/down varies according to *Table 19* for all pins with fast pads, and *Table 20* for all pins with medium, slow, and multi-voltage pads.

Table 19. Power sequence pin states (fast pads)

V_{DDE}	V_{RC33}	V_{DD}	Pad State
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 20. Power sequence pin states (medium, slow, and multi-voltage pads)

V_{DDEH}	V_{DD}	Pad State
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

Table 29. eQADC single ended conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
OFFNC	CC	C	Offset error without calibration	0	160	Counts
OFFWC	CC	C	Offset error with calibration	–4	4	Counts
GAINNC	CC	C	Full scale gain error without calibration	–160	0	Counts
GAINWC	CC	C	Full scale gain error with calibration	–4	4	Counts
I_{INJ}	CC	T	Disruptive input injection current (1), (2), (3), (4)	–3	3	mA
E_{INJ}	CC	T	Incremental error due to injection current(5),(6)	–4	4	Counts
TUE8	CC	C	Total unadjusted error (TUE) at 8 MHz	–4	4(6)	Counts
TUE16	CC	C	Total unadjusted error at 16 MHz	–8	8	Counts

1. Below disruptive current conditions, the channel being stressed has conversion values of 0x3FF for analog inputs greater then V_{RH} and 0x0 for values less then V_{RL}. Other channels are not affected by non-disruptive conditions.
2. Exceeding limit may cause conversion error on stressed channels and on unstressed channels. Transitions within the limit do not affect device reliability or cause permanent damage.
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values using $V_{POSCLAMP} = V_{DDA} + 0.5$ V and $V_{NEGCLAMP} = – 0.3$ V, then use the larger of the calculated values.
4. Condition applies to two adjacent pins at injection limits.
5. Performance expected with production silicon.
6. All channels have same 10 kΩ < Rs < 100 kΩ; Channel under test has Rs=10 kΩ; I_{INJ}=I_{INJMAX},I_{INJMIN}

Table 30. eQADC differential ended conversion specifications (operating)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA1 (1)	CC	–	Variable gain amplifier accuracy (gain=1)(2)				
	CC	C	INL	8 MHz ADC	–4	4	Counts(3)
	CC	C		16 MHz ADC	–8	8	Counts
	CC	C	DNL	8 MHz ADC	–3(4)	3(4)	Counts
	CC	C		16 MHz ADC	–3(4)	3(4)	Counts

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)(1)

Name		C	Output Delay (ns)(2),(3) Low-to-High / High-to-Low		Rise/Fall Edge (ns)(3),(4)		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5),(6),(7)	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11(8)
	N/A							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7),(10)	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11(8)
	N/A							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	N/A							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	N/A							
pad_i_hv(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
7. Output delay is shown in *Figure 9: Pad output delay*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
11. Selectable high/low swing IO pad with selectable slew in high swing mode only.
12. Fast pads are 3.3 V pads.
13. Stand alone input buffer. Also has weak pull-up/pull-down.

next Nexus/JTAG command. Expect the affect of EVTI and RDY to be delayed by edges of TCK. Note: RDY is not available in all packages of all devices.

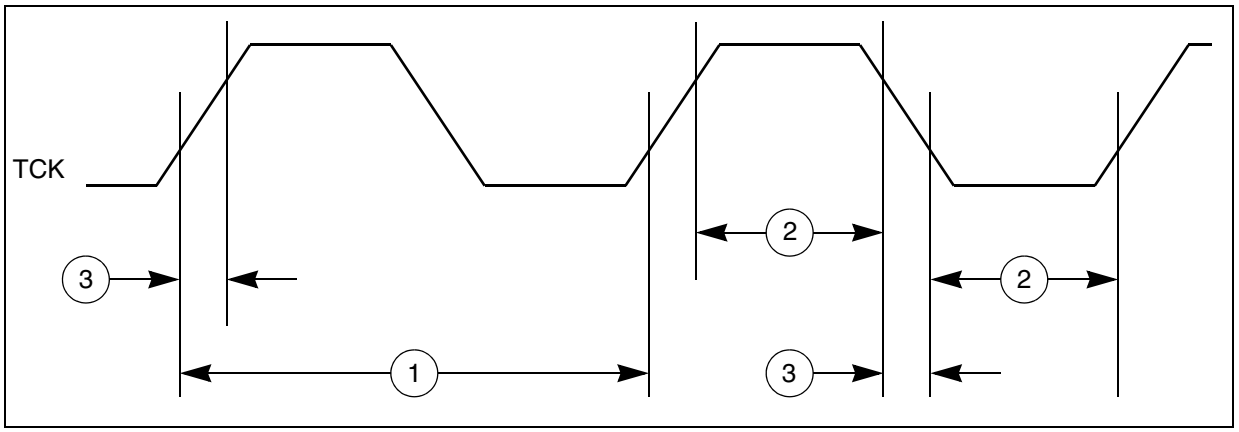


Figure 11. JTAG test clock input timing

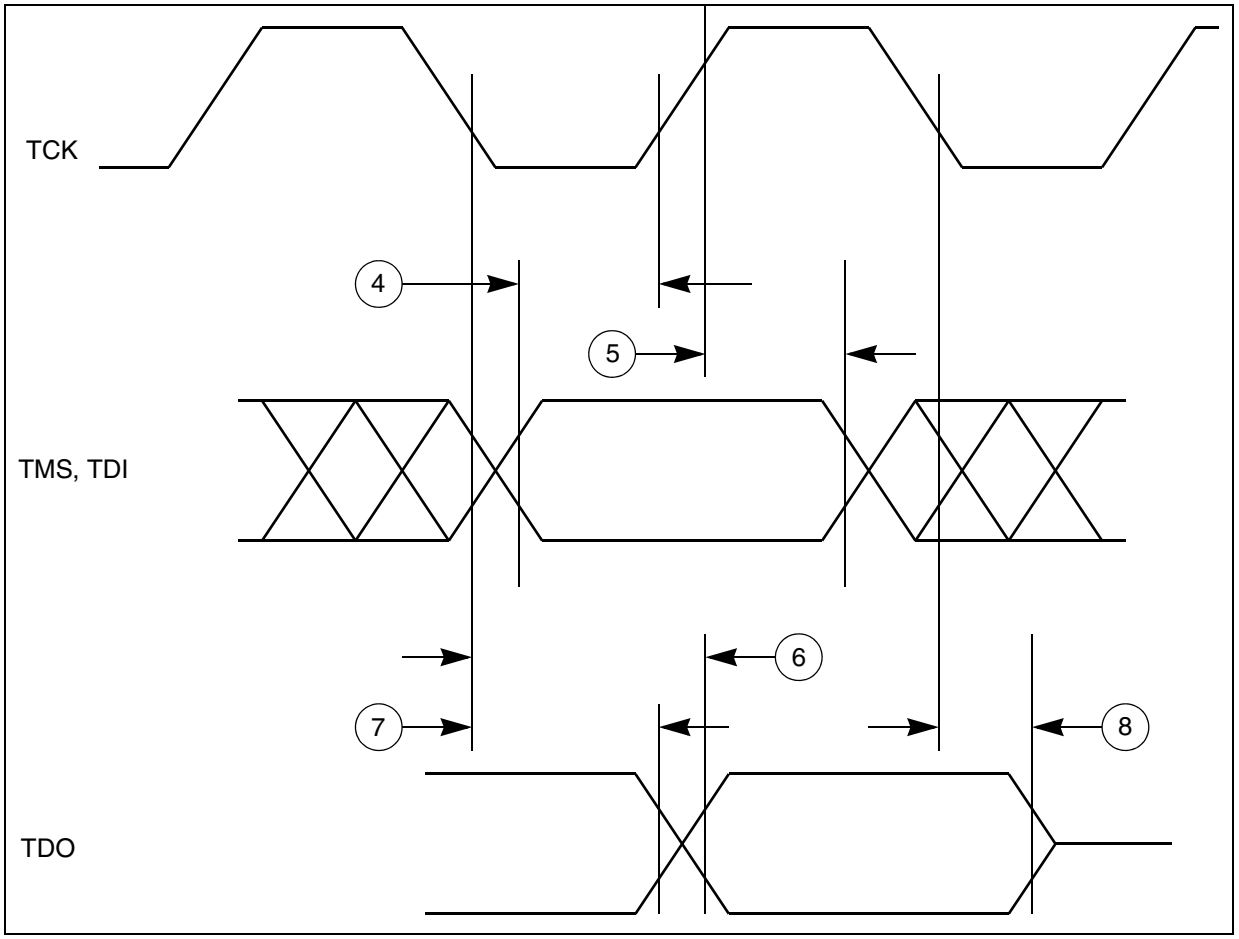
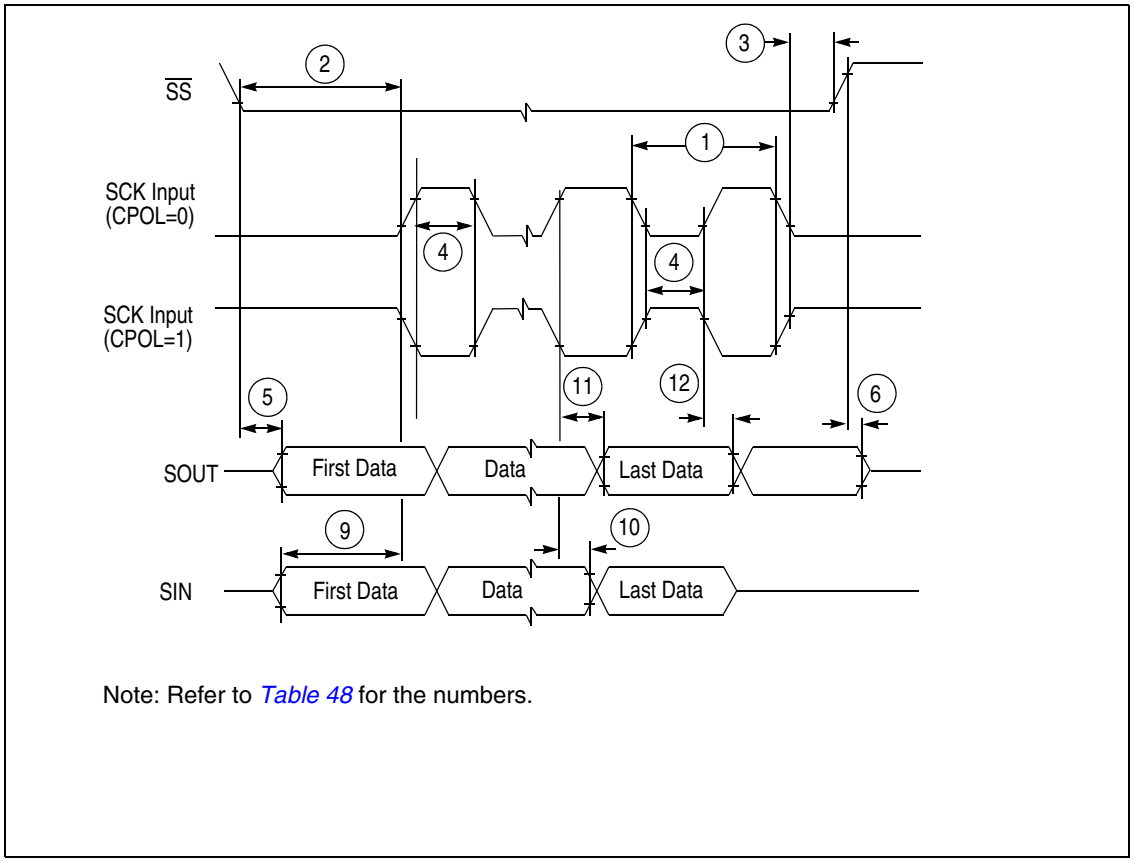


Figure 12. JTAG test access port timing



Note: Refer to *Table 48* for the numbers.

Figure 29. DSPI modified transfer format timing — slave, CPHA =0

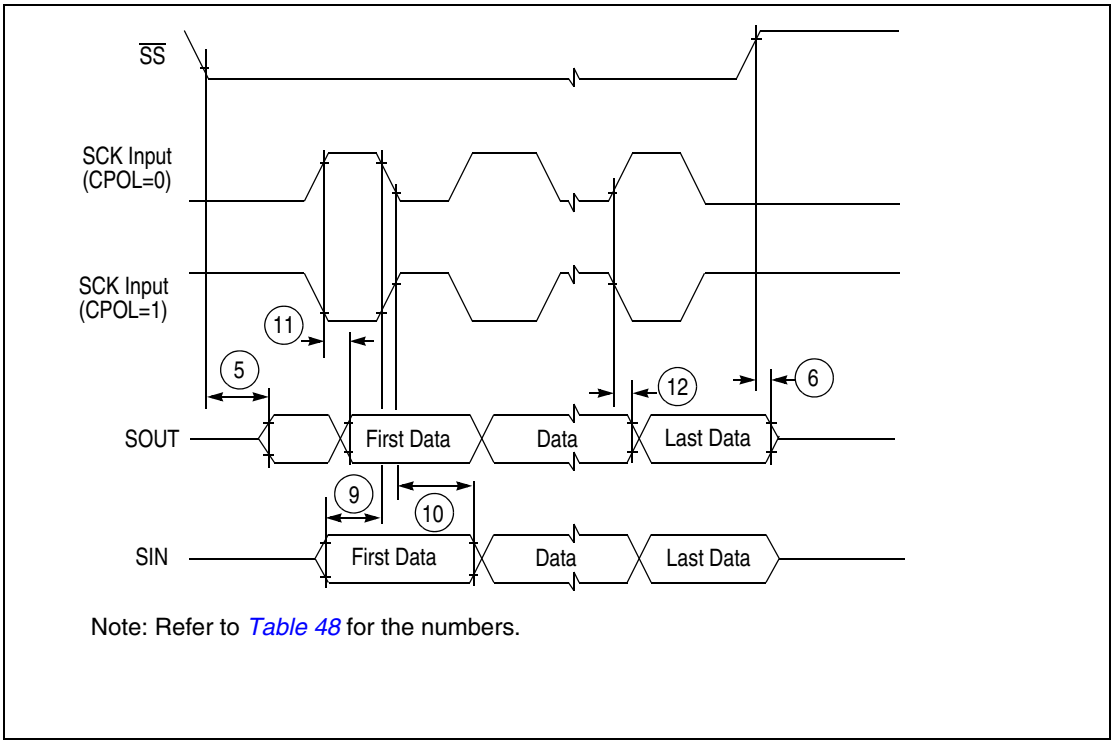


Figure 30. DSPI modified transfer format timing — slave, CPHA =1

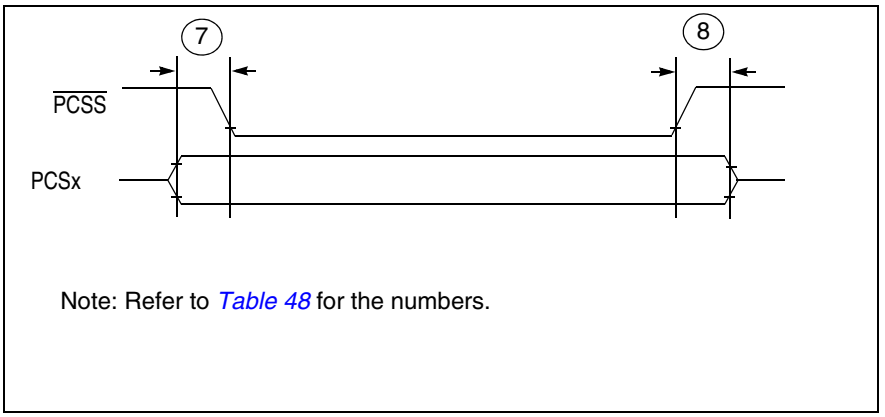


Figure 31. DSPI PCS strobe ($\overline{\text{PCSS}}$) timing

4 Packages

4.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK® is an ST trademark.

Table 52. LQFP176 package mechanical data

REF.	DATABOOK			MILLIMETERS(1)			INCHES		
	TYP	MIN	MAX	TYP	MIN	MAX	TYP	MIN	MAX
A						1.600			0.063
A1					0.050	0.150		0.002	
A2					1.350	1.450		0.053	0.057
b					0.170	0.270		0.007	0.011
C					0.090	0.200		0.004	0.008
D					23.900	24.100		0.941	0.949
E					23.900	24.100		0.941	0.949
e				0.500			0.020		
HD					25.900	26.100		1.020	1.028
HE					25.900	26.100		1.020	1.028
L(2)					0.450	0.750		0.018	0.030
L1				1.000			0.039		
ZD				1.250			0.049		
ZE				1.250			0.049		
ccc						0.080			0.003
ANGLE					0^o	7^o		0	7^o

1. Controlling Dimension: MILLIMETER
2. L dimension is measured at gauge plane at 0.25 above the seating plane.

Table 53. LBGA208 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	16.80	17.00	17.20	0.6614	0.6693	0.6772
D1		15.00			0.5906	
E	16.80	17.00	17.20	0.6614	0.6693	0.6772
E1		15.00			0.5906	
e		1.00			0.0394	
F		1.00			0.0394	
ddd			0.20			0.0079
eee[4]			0.25			0.0098
fff[5]			0.10			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   —Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   —The maximum total package height is calculated by the following methodology:
   A2 Typ+A1 Typ +√ ($A1^2$+$A3^2$+$A4^2$ tolerance values)
   — Low profile: 1.20mm < A ≤ 1.70mm
3. The typical ball diameter before mounting is 0.60mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

4.2.3 PBGA324

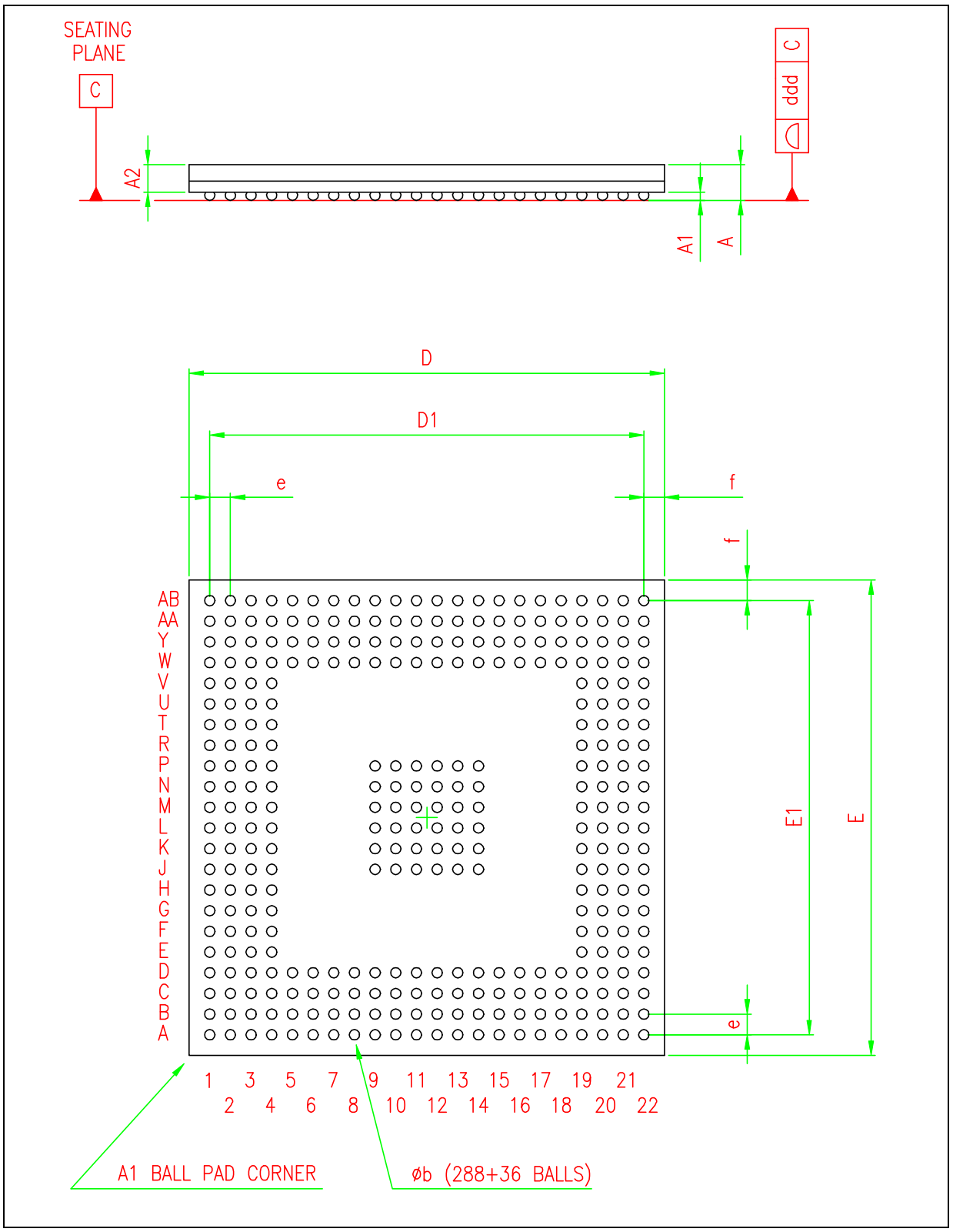


Figure 34. PBGA324 package mechanical drawing