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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a74l7cfar

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1.4 SPC564A80 feature list

- 150 MHz e200z4 Power Architecture core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 4 MB on-chip flash memory with ECC and Read While Write (RWW)
  - 192 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 5 × 4 crossbar switch (XBAR)
  - 24-entry MMU
  - External Bus Interface (EBI) with slave and master port
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 sub-modules
  - Junction temperature sensor
- Interrupts
  - Configurable interrupt controller (with NMI)
  - 64-channel DMA
- Serial channels
  - 3 × eSCI
  - 3 × DSPI (2 of which support downstream Micro Second Channel [MSC])
  - 3 × FlexCAN with 64 messages each
  - 1 × FlexRay module (V2.1) up to 10 Mbit/s with dual or single channel and 128 message objects and ECC
- 1 × eMIOS: 24 unified channels
- 1 × eTPU2 (second generation eTPU)
  - 32 standard channels
  - 1 × reaction module (6 channels with three outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- Nexus
  - Class 3+ for the e200z4 core
  - Class 1 for the eTPU
- JTAG (5-pin)

1.5 Feature details

1.5.1 e200z4 core

SPC564A80 devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New ‘Wait for Interrupt’ instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.5.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
  - External Bus Interface

1.5.17 FlexRay

The SPC564A80 includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
  - Receive message buffer
  - Single buffered transmit message buffer
  - Double buffered transmit message buffer (combines two single buffered message buffer)
- 2 independent receive FIFOs
  - 1 receive FIFO per channel
  - Up to 255 entries for each FIFO
- ECC support

1.5.18 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system 'tick' signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

System timer module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR[(b)]. It consists of a single 32-bit counter, clocked by the system clock,

b. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

1.6.2 Block summary

Table 3 summarizes the functions of the blocks present on the SPC564A80 series microcontrollers.

Table 3. SPC564A80 series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM.
Calibration Bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration tool connector.
Controller area network (FlexCAN)	Supports the standard CAN communications protocol.
Crossbar switch (XBAR)	Internal busmaster.
Cyclic redundancy check (CRC)	CRC checksum generator.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices.
e200z4 core	Executes programs and interrupt handlers.
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events.
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications.
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units.
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention.
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
External bus interface (EBI)	Enables expansion of internal bus to enable connection of external memory or peripherals.
Flash memory	Provides storage for program code, constants, and variables.
FlexRay	Provides high-speed distributed control for advanced automotive applications.
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests.
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode.
Memory protection unit (MPU)	Provides hardware access control for all memory references generated.
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard.

2.2 LBGA208 ballmap

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS3	DSPI_B_SIN	DSPI_B_PCS0	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_PCS4	DSPI_B_PCS2	DSPI_B_PCS1	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS5	SCI_A_TX	GPIO98	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS(1)	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO206	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO219	MDO9_ETPUA25_O	EMIOS13	EMIOS15	MDO5_ETPUA4_O	MDO6_ETPUA13_O	CAN_B_TX	VDDE5	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1. This pin (N13) should be tied low.

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_DATA[11]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[12]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[13]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[14]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[15]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_RD_WR	Calibration read/write enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[0]/$\overline{BE}$[0]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{WE}$[1]/$\overline{BE}$[1]	Calibration write/byte enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_OE	Calibration output enable	P	01	342	O	VDDE12 Fast		— / —	—	—	—
CAL_TS CAL_ALE	Calibration transfer start Address Latch Enable	P A	01 10	343	O O	VDDE12 Fast		— / —	—	—	—
CAL_MDO[4]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[4] / —	—	—	—
CAL_MDO[5]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[5] / —	—	—	—
CAL_MDO[6]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[6] / —	—	—	—
CAL_MDO[7]	Calibration Nexus Message Data Out	P	01	—	O	VDDE12 Fast	—	CAL_MDO[7] / —	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0[18] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[0] / —	172	B5	B8
AN1[18] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[1] / —	171	A6	A8
AN2[18] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[2] / —	170	D6	D10

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN14 - SDI MA2 ETPUA27_O[8] SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7[19] Medium	I / —	AN[14] / —	146	C12	C16
AN15 - FCK FCK ETPUA29_O[8]	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7[19] Medium	I / —	AN[15] / —	145	C13	D16
AN16	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[16] / —	3	C6	B7
AN17	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[17] / —	2	C4	C6
AN18	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[18] / —	1	D5	D9
AN19	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[19] / —	—	—	B6
AN20	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[20] / —	—	—	C7
AN21	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[21] / —	173	B4	C8
AN22	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[22] / —	161	B8	C11
AN23	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[23] / —	160	C9	B11
AN24	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[24] / —	159	D8	D12
AN25	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[25] / —	158	B9	C12

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA24 IRQ[12] DSPI_C_SCK_LVDS- GPIO[138]	eTPU A channel External interrupt request LVDS negative DSPI clock GPIO	P A1 A2 G	001 010 100 000	138	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	28	G1	E1
ETPUA25 IRQ[13] DSPI_C_SCK_LVDS+ GPIO[139]	eTPU A channel External interrupt request LVDS positive DSPI clock GPIO	P A1 A2 G	001 010 100 000	139	I/O I O I/O	VDDEH1 Medium + LVDS	— / WKPCFG	— / WKPCFG	27	G3	E3
ETPUA26 IRQ[14] DSPI_C_SOUT_LVDS- GPIO[140]	eTPU A channel External interrupt request LVDS negative DSPI data out GPIO	P A1 A2 G	001 010 100 000	140	I/O I O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	26	F3	D3
ETPUA27 IRQ[15] DSPI_C_SOUT_LVDS+ DSPI_B_SOUT GPIO[141]	eTPU A channel External interrupt request LVDS positive DSPI data out DSPI data out GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	141	I/O I O O I/O	VDDEH1 Slow + LVDS	— / WKPCFG	— / WKPCFG	25	G2	E2
ETPUA28 DSPI_C_PCS[1] RCH5_B GPIO[142]	eTPU A channel DSPI C peripheral chip select Reaction channel 5B GPIO	P A1 A2 G	001 010 100 000	142	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	24	F1	D1
ETPUA29 DSPI_C_PCS[2] RCH5_C GPIO[143]	eTPU A channel DSPI C peripheral chip select Reaction channel 5C GPIO	P A1 A2 G	001 010 100 000	143	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	23	F2	D2

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 Analog	—	—	93	P16	V22
EXTAL EXTCLK	Crystal oscillator input External clock input	P A	01 10	—	I	VDDEH6 Analog	—	—	92	N16	U22
CLKOUT	System clock output	P	01	229	O	VDDE5 Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE5 Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage Regulator Supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage Regulator Control Output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[20]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—		3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	—	—
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	—	—
VDDA0[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA0	—	B11	A6
VSSA0[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA0	—	A11	A7
VDDA1[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA1	—	A4	C15
VSSA1[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA1	—	A5	A15, B15
VDDPLL	FMPLL Supply Voltage	—		—	I	1.2	I / —	VDDPLL	91	R16	W22
VSTBY	Power Supply for Standby RAM	—		—	I	0.9 V - 6 V	I / —	VSTBY	12	C1	A3

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A80 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.6 Power management control (PMC) and power on reset (POR) electrical specifications

Table 15. PMC Operating Conditions and External Regulators Supply Voltage

ID	Name			Parameter	Min	Typ	Max	Unit
1	Jtemp	SR	—	Junction temperature	–40	27	150	°C
2	Vddreg	SR	—	PMC 5 V supply voltage V_{DDREG}	4.75	5	5.25	V
3	Vdd	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used without disabling the internal regulator (PMC unit turned on, LVI monitor active)(1)	1.26(2)	1.3	1.32	V
3a	—	SR	—	Core supply voltage 1.2 V V_{DD} when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	1.14	1.2	1.32	V
4	Ivdd	SR	—	Voltage regulator core supply maximum required DC output current	445	—	—	mA
5	Vdd33	SR	—	Regulated 3.3 V supply voltage when external regulator is used without disabling the internal regulator (PMC unit turned-on, internal 3.3V regulator enabled, LVI monitor active)(3)	3.3	3.45	3.6	V
5a	—	SR	—	Regulated 3.3 V supply voltage when external regulator is used with a disabled internal regulator (PMC unit turned-off, LVI monitor disabled)	3	3.3	3.6	V
6	—	SR	—	Voltage regulator 3.3 V supply maximum required DC output current	80	—	—	mA

1. An internal regulator controller can be used to regulate core supply.
2. The minimum supply required for the part to exit reset and enter in normal run mode is 1.28 V.
3. An internal regulator can be used to regulate 3.3 V supply.

Table 16. PMC Electrical Characteristics

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
1	VBG	CC	C	Nominal bandgap voltage reference	—	1.219	—	V	
1a	—	CC	P	Untrimmed bandgap reference voltage	VBG - 7%	VBG	Vbg + 6%	V	
1b	—	CC	P	Trimmed bandgap reference voltage (5 V, 27 °C)	VBG -10mV	VBG	VBG + 10mV	V	
1c	—	CC	C	Bandgap reference temperature variation	—	100	—	ppm/°C	
1d	—	CC	C	Bandgap reference supply voltage variation	—	3000	—	ppm/V	

Table 16. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
2	Vdd	CC	C	Nominal V_{DD} core supply internal regulator target DC output voltage(1)	—	1.28	—	V	
2a	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation at power-on reset	Vdd - 6%	Vdd	Vdd + 10%	V	
2b	—	CC	P	Nominal V_{DD} core supply internal regulator target DC output voltage variation after power-on reset	Vdd - 10%(2)	Vdd	Vdd + 3%	V	
2c	—	CC	C	Trimming step Vdd	—	20	—	mV	
2d	Ivrcctl	CC	C	Voltage regulator controller for core supply maximum DC output current	20	—	—	mA	
3	Lvi1p2	CC	C	Nominal LVI for rising core supply(3)	—	1.160	—	V	
3a	—	CC	C	Variation of LVI for rising core supply at power-on reset	1.120	1.200	1.280	V	See note (4)
3b	—	CC	C	Variation of LVI for rising core supply after power-on reset	Lvi1p2 - 3%	Lvi1p2	Lvi1p2 + 3%	V	See note (4)
3c	—	CC	C	Trimming step LVI core supply	—	20	—	mV	
3d	Lvi1p2_h	CC	C	LVI core supply hysteresis	—	40	—	mV	
4	Por1.2V_r	CC	C	POR 1.2 V rising	—	0.709	—	V	
4a	—	CC	C	POR 1.2 V rising variation	Por1.2V_r - 35%	Por1.2V_r	Por1.2V_r + 35%	V	
4b	Por1.2V_f	CC	C	POR 1.2 V falling	—	0.638	—	V	
4c	—	CC	C	POR 1.2 V falling variation	Por1.2V_f - 35%	Por1.2V_f	Por1.2V_f + 35%	V	
5	Vdd33	CC	C	Nominal 3.3 V supply internal regulator DC output voltage	—	3.39	—	V	
5a	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation at power-on reset	Vdd33 - 8.5%	Vdd33	Vdd3 + 7%	V	See note (5)
5b	—	CC	P	Nominal 3.3 V supply internal regulator DC output voltage variation power-on reset	Vdd33 - 7.5%	Vdd33	Vdd33 + 7%	V	With internal load up to Idd3p3

3.8 DC electrical specifications

Table 21. DC electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14		1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62		3.6	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{DDE-EH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{RC33}	SR	—	3.3 V regulated voltage(1)	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75(2)	—	5.25	V
V_{INDC}	SR	—	Analog input voltage	—	V_{SSA}-0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	VRL differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA}-0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage(3)	—	1.14	—	1.32	V
V_{FLASH}(4)	SR	—	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
			Keep-out Range: 1.2V–2V	Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium I/O pad input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDEH}	

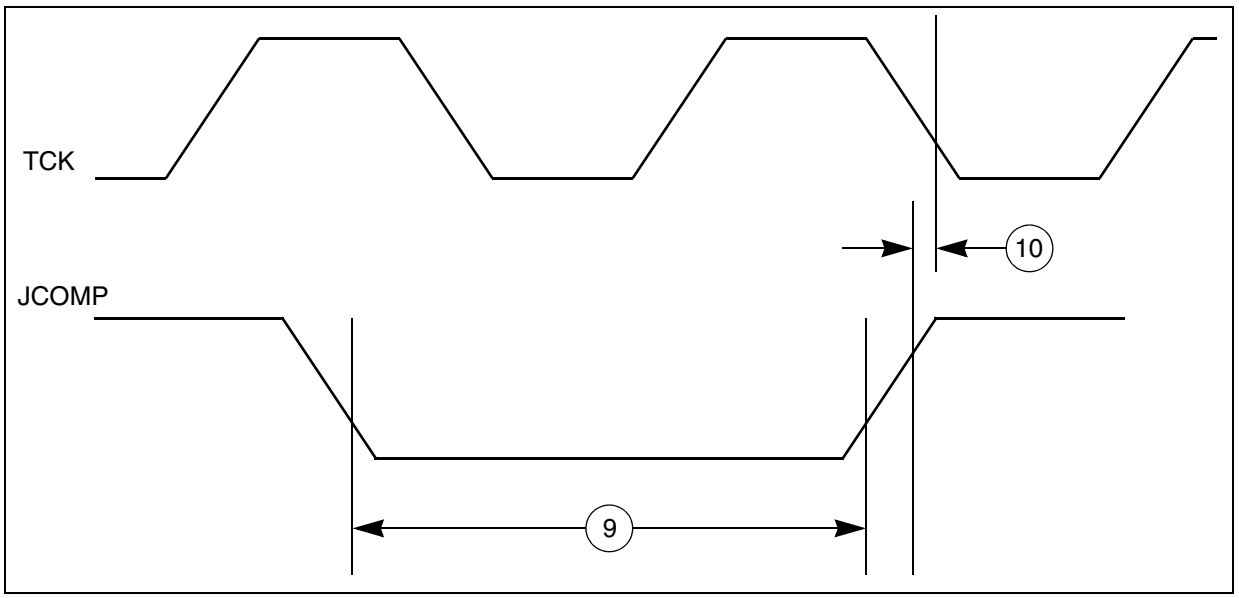
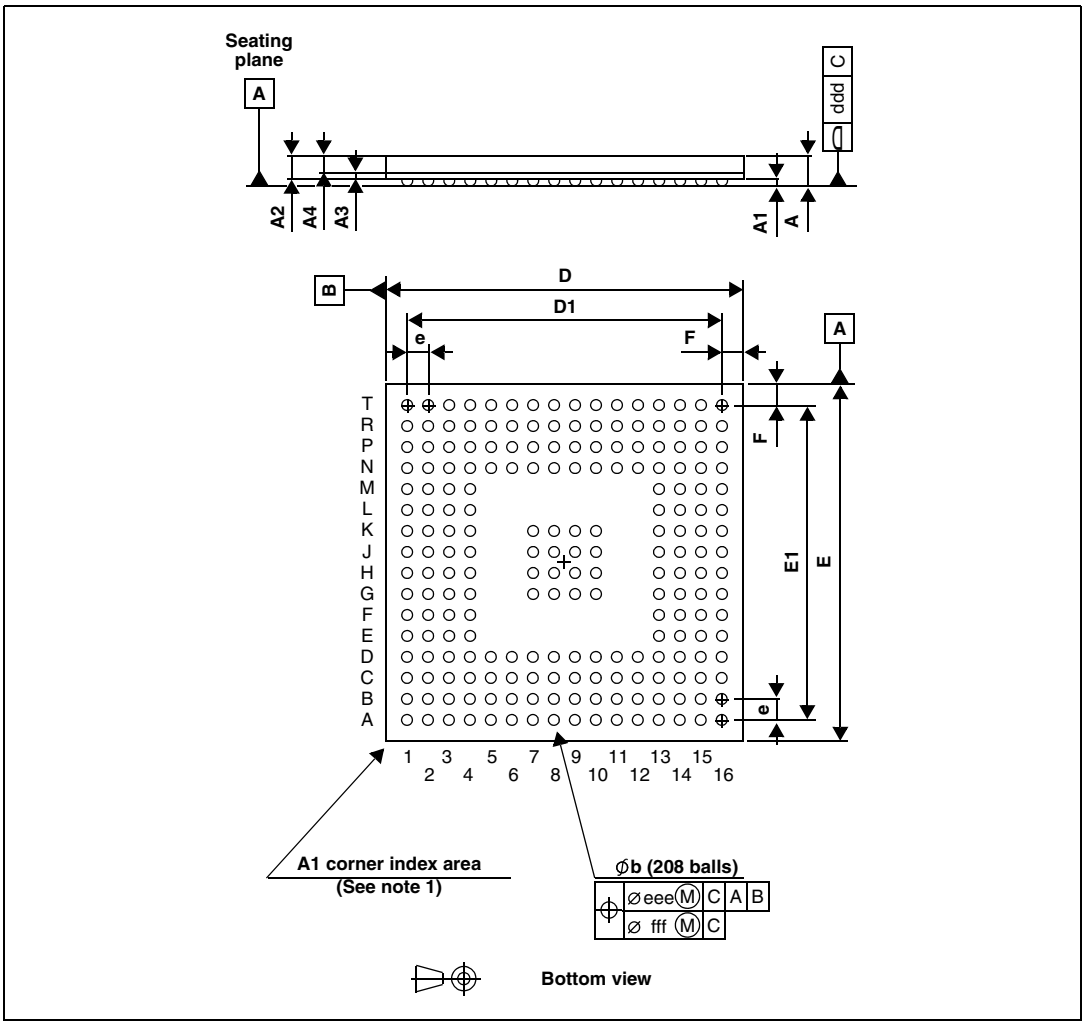


Figure 13. JTAG JCOMP timing

4.2.2 BGA208



1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 53. LBGA208 mechanical data

Symbol	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)			1.70			0.0669
A1	0.30			0.0118		
A2		1.085			0.0427	
A3		0.30			0.0118	
A4			0.80			0.0315
b(3)	0.50	0.60	0.70	0.0197	0.0236	0.0276

Figure 35. Product code structure

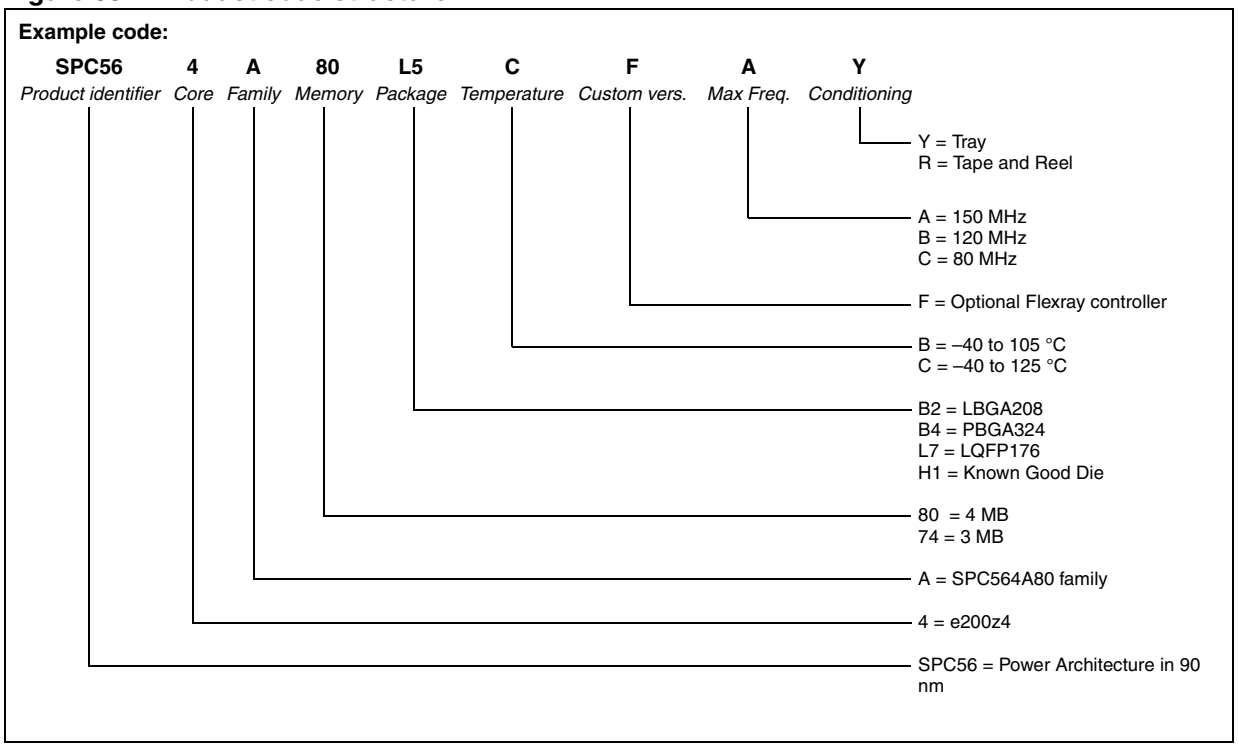


Table 56. Revision history (continued)

Date	Revision	Changes
01-Oct-2010 (cont)	4 (cont)	Updates to EBI timings: – Note added to t_{AAI}: When CAL_TS is used as CAL_ALE the hold time is 1 ns instead of 1.5 ns. – Correction: maximum calibration bus interface operating frequency is 66 MHz for all port configurations. – VDDE range in footnote 1 corrected to read, “External Bus and Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, VDD = 1.14 V to 1.32 V, VDDE = 3 V to 3.6 V (unless stated otherwise)” (VDDE range was 1.62 V to 3.6 V) Correction to IEEE 1149.1 timings: – SRC value in footnote 1 corrected to read, “JTAG timing specified at VDD = 1.14 V to 1.32 V, VDDEH = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, TA = TL to TH, and CL = 30 pF with DSC = 0b10, SRC = 0b11.” (SRC value was 0b00) Correction to External interrupt timing (IRQ pin) timings: – Timings are specified at V_{DD} = 1.14 V to 1.32 V (was 1.08 V to 1.32 V). Update to DSPI timings: – Some of the timing parameters can vary depending on the value of V_{DDE}. For these parameters, ranges are now defined for two ranges of V_{DDE}. Change in signal name notation for DSPI, CAN and SCI signals: – DSPI: PCS_x[n] is now DSPI_x_PCS[n] SOUT_x is now DSPI_x_SOUT SIN_x is now DSPI_x_SIN SCK_x is now DSPI_x_SCK – CAN: CNTXx is now CAN_x_TX CNRXx is now CAN_x_RX – SCI: RXDx is now SCI_x_RX TXDx is now SCI_x_TX Updates to DC electrical specifications: – Slew rate on power supply pins specification changed to 25 V/ms (was 50 V/ms) V_{OH_LS} min spec changed to 2.0 V at 0.5 mA (was 2.7 V at 0.5 mA) Updated I/O pad current specifications Updated I/O pad V_{RC33} current specifications Corrections to Nexus timing: – Maximum Nexus debug port operating frequency is 40 MHz in all configurations – To route Nexus to MDO, clear NPC_PCR[NEXCFG] (formerly this was documented as NPC_PCR[CAL] – To route Nexus to CAL_MDO, set NPC_PCR[NEXCFG]=1 (formerly this was documented as NPC_PCR[CAL]
10-Feb-2011	5	– Minor editorial updates. – Re-organized the first few subsections of the “Overview” section. – Added ECSM to the block diagram. – Added information on the REACM, SIU, and ECS modules to the “Block summary” section.