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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	3MB (3M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	160K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a74l7cfay

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1 Introduction

1.1 Document Overview

This document provides electrical specifications, pin assignments, and package diagrams for the SPC564A80 series of microcontroller units (MCUs). For functional characteristics, refer to the *SPC564A80 Microcontroller Reference Manual.*

1.2 Description

The microcontroller's e200z4 host processor core is built on Power Architecture technology and designed specifically for embedded applications. In addition to the Power Architecture technology, this core supports instructions for digital signal processing (DSP).

The SPC564A80 has two levels of memory hierarchy consisting of 8 KB of instruction cache, backed by 192 KB on-chip SRAM and 4 MB of internal flash memory. The SPC564A80 includes an external bus interface, and also a calibration bus that is only accessible when using the calibration tools.

This document describes the features of the SPC564A80 and highlights important electrical and physical characteristics of the device.

1.3 Device comparison

Table 2 summarizes the SPC564A80 and compares it to the SPC563M64.

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison

Feature		SPC564A80	SPC563M64	SPC564A70
Process		90 nm		
Core		e200z4	e200z3	e200z4
	SIMD	Yes		
	VLE	Yes		
	Cache	8 KB instruction	No	8 KB instruction
	Non-Maskable Interrupt (NMI)	NMI & Critical Interrupt		
	MMU	24 entry	16 entry	24 entry
	MPU	16 entry	No	16 entry
	Crossbar switch	5 × 4	3 × 4	4 × 4
	Core performance	0–150 MHz	0–80 MHz	0–150 MHz
Windowing software watchdog		Yes		
Core Nexus		Class 3+	Class 2+	Class 3+
SRAM		192 KB	94 KB	128 KB
Flash		4 MB	1.5 MB	2 MB
Flash fetch accelerator		4 × 256-bit	4 × 128-bit	
External bus		16-bit (incl 32-bit muxed)	None	
Calibration bus		16-bit (incl 32-bit muxed)	16-bit	16-bit (incl 32-bit muxed)
DMA		64 ch.	32 ch.	64 ch.
DMA Nexus		None		
Serial		3	2	3
	eSCI_A	Yes (MSC Uplink)		
	eSCI_B	Yes (MSC Uplink)		
	eSCI_C	Yes	No	Yes
CAN		3	2	3
	CAN_A	64 buf		
	CAN_B	64 buf	No	64 buf
	CAN_C	64 buf	32 buf	64 buf
SPI		3	2	3

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison (continued)

Feature		SPC564A80	SPC563M64	SPC564A70
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch.(1)	307 ch.	486 ch.(1)
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V(2)	5 V, 3.3 V(3)	5 V, 3.3 V(2)
Low-power modes		Stop Mode Slow Mode		
Packages		LQFP176(4) LBGA208(4) PBGA Known Good Die (KGD) 496-pin CSP(5)	LQFP100 LQFP144 LQFP176 LBGA208 496-pin CSP(5)	LQFP176(4) LBGA208(4) PBGAKnown Good Die (KGD) 496-pin CSP(5)

1. 199 interrupt vectors are reserved.
2. 5 V single supply only for LQFP176.
3. 5 V single supply only for LQFP144 and LQFP100.
4. Pinout compatible with STMicroelectronics' SPC563M64 devices.
5. For ST calibration tool only.

  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.14 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the SPC564A80 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A80 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHZ for SOUT and SCK pins for DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI Module can generate and check parity in a serial frame

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A80.

The sources of the ECC errors are:

- Flash
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 Parameter RAM)

1.5.22 External bus interface (EBI)

The SPC564A80 device features an external bus interface that is available in PBGA324 and calibration packages.

The EBI supports operation at frequencies of system clock /1, /2 and /4, with a maximum frequency support of 80 MHz. Customers running the device at 120 MHz or 132 MHz will use the /2 divider, giving an EBI frequency of 60 MHz or 66 MHz. Customers running the device at 80 MHz will be able to use the /1 divider to have the EBI run at the full 80 MHz frequency.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller with support for various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing included to support 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The Calibration EBI is only available in the calibration tool.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

VSS	VSS	VSS					DSPI_A_ PCS1	DSPI_A_ PCS0	GPIO98	VDDREG	M
VSS	VSS	VSS					DSPI_A_ PCS4	SCI_A_TX	DSPI_A_ PCS5	NIC(1)	N
VSS	VSS	VSS					CAN_C_TX	SCI_A_RX	RSTOUT	RSTCFG	P
							WKPCFG	CAN_C_RX	SCI_B_TX	RESET	R
							SCI_B_RX	BOOTCFG1	VSS(2)	VSS	T
							VDDEH6AB	PLLCFG1	BOOTCFG0	EXTAL	U
							VDD	VRCCTL	PLLREF	XTAL	V
EMIOS2	EMIOS8	VDDEH4AB	EMIOS12	EMIOS21	VDDE5	SCI_C_TX	VSS	VDD	NIC(1)	VDDPLL	W
EMIOS6	EMIOS10	EMIOS15	EMIOS17	EMIOS22	CAN_A_TX	VDDE5	SCI_C_RX	VSS	VDD	VRC33	Y
EMIOS5	EMIOS9	EMIOS13	EMIOS16	EMIOS19	EMIOS23	CAN_A_RX	VDDE5	CLKOUT	VSS	VDD	AA
EMIOS4	EMIOS7	EMIOS11	EMIOS14	EMIOS18	EMIOS20	CAN_B_TX	CAN_B_RX	VDDE5	ENGCLK	VSS	AB
12	13	14	15	16	17	18	19	20	21	22	

1. Pins marked “NIC” have no internal connection.
2. This pin (T21) should be tied low.

Figure 7. 324-pin PBGA package ballmap (southeast, viewed from above)

2.4 Signal summary

Table 4. SPC564A80 signal properties

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7] During Reset	Status[7] After Reset	Package pin # 176	Package pin # 208	Package pin # 324
GPIO											
EMIOS14[8] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 Slow	— / Up	— / Up	—	—	H20
EMIOS15[8] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 Slow	— / Up	—/ Up	—	—	H21
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[9]	VDDEH7 Slow[10]	— / Up	— / Up	143	R4	AA7
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[9]	VDDEH7 Slow	— / Up	— / Up	144	P5	Y9
GPIO[219]	GPIO	G	—	219[11]	I/O	VDDEH7 MultiV[12]	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF $\overline{\text{IRQ}}$[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 Slow	— / Up	PLLREF / Up	83	M14	V21
PLLCFG1[13] $\overline{\text{IRQ}}$[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 Slow	— / Down	—	—	—	P22

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR30 ADDR6[8] DATA30 GPIO[26]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	26	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	W3
ADDR31 ADDR7[8] DATA31 GPIO[27]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	27	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V4
DATA0 ADDR16 GPIO[28]	External data bus External address bus GPIO	P A1 G	001 010 000	28	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB4
DATA1 ADDR17 GPIO[29]	External data bus External address bus GPIO	P A1 G	001 010 000	29	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA5
DATA2 ADDR18 GPIO[30]	External data bus External address bus GPIO	P A1 G	001 010 000	30	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB5
DATA3 ADDR19 GPIO[31]	External data bus External address bus GPIO	P A1 G	001 010 000	31	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB6
DATA4 ADDR20 GPIO[32]	External data bus External address bus GPIO	P A1 G	001 010 000	32	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB7
DATA5 ADDR21 GPIO[33]	External data bus External address bus GPIO	P A1 G	001 010 000	33	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA8
DATA6 ADDR22 GPIO[34]	External data bus External address bus GPIO	P A1 G	001 010 000	34	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB8

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_DATA[0]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[1]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0[18] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[0] / —	172	B5	B8
AN1[18] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[1] / —	171	A6	A8
AN2[18] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[2] / —	170	D6	D10

3.4 EMI (electromagnetic interference) characteristics

Table 13. EMI Testing Specifications(1)

Symbol	Parameter	Conditions	Clocks	Frequency Range	Level (Max)	Unit
Radiated emissions, electric field	V_{RE_TEM}	V_{DDREG} = 5.25 V; T_A = 25 °C 150 kHz – 30 MHz RBW 9 kHz, Step Size 5 kHz 30 MHz – 1 GHz - RBW 120 kHz, Step Size 80 kHz	16 MHz crystal 40 MHz bus No PLL frequency modulation	150 kHz – 50 MHz	20	dBµV
				50 – 150 MHz	20	
				150 – 500 MHz	26	
				500 – 1000 MHz	26	
				IEC Level	K	—
				SAE Level	3	—
			16 MHz crystal 40 MHz bus ± 2% PLL frequency modulation	150 kHz– 50 MHz	13	dBµV
				50 – 150 MHz	13	
				150 – 500 MHz	11	
				500 – 1000 MHz	13	
				IEC Level	L	—
				SAE Level	2	—

1. EMI testing and I/O port waveforms per SAE J1752/3 issued 1995-03 and IEC 61967-2.

3.5 Electrostatic discharge (ESD) characteristics

Table 14. ESD ratings(1),(2)

Symbol		Parameter	Conditions	Value	Unit
—	SR	ESD for Human Body Model (HBM)	—	2000	V
R1	SR	HBM circuit description	—	1500	Ω
C	SR		—	100	pF
—	SR	ESD for field induced charge Model (FDCM)	All pins	500	V
			Corner pins	750	
—	SR	Number of pulses per pin	Positive pulses (HBM)	1	—
			Negative pulses (HBM)	1	—
—	SR	Number of pulses	—	1	—

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Device failure is defined as: “If after exposure to ESD pulses, the device does not meet the device specification requirements, which includes the complete DC parametric and functional testing at room temperature and hot temperature.”

3.9.1 I/O pad V_{RC33} current specifications

The power consumption of the V_{RC33} supply is dependent on the usage of the pins on all I/O segments. The power consumption is the sum of all input and output pin V_{RC33} currents for all I/O segments. The output pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all fast pad pins. The input pin V_{RC33} current can be calculated from *Table 23* based on the voltage, frequency, and load on all medium-speed pads. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 23*.

Table 23. I/O pad V_{RC33} average I_{DDE} specifications(1)

Pad Type	Symbol		C	Period (ns)	Load (2) (pF)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	100	50	11	0.8	235.7
		CC	D	200	50	01	0.04	87.4
		CC	D	800	50	00	0.06	47.4
		CC	D	800	200	00	0.009	47
Medium	$I_{DRV\_MSR\_HV}$	CC	D	40	50	11	2.75	258
		CC	D	100	50	01	0.11	76.5
		CC	D	500	50	00	0.02	56.2
		CC	D	500	200	00	0.01	56.2
MultiV(3) (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	11	33.4	35.4
		CC	D	30	50	01	33.4	34.8
		CC	D	117	50	00	33.4	33.8
		CC	D	212	200	00	33.4	33.7
MultiV(4) (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	11	33.4	34.9

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.
3. Average current is for pad configured as output only.
4. In low swing mode, multi-voltage pads must operate in highest slew rate setting.

Table 33. Flash program and erase specifications(1) (continued)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	3000	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5300	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.
4. Page size is 128 bits (4 words).
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.17 AC timing

3.17.1 Reset and configuration pin timing

Table 37. Reset and Configuration Pin Timing(1)

#	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width(2)	t_{RPW}	10	—	t_{cyc}
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}
3	PLLREF, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}
4	PLLREF, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.14 V to 1.32 V, $T_A = T_L$ to T_H.
2. $\overline{\text{RESET}}$ pulse width is measured from 50% of the falling edge to 50% of the rising edge.

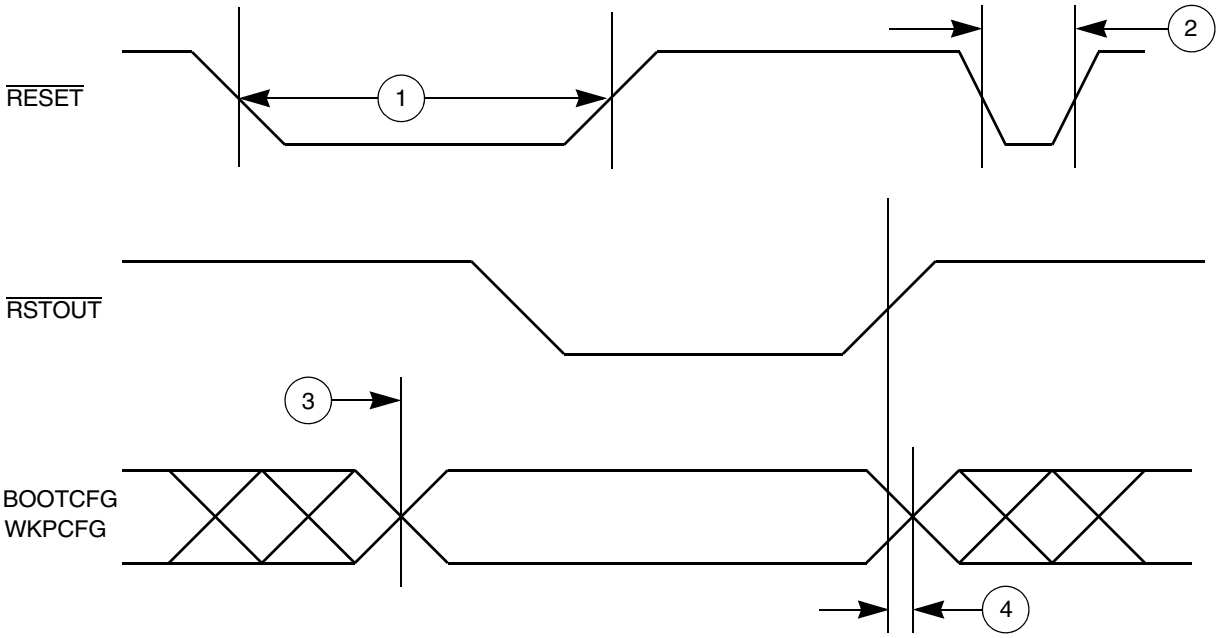

Figure 10. Reset and Configuration Pin Timing

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	22[2]	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	22	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	25[3]	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	25[3]	—	ns

1. JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b11. These specifications apply to JTAG boundary scan only. See *Table 39* for functional specifications.
2. Pad delay is 8–10 ns. Remainder includes TCK pad delay, clock tree delay logic delay and TDO output pad delay.
3. For 20 MHz TCK.

Note: The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK. In addition, EVTI is not latched into the device unless there are clock transitions on TCK.

The tool/debugger must provide at least one TCK clock for the EVTI signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least 1 TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the

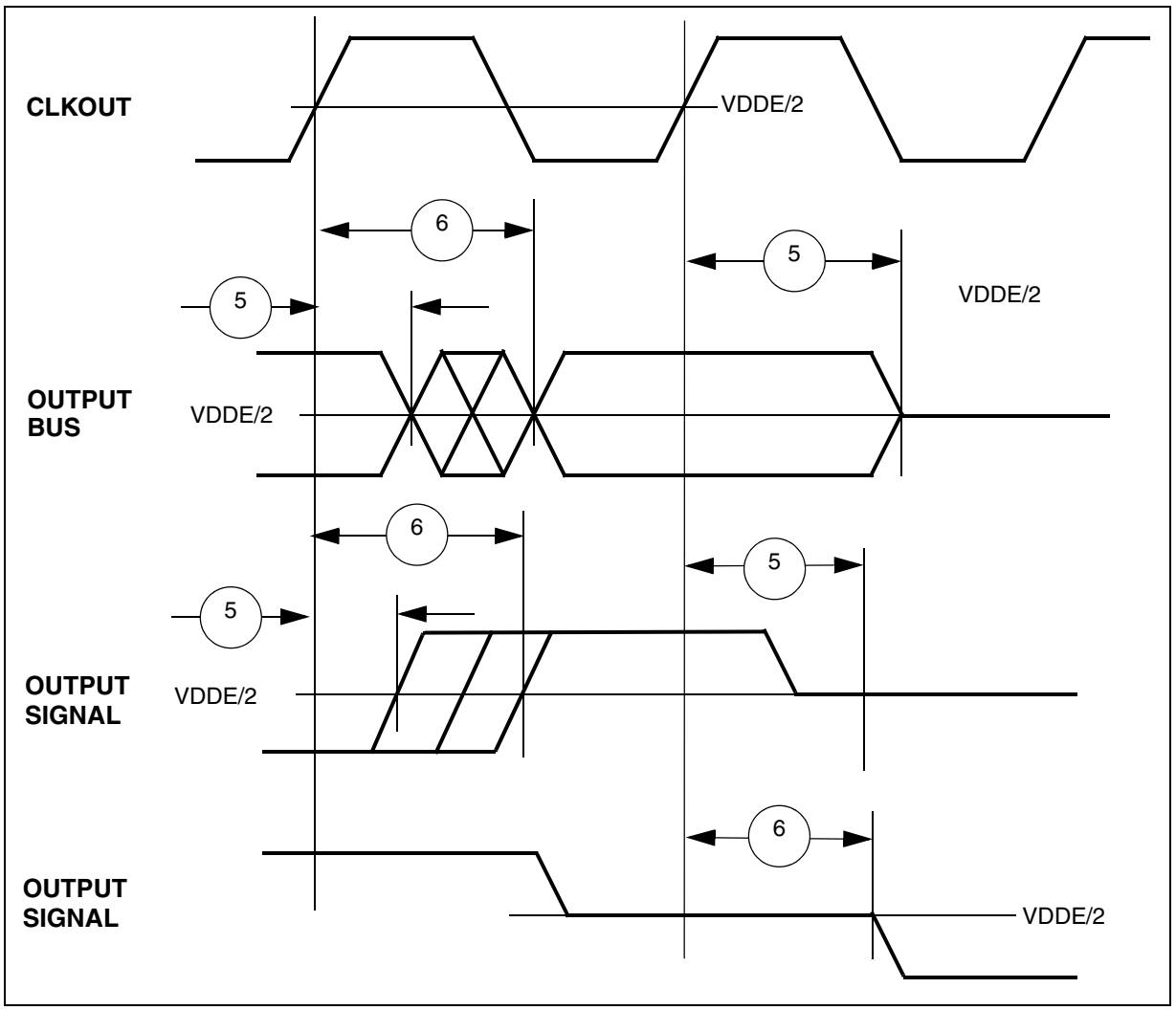

Figure 19. Synchronous output timing

3.17.7 eMIOS timing

Table 46. eMIOS timing(1)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{MIPW}	CC	D	eMIOS Input Pulse Width	4	—	t_{CYC}
2	t_{MOPW}	CC	D	eMIOS Output Pulse Width	1	—	t_{CYC}

1. eMIOS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b00.

3.17.8 DSPI timing

DSPI channel frequency support for the SPC564A80 MCU is shown in *Table 47*. Timing specifications are in *Table 48*.

Table 47. DSPI channel frequency support

System Clock (MHz)	DSPI Use Mode	Max. Usable Frequency (MHz)	Notes
150	LVDS	37.5	Use sysclock /4 divide ratio.
	Non-LVDS	18.75	Use sysclock /8 divide ratio.
120	LVDS	40	Use sysclock /3 divide ratio. Gives 33/66 duty cycle. Use DSPI configuration DBR=0b1 (double baud rate), BR=0b0000 (scaler value 2) and PBR=0b01 (prescaler value 3).
	Non-LVDS	20	Use sysclock /6 divide ratio.
80	LVDS	40	Use sysclock /2 divide ratio.
	Non-LVDS	20	Use sysclock /4 divide ratio.

Table 48. DSPI timing(1),(2)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
1	t_{SCK}	CC	D	SCK Cycle Time(3),(4),(5)		24.4 ns	2.9 ms	—
2	t_{CSC}	CC	D	PCS to SCK Delay(6)		22(7)	—	ns
3	t_{ASC}	CC	D	After SCK Delay(8)		21(9)	—	ns
4	t_{SDC}	CC	D	SCK Duty Cycle		$(½t_{SC})–2$	$(½t_{SC})+2$	ns
5	t_A	CC	D	Slave Access Time ($\overline{SS}$ active to SOUT driven)		—	25	ns
6	t_{DIS}	CC	D	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)		—	25	ns
7	t_{PCSC}	CC	D	PCSx to $\overline{PCSS}$ time		4(10)	—	ns
8	t_{PASC}	CC	D	$\overline{PCSS}$ to PCSx time		5(11)	—	ns

Table 56. Revision history (continued)

Date	Revision	Changes
09-Dec-2009	2	– C4 is VDD (was VDDEH1A) – C15 is VDDA (was VDDA0) – C16 is AN14_SDI (was AN14) – C17 is MDO5_ETPUA4O (was MDO5) – C21 is NIC1 (was VDDE7) – D15 is VDDEH7 (was VDDEH9) – D16 is AN15_FCK (was AN15) – D17 is MDO6_ETPUA13O (was MDO6) – D20 is NIC (was VDDE7) – E19 is NIC (was VDDE7) – E22 is NIC (was NC) – F19 is NIC (was VDDE7) – H4 is VDDEH1AB (was VDDEH1A) – H19 is VDDEH6AB (was VDDEH10) – J14 is NIC (was VDDE7) – K19 is GPIO99 (was PCSA3) – M9 is VDDE2 (was VDD2) – M21 is GPIO98 (was PCSA2) – M22 is VDDREG (was NC) – N22 is NIC (was NC) – P2 is ADDR17 (was ADD17) – P4 is VRC33 (was VDD33) – R3 is VDDE-EH (was VDDE2) – T21 is VSS (was VRCVSS) – T22 is VSS (was VSSPLL) – U19 is VDDEH6AB (was VDDEH6A) – W2 is VDDE-EH (was VDDE2) – W7 is VRC33 (was VDD33) – W14 is VDDEH4AB (was VDDEH4B) – W21 is NIC (was VRC33) – Y22 is VRC33 (was VDD33) – AB22 is VSS (was VSSPLL) Recommended operating characteristics for power transistor updated Pad current specifications updated LVDS pad specifications updated. SRC does not apply to common mode voltage. Temperature sensor electrical characteristics added eQADC electrical characteristics updated with VGA gain specs Pad AC specifications updated Definition for RDY signal added to signal details V_{STBY} maximum is 5.5 V (was listed incorrectly as 6.0 V) I_{MAXA} maximum is 5 mA (was TBD) Analog differential input functions added to AN0–AN7 in signal summary

Table 56. Revision history (continued)

Date	Revision	Changes
03-Feb-2012	6	– Minor editorial changes. – In *Section 1.4: SPC564A80 feature list*, moved “24 unified channels” after “1 x eMIOS”. – In *Table 4* updated the following rows: DSPI_D_SCK /GPIO [98] -Changed “-” to CS[2] DSPI_D_SIN /GPIO[99] -Changed “-” to CS[3]. – In *Table 12* Column “Value” added conditional text. – In *Table 21* made the following changes: -For the value “VOL_S” parameter changed from “Slow/ medium/multi-voltage pad I/O output low voltage” to “Slow/medium pad I/O output low voltage”. -Added a new row for “IDDSTBY27”. -For row “IDDSTBY(operating current 0.95 -1.2V)” added max value “100” and changed typ value from “125” to “35”. -For row “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “110” and changed typ value from “135” to “45”. -For symbol “$I_{DDSTBY\ 150}$(operating current 0.95 -1.2V)” added max value “2000”, changed typ value from “1050” to “790”,C cell changed from “T” to “P” and for symbol “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “2000”, changed typ value from “1050” to “760”, C cell changed from “T” to “P”. -Removed note 9 and note 10 (Characterization based capability) from symbol “V_{OL_HS}”. – Splitted *Table 28: eQADC conversion specifications (operating)* into *Table 29: eQADC single ended conversion specifications (operating)* and *Table 30: eQADC differential ended conversion specifications (operating)* – In *Table 30: eQADC differential ended conversion specifications (operating)* made the following changes: -Added the note of $DIFF_{cmv}$ on all of the DIFF specs. -Min value changed from (VRH-VRL)/2-5% to (VRH+VRL)/2-5 % and max value changed from (VRH-VRL)/2+5% to (VRH+VRL)/2+5%for DIFFcmv. – In *Table 31: Cutoff frequency for additional SRAM wait state* made the following changes: -Added note “Max frequencies including 2% PLL FM”. -Max operating frequency changed from “96” to “98” and “150” to “153”. – In *Section 3.13: Configuring SRAM wait states*, changed text from “SPC564A80 4M Microcontroller Reference Manual “ to “device reference manual”. – In *Table 32: APC, RWSC, WWSC settings vs. frequency of operation* - Added note for “Max Flash Operating Frequency(MHz). - Changed values from 30, 60,120, 150 to 20,61,123, 153 respectively in Max Flash Operating Frequency (MHz). – In *Table 33: Flash program and erase specifications*, added two parameter “T_{psrt}” and “T_{esrt}”. – In *Table 41: External Bus Interface maximum operating frequency*, replacedthe <= symbol in notes with ≤ – Added note “Refer to table DSPI timing for the numbers” in all the figures under *Section 3.17.8: DSPI timing* .