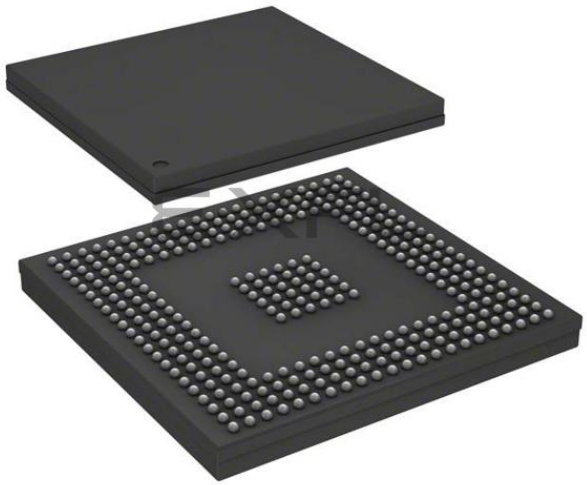

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80b4cfar

- Supports booting from calibration bus interface
- Supports censorship protection for internal flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

1.5.10 eMIOS

The eMIOS timer module provides the capability to generate or measure events in hardware.

The eMIOS module features include:

- Twenty-four 24-bit wide channels
- 3 channels' internal timebases can be shared between channels
- 1 Timebase from eTPU2 can be imported and used by the channels
- Global enable feature for all eMIOS and eTPU timebases
- Dedicated pin for each channel (not available on all package types)

Each channel (0–23) supports the following functions:

- General-purpose input/output (GPIO)
- Single-action input capture (SAIC)
- Single-action output compare (SAOC)
- Output pulse-width modulation buffered (OPWMB)
- Input period measurement (IPM)
- Input pulse-width measurement (IPWM)
- Double-action output compare (DAOC)
- Modulus counter buffered (MCB)
- Output pulse width and frequency modulation buffered (OPWFMB)

1.5.11 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, the eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High-level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

SPC564A80 devices feature the second generation of the eTPU, called eTPU2. Enhancements of the eTPU2 over the standard eTPU include:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.

include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    12-bit conversion time: 938 ns (1 M sample/sec)
    10-bit conversion time: 813 ns (1.2 M sample/second)
    8-bit conversion time: 688 ns (1.4 M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 8-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports four external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 Decimation Filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients

1.5.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.16 FlexCAN

The SPC564A80 MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

2.2 LBGA208 ballmap

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS3	DSPI_B_SIN	DSPI_B_PCS0	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_PCS4	DSPI_B_PCS2	DSPI_B_PCS1	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS5	SCI_A_TX	GPIO98	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS(1)	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO206	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO219	MDO9_ETPUA25_O	EMIOS13	EMIOS15	MDO5_ETPUA4_O	MDO6_ETPUA13_O	CAN_B_TX	VDDE5	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1. This pin (N13) should be tied low.

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR21 FR_B_RX DATA21 GPIO[17]	External address bus Flexray RX data channel B External data bus GPIO	P A1 A2 G	001 010 100 000	17	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T2
ADDR22 DATA22 GPIO[18]	External address bus External data bus GPIO	P A2 G	001 100 000	18	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U1
ADDR23 DATA23 GPIO[19]	External address bus External data bus GPIO	P A2 G	001 100 000	19	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	U2
ADDR24 DATA24 GPIO[20]	External address bus External data bus GPIO	P A2 G	001 100 000	20	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V1
ADDR25 DATA25 GPIO[21]	External address bus External data bus GPIO	P A2 G	001 100 000	21	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V2
ADDR26 DATA26 GPIO[22]	External address bus External data bus GPIO	P A2 G	001 100 000	22	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	W1
ADDR27 DATA27 GPIO[23]	External address bus External data bus GPIO	P A2 G	001 100 000	23	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	Y2
ADDR28 DATA28 GPIO[24]	External address bus External data bus GPIO	P A2 G	001 100 000	24	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	Y1
ADDR29 DATA29 GPIO[25]	External address bus External data bus GPIO	P A2 G	001 100 000	25	I/O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	AA1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAL_ADDR[28] CAL_DATA[28]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[29] CAL_DATA[29]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[30] CAL_DATA[30]	Calibration address bus Calibration data bus	P A	01 10	345	I/O I/O	VDDE12 Fast		— / —	—	—	—
CAL_DATA[0]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[1]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[2]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[3]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[4]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[5]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[6]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[7]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[8]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[9]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—
CAL_DATA[10]	Calibration data bus	P	01	341	I/O	VDDE12 Fast	— / Up	— / Up	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DSPI_A_SOUT[17] DSPI_C_PCS[5] GPIO[95]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	95	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	L20
DSPI_A_PCS[0][17] DSPI_D_PCS[2] GPIO[96]	— DSPI D peripheral chip select GPIO	— A1 G	— 10 00	96	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	M20
DSPI_A_PCS[1][17] DSPI_B_PCS[2] GPIO[97]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	97	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	M19
CS[2] DSPI_D_SCK GPIO[98]	— SPI clock pin for DSPI module GPIO	— A1 G	— 10 00	98	— I/O I/O	VDDEH7 Medium	— / Up	— / Up	141	J15	M21
CS[3] DSPI_D_SIN GPIO[99]	— DSPI D data input GPIO	— A1 G	— 10 00	99	— I I/O	VDDEH7 Medium	— / Up	— / Up	142	H13	K19
DSPI_A_PCS[4][17] DSPI_D_SOUT GPIO[100]	— DSPI D data output GPIO	— A1 G	— 10 00	100	O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	N19
DSPI_A_PCS[5][17] DSPI_B_PCS[3] GPIO[101]	— DSPI B peripheral chip select GPIO	— A1 G	— 10 00	101	O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	N21
DSPI_B_SCK DSPI_C_PCS[1] GPIO[102]	SPI clock pin for DSPI module DSPI C peripheral chip select GPIO	P A1 G	01 10 00	102	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	106	J16	K21
DSPI_B_SIN DSPI_C_PCS[2] GPIO[103]	DSPI B data input DSPI C peripheral chip select GPIO	P A1 G	01 10 00	103	I O I/O	VDDEH6 Medium	— / Up	— / Up	112	G15	H22

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field [3]	PCR [4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN26	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[26] / —	—	—	B12
AN27	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[27] / —	157	A10	A12
AN28	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[28] / —	156	B10	A13
AN29	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[29] / —	—	—	D13
AN30	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[30] / —	155	D9	C13
AN31	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[31] / —	154	D10	B13
AN32	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[32] / —	153	C10	B14
AN33	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[33] / —	152	C11	C14
AN34	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[34] / —	151	C5	D14
AN35	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[35] / —	150	D11	A14
AN36	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[36] / —	174	F4	B4
AN37	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[37] / —	175	E3	A4
AN38	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[38] / —	—	—	C5
AN39	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[39] / —	8	D2	B5

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 Analog	—	—	93	P16	V22
EXTAL EXTCLK	Crystal oscillator input External clock input	P A	01 10	—	I	VDDEH6 Analog	—	—	92	N16	U22
CLKOUT	System clock output	P	01	229	O	VDDE5 Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE5 Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage Regulator Supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage Regulator Control Output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[20]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—		3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	—	—
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	—	—
VDDA0[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA0	—	B11	A6
VSSA0[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA0	—	A11	A7
VDDA1[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA1	—	A4	C15
VSSA1[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA1	—	A5	A15, B15
VDDPLL	FMPLL Supply Voltage	—		—	I	1.2	I / —	VDDPLL	91	R16	W22
VSTBY	Power Supply for Standby RAM	—		—	I	0.9 V - 6 V	I / —	VSTBY	12	C1	A3

Table 5. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV(1),(2)	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1. Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.
2. VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 6. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	SPC564A80 clock output for the external/calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode. On the 324BGA package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with previous devices . For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected. 1: XTAL oscillator mode is selected For the 324 ball BGA package: If RSTCFG is 0: 0: External reference clock is selected. 1: XTAL oscillator mode is selected. If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS- DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS- DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission

Table 6. Signal details (continued)

Signal	Module or Function	Description
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base
CAN_A_TX CAN_B_TX CAN_C_TX	FlexCan_A - FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_B_RX CAN_C_RX	FlexCAN_A - FlexCAN_C	FlexCAN receive
FR_A_RX FR_B_RX	FlexRay	FlexRay receive (Channels A, B)
$\overline{\text{FR\_A\_TX\_EN}}$ $\overline{\text{FR\_B\_TX\_EN}}$	FlexRay	FlexRay transmit enable (Channels A, B)
FR_A_TX FR_B_TX	FlexRay	Flexray transmit (Channels A, B)
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test logic.
$\overline{\text{EVTI}}$	Nexus	$\overline{\text{EVTI}}$ is an input that is read on the negation of $\overline{\text{RESET}}$ to enable or disable the Nexus Debug port. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program synchronization messages or generate a breakpoint.
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[0:11](1)	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[0:1](1)	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
$\overline{\text{RDY}}$	Nexus	Nexus Ready Output ($\overline{\text{RDY}}$) is an output that indicates to the development tools the data is ready to be read from or written to the Nexus read/write access registers.

Table 6. Signal details (continued)

Signal	Module or Function	Description
BOOTCFG[0:1]	SIU - Configuration	Two BOOTCFG signals are implemented in SPC564A80 MCUs. The BAM program uses the BOOTCFG0 bit to determine where to read the reset configuration word, and whether to initiate a FlexCAN or eSCI boot. The BOOTCFG1 pin is sampled during the assertion of the RSTOUT signal, and the value is used to update the RSR and the BAM boot mode See the *SPC564A80 Microcontroller Reference Manual* for more information. The following values are for BOOTCFG[0:1}: 00:Boot from internal flash memory 01:FlexCAN/eSCI boot 10:Boot from external memory using EBI 11:Reserved Note: For the 176-pin QFP and 208-ball BGA packages BOOTCFG[0] is always 0 since the EBI interface is not available.
WKPCFG	SIU - Configuration	The WKPCFG pin is applied at the assertion of the internal reset signal (assertion of $\overline{\text{RSTOUT}}$), and is sampled 4 clock cycles before the negation of the $\overline{\text{RSTOUT}}$ pin. The value is used to configure whether the eTPU and eMIOS pins are connected to internal weak pull up or weak pull down devices after reset. The value latched on the WKPCFG pin at reset is stored in the Reset Status Register (RSR), and is updated for all reset sources except the Debug Port Reset and Software External Reset. 0:Weak pulldown applied to eTPU and eMIOS pins at reset 1:Weak pullup applied to eTPU and eMIOS pins at reset.
ETRIG[2:3]	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[206] ETRIG0 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx
GPIO[207] ETRIG1 (Input)	SIU - eQADC Triggers	External signal eTRIGx triggers eQADC CFIFOx

3.2 Maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage(2)		–0.3	1.32	V
V_{FLASH}	SR	Flash core voltage(3),(4)		–0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage(5)		–0.3	6	V
V_{DDPLL}	SR	Clock synthesizer voltage		–0.3	1.32	V
V_{RC33}	SR	Voltage regulator control input voltage(4)		–0.3	3.6	V
V_{DDA}	SR	Analog supply voltage(5)	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage(4),(6)		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage(5)		–0.3	5.5	V
V_{IN}	SR	DC input voltage(7)	V_{DDEH} powered I/O pads	–1.0(8)	V_{DDEH} + 0.3 V(9)	V
			V_{DDE} powered I/O pads	–1.0(10)	V_{DDE} + 0.3 V(10)	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current(11)	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current(12)	Per pin, applies to all analog pins	—	5	mA

Table 9. Absolute maximum ratings(1) (continued)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
T_J	SR	Maximum operating temperature range - die junction temperature		–40.0	150.0	°C
T_{STG}	SR	Storage temperature range		–55.0	150.0	°C
T_{SDR}	SR	Maximum solder temperature(13)		—	260.0	°C
MSL	SR	Moisture sensitivity level(14)		—	3	

1. Functional operating conditions are given in the DC electrical specifications. Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the listed maxima may affect device reliability or cause permanent damage to the device.
2. Allowed 2 V for 10 hours cumulative time, remaining time at 1.2 V +10%.
3. The V_{FLASH} supply is connected to V_{RC33} in the package substrate. This specification applies to calibration package devices only.
4. Allowed 5.3 V for 10 hours cumulative time, remaining time at 3.3 V +10%.
5. Allowed 5.9 V for 10 hours cumulative time, remaining time at 5 V +10%.
6. All functional non-supply I/O pins are clamped to V_{SS} and V_{DDE}, or V_{DDEH}.
7. AC signal overshoot and undershoot of up to 2.0 V of the input voltages is permitted for an accumulative duration of 60 hours over the complete lifetime of the device (injection current not limited for this duration).
8. Internal structures hold the voltage greater than –1.0 V if the injection current limit of 2 mA is met.
9. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDEH} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDEH} is within the operating voltage specifications.
10. Internal structures hold the input voltage less than the maximum voltage on all pads powered by V_{DDE} supplies, if the maximum injection current specification is met (2 mA for all pins) and V_{DDE} is within the operating voltage specifications.
11. Total injection current for all pins (including both digital and analog) must not exceed 25 mA.
12. Total injection current for all analog input pins must not exceed 15 mA.
13. Solder profile per IPC/JEDEC J-STD-020D.
14. Moisture sensitivity per JEDEC test method A112.

3.3 Thermal characteristics

Table 10. Thermal characteristics for 176-pin QFP(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Single layer board - 1s	38	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board - 2s2p	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	200 ft./min., single layer board - 1s	30	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., four layer board - 2s2p	25	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board(3)		20	°C/W

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
$I_{DDSTBY150}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 150 °C	—	790	2000	µA
		P	Operating current 2–5.5 V	V_{STBY} at 150 °C	—	760	2000	µA
I_{DDSLOW} I_{DDSTOP}	CC	P	V_{DD} low-power mode operating current at 1.32 V	Slow mode(10)	—		191	mA
		P		Stop mode(11)	—		190	
I_{DD33}	CC	C	Operating current 3.3 V supplies	V_{RC33}(1),(12)	—		60	mA
I_{DDA} I_{REF} I_{DDREG}	CC	P	Operating current 5.0 V supplies	V_{DDA}	—	—	30.0	mA
		P		Analog reference supply current (transient)	—	—	1.0	
		C		V_{DDREG}	—	—	70(13)	
I_{DDH1} I_{DDH4} I_{DDH6} I_{DDH7} I_{DD7} I_{DDH9} I_{DD12}	CC	D	Operating current V_{DDE}(14) supplies	V_{DDEH1}	—	—	See note (14)	mA
		D		V_{DDEH4}	—	—		
		D		V_{DDEH6}	—	—		
		D		V_{DDEH7}	—	—		
		D		V_{DDE7}	—	—		
		D		V_{DDEH9}	—	—		
		D		V_{DDE12}	—	—		
I_{ACT_S}	CC	C	Slow/medium I/O weak pull up/down current(15)	3.0 V – 3.6 V	15	—	95	µA
		P		4.75 V – 5.5 V	35	—	200	
I_{ACT_F}	CC	D	Fast I/O weak pull up/down current(15)	1.62 V – 1.98 V	36	—	120	µA
		D		2.25 V – 2.75 V	34	—	139	
		D		3.0 V – 3.6 V	42	—	158	
$I_{ACT\_MV\_PU}$	CC	C	Multi-voltage pad weak pullup current	V_{DDE}= 3.0–3.6 V(5), MultiV pad, high swing mode only	10	—	75	µA
		P		4.75 V – 5.25 V	25	—	200	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
R_{PUPD5K}	SR	C	Weak Pull-Up/Down Resistance(20), 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
$R_{PUPDMTCH}$	CC	C	Pull-up/Down Resistance matching ratios (100K/200K)	Pull-up and pull-down resistances both enabled and settings are equal.	–2.5	—	2.5	%
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0		125.0	°C
—	SR	—	Slew rate on power supply pins	—	—		25	V/ms

1. These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).
2. ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no undesirable behavior, but the accuracy will be degraded.
3. The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.
4. V_{FLASH} is only available in the calibration package.
5. Power supply for multi-voltage pads cannot be below 4.5 V when in low-swing mode.
6. The slew rate (SRC) setting must be 0b11 when in low-swing mode.
7. While in low-swing mode there are no restrictions in transitioning to high-swing mode.
8. Pin in low-swing mode can accept a 5 V input.
9. All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where noted.
10. Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels 1 kHz, all other modules stopped.
11. Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.
12. This current will be consumed for external regulation and internal regulation, when 3.3V regulator is switched off by shadow flash
13. If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

    If supply is external that is 3.3V internal regulator is off, then iddreg=15mA
14. Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See *Table 22* for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
15. Absolute value of current, measured at V_{IL} and V_{IH}.
16. Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to fast, slow, and medium pads.
17. Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.
18. Applies to CLKOUT, external bus pins, and Nexus pins.
19. Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.
20. This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from *Table 22* based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 22*.

Table 22. I/O pad average I_{DDE} specifications(1)

Pad Type	Symbol		C	Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.5	11	3.4	—

1. Numbers from simulations at best case process, 150 °C.
2. All loads are lumped.
3. Average current is for pad configured as output only.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1),(2)

Max. Flash Operating Frequency (MHz)(3)	APC(4)	RWSC(4)	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. TBD: To Be Defined.
3. Max frequencies including 2% PLL FM.
4. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	45	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	55	160(4)	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	300	1000	5000	ms

5 Ordering information

Table 55 shows the orderable part numbers for the SPC564A80 series.

Table 55. Order codes

Order code	Flash/SRAM	Package	Speed (MHz)
SPC564A74L7CFA	3 MB/160 KB	176LQFP	150
SPC564A74B2CFA	3 MB/160 KB	208LBGA	150
SPC564A74B4CFA	3 MB/160 KB	324PBGA	150
SPC564A80L7CFC	4 MB/192 KB	LQFP176	80
SPC564A80B2CFC	4 MB/192 KB	LBGA208	80
SPC564A80B4CFC	4 MB/192 KB	PBGA324	80
SPC564A80L7CFB	4 MB/192 KB	LQFP176	120
SPC564A80B2CFB	4 MB/192 KB	LBGA208	120
SPC564A80B4CFB	4 MB/192 KB	PBGA324	120
SPC564A80L7CFA	4 MB/192 KB	LQFP176	150
SPC564A80B2CFA	4 MB/192 KB	LBGA208	150
SPC564A80B4CFA	4 MB/192 KB	PBGA324	150
SPC564A80H1EFA	4 MB/192 KB	KGD	150

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010	3	Internal release. Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: – WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) – WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: – CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) – CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) – CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: – AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball). AN[8] was on C5 (324-ball) on previous devices. AN[38] Is now on C5 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball) on previous devices. – ANZ function added to AN11 pin Reaction channels added to eTPU2: – RCH0_A (A3) added to ETPU_A[14] (PCR 128) – RCH0_B (A2) added to ETPU_A[20] (PCR 134) – RCH0_C (A2) added to ETPU_A[21] (PCR 135) – RCH1_A (A2) added to ETPU_A[15] (PCR 129) – RCH1_B (A2) added to ETPU_A[9] (PCR 123) – RCH1_C (A2) added to ETPU_A[10] (PCR 124) – RCH2_A (A2) added to ETPU_A[16] (PCR 130) – RCH3_A (A2) added to ETPU_A[17] (PCR 131 – RCH4_A (A2) added to ETPU_A[18] (PCR 132)) – RCH4_B (A2) added to ETPU_A[11] (PCR 125) – RCH4_C (A2) added to ETPU_A[12] (PCR 126) – RCH5_A (A2) added to ETPU_A[19] (PCR 133) – RCH5_B (A2) added to ETPU_A[28] (PCR 142) – RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: – RCH2_B (A2) added to EMIOS[2] (PCR 181) – RCH2_C (A2) added to EMIOS[4] (PCR 183) – RCH3_B (A2) added to EMIOS[10] (PCR 189) – RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: – ETPUA16 (PCR 130) has Medium (was Slow) pad – ETPUA17 (PCR 131) has Medium (was Slow) pad – ETPUA18 (PCR 132) has Medium (was Slow) pad – ETPUA19 (PCR 133) has Medium (was Slow) pad – ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads