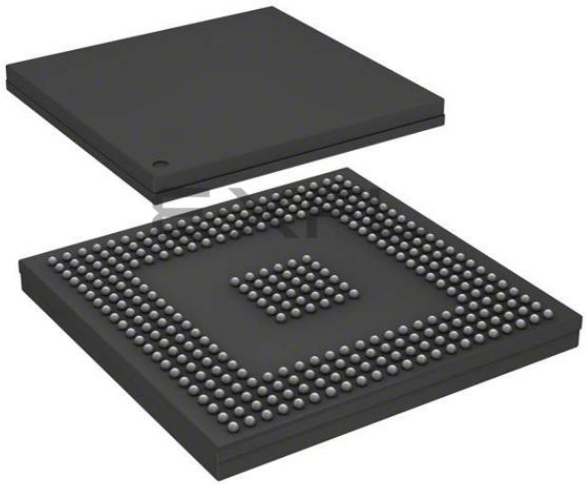

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80b4cfay

List of figures

GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z4 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - Centralized control of I/O and bus pins
  - Virtual GPIO via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

1.5.8 Flash memory

The SPC564A80 provides up to 4 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used to store instructions or data, or both. The flash module includes a Fetch Accelerator that optimizes the performance of the flash array to match the CPU architecture. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and 128- and 256-bit read data interfaces to flash memory. The module contains a prefetch controller which prefetches sequential lines of data from the flash array into the buffers. Prefetch buffer hits allow no-wait responses.

The flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch Accelerator
  - Architected to optimize the performance of the flash
  - Configurable read buffering and line prefetch support

1.5.17 FlexRay

The SPC564A80 includes one dual-channel FlexRay module that implements the FlexRay Communications System Protocol Specification, Version 2.1 Rev A. Features include:

- Single channel support
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 message buffers, each configurable as:
  - Receive message buffer
  - Single buffered transmit message buffer
  - Double buffered transmit message buffer (combines two single buffered message buffer)
- 2 independent receive FIFOs
  - 1 receive FIFO per channel
  - Up to 255 entries for each FIFO
- ECC support

1.5.18 System timers

The system timers include two distinct types of system timer:

- Periodic interrupts/triggers using the Periodic Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

Periodic interrupt timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to provide system 'tick' signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock and one is clocked by the crystal clock. This one channel is also referred to as Real-Time Interrupt (RTI) and is used to wake up the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered; used to restart system clock after predefined time-out period
- Each channel optionally able to generate an interrupt request or a trigger event (to trigger eQADC queues) when timer reaches zero

System timer module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR[(b)]. It consists of a single 32-bit counter, clocked by the system clock,

b. AUTOSAR: AUTomotive Open System ARchitecture (see www.autosar.org)

and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.19 Software watchdog timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.20 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC features:

- Support for CRC-16-CCITT (x25 protocol):
  - $X^{16} + X^{12} + X^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.21 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	C1
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	C2
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AB10
EMIOS1 ETPUA1_O[8] GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 Slow	— / Up	— / Up	64	T5	AB11
EMIOS2 ETPUA2_O[8] RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	65	N7	W12
EMIOS3 ETPUA3_O[8] GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	66	R6	AA11
EMIOS4 ETPUA4_O[8] RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	67	R5	AB12

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field (3)	PCR (4)	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDEH7B	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4,W19, Y3, Y20, AA2, AA21, AB1, AB22

1. For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.
2. The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.
3. The Pad Configuration Register (PCR) PA field is used by software to select pin function.
4. Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.
5. The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (-10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/- 10%).
6. See *Table 5* for details on pad types.

7. The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. Terminology is O - output, I - input, Up - weak pull up enabled, Down - weak pull down enabled, Low - output driven low, High - output driven high. A dash for the function in this column denotes that both the input and output buffer are turned off. The signal name to the left or right of the slash indicates the pin is enabled.
8. Output only.
9. When used as ETRIG, this pin must be configured as an input. For GPIO it can be configured either as an input or output.
10. Maximum frequency is 50 kHz.
11. The SIU_PCR219 register is unusual in that it controls pads for two separate device pins: GPIO[219] and MCKO. See the SPC564A80 Microcontroller Reference Manual (SIU chapter) for details.
12. Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.
13. On LQFP176 and LBGA208 packages, this pin is tied low internally.
14. Nexus multivoltage pads default to 5 V operation until the Nexus module is enabled.
15. $\overline{\text{EVTO}}$ should be clamped to 3.3 V to prevent possible damage to external tools that only support 3.3 V.
16. Do not connect pin directly to a power supply or ground.
17. This signal name is used to support legacy naming.
18. During and just after POR negates, internal pull resistors can be enabled, resulting in as much as 4 mA of current draw. The pull resistors are disabled when the system clock propagates through the device.
19. For pins AN12-AN15, if the analog features are used the VDDEH7 input pins should be tied to VDDA because that segment must meet the VDDA specification to support analog input function.
20. Do not use VRC33 to drive external circuits.
21. VDDA0 and VDDA1 are shorted together internally in BGA packages. In the QFP package the two pads are double bonded on one pin called VDDA.
22. VSSA0 and VSSA1 are shorted together internally in BGA packages. In the QFP package the two pads are double bonded on one pin called VSSA.
23. VDDE2 and VDDE3 are shorted together in all production packages.
24. VDDE2 and VDDE3 are shorted together in all production packages.
25. VDDEH1A, VDDEH1B, and VDDEH1AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.
26. VDDEH4, VDDEH4A, VDDEH4B, and VDDEH4AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.
27. VDDEH6, VDDEH6A, VDDEH6B, and VDDEH6AB are shorted together in all production packages. The separation of the signal names is present to support legacy naming, however they should be considered as the same signal in this document.

Table 6. Signal details (continued)

Signal	Module or Function	Description
RD_$\overline{WR}$	EBI	RD_$\overline{WR}$ indicates whether the current transaction is a read access or a write access.
$\overline{TA}$	EBI	$\overline{TA}$ is asserted to indicate that the slave has received the data (and completed the access) for a write cycle, or returned data for a read cycle. If the transaction is a burst read, $\overline{TA}$ is asserted for each one of the transaction beats. For write transactions, $\overline{TA}$ is only asserted once at access completion, even if more than one write data beat is transferred.
$\overline{TS}$	EBI	The Transfer Start signal ($\overline{TS}$) is asserted by the SPC564A80 to indicate the start of a transfer.
$\overline{WE}$[2:3]	EBI	Write enables are used to enable program operations to a particular memory. $\overline{WE}$[2:3] are only asserted for write accesses
$\overline{WE}$[0:3]/$\overline{BE}$[0:3]	EBI	Write enables are used to enable program operations to a particular memory. These signals can also be used as byte enables for read and write operation by setting the WEBS bit in the appropriate EBI Base Register (EBI_BR*n*). $\overline{WE}$[0:3] are only asserted for write accesses. $\overline{BE}$[0:3] are asserted for both read and write accesses
eMIOS[0:23]	eMIOS	eMIOS I/O channels
AN[0:39]	eQADC	Single-ended analog inputs for analog-to-digital converter
FCK	eQADC	eQADC free running clock for eQADC SSI.
MA[0:2]	eQADC	These three control bits are output to enable the selection for an external Analog Mux for expansion channels.
REFBYPC	eQADC	Bypass capacitor input
SDI	eQADC	Serial data in
SDO	eQADC	Serial data out
SDS	eQADC	Serial data select
VRH	eQADC	Voltage reference high input
VRL	eQADC	Voltage reference low input
SCI_A_RX SCI_B_RX SCI_C_RX	eSCI_A - eSCI_C	eSCI receive
SCI_A_TX SCI_B_TX SCI_C_TX	eSCI_A - eSCI_C	eSCI transmit
ETPU_A[0:31]	eTPU	eTPU I/O channel

Table 6. Signal details (continued)

Signal	Module or Function	Description
$\overline{\text{IRQ}}$[0:5] $\overline{\text{IRQ}}$[7:15]	SIU - External Interrupts	The $\overline{\text{IRQ}}$[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the $\overline{\text{IRQ}}$[0:15] pins as inputs to the IRQs. See the *SPC564A80 Microcontroller Reference Manual* for more information.
$\overline{\text{NMI}}$	SIU - External Interrupts	Non-Maskable Interrupt
GPIO[0:3] GPIO[8:43] GPIO[62:65] GPIO[68:70] GPIO[75:145] GPIO[179:204] GPIO[208:213] GPIO[219] GPIO[244:245]	SIU - GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pins is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See The *SPC564A80 Microcontroller Reference Manual* for more information. –
$\overline{\text{RESET}}$	SIU - Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU - Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0:Get configuration information from BOOTCFG[0:1] and PLLREF 1:Use default configuration of booting from internal flash with crystal clock source For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.
$\overline{\text{RSTOUT}}$	SIU - Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the RSTOUT pin.

1. Do not connect pin directly to a power supply or ground.

board. This model can be used to generate simple estimations and for computational fluid dynamics (CFD) thermal models.

To determine the junction temperature of the device in the application on a prototype board, use the thermal characterization parameter (Ψ_{JT}) to determine the junction temperature by measuring the temperature at the top center of the package case using the following equation:

Equation 4 $T_J = T_T + (\Psi_{JT} \times P_D)$

where:

T_T = thermocouple temperature on top of the package (^oC)

Ψ_{JT} = thermal characterization parameter ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured in compliance with the JESD51-2 specification using a 40-gauge type T thermocouple epoxied to the top center of the package case. Position the thermocouple so that the thermocouple junction rests on the package. Place a small amount of epoxy on the thermocouple junction and approximately 1 mm of wire extending from the junction. Place the thermocouple wire flat against the package case to avoid measurement errors caused by the cooling effects of the thermocouple wire.

References:

Semiconductor Equipment and Materials International

3081 Zanker Road
San Jose, CA 95134
USA
(408) 943-6900

MIL-SPEC and EIA/JESD (JEDEC) specifications are available from Global Engineering Documents at 800-854-7179 or 303-397-7956.

JEDEC specifications are available on the WEB at http://www.jedec.org.

- C.E. Triplett and B. Joiner, “An Experimental Characterization of a 272 PBGA Within an Automotive Engine Controller Module,” Proceedings of SemiTherm, San Diego, 1998, pp. 47-54.
- G. Kromann, S. Shidore, and S. Addison, “Thermal Modeling of a PBGA for Air-Cooled Applications”, Electronic Packaging and Production, pp. 53-58, March 1998.
- B. Joiner and V. Adams, “Measurement and Simulation of Junction to Board Thermal Resistance and Its Application in Thermal Modeling,” Proceedings of SemiTherm, San Diego, 1999, pp. 212-220.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from *Table 22* based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 22*.

Table 22. I/O pad average I_{DDE} specifications(1)

Pad Type	Symbol		C	Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.5	11	3.4	—

1. Numbers from simulations at best case process, 150 °C.
2. All loads are lumped.
3. Average current is for pad configured as output only.

5. f_{VCO} self clock range is 20–150 MHz. f_{SCM} represents f_{SYS} after PLL output divider (ERFD) of 2 through 16 in enhanced mode.
6. This value is determined by the crystal manufacturer and board design.
7. Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{SYS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the C_{JITTER} percentage for a given interval.
8. Proper PC board layout procedures must be followed to achieve specifications.
9. Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{JITTER} and either f_{CS} or f_{DS} (depending on whether center spread or down spread modulation is enabled).
10. This value is determined by the crystal manufacturer and board design. For 4 MHz to 40 MHz crystals specified for this PLL, load capacitors should not exceed these limits.
11. Proper PC board layout procedures must be followed to achieve specifications.
12. This parameter is guaranteed by design rather than 100% tested.
13. V_{IHEXT} cannot exceed V_{RC33} in external reference mode.
14. This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
15. Modulation depth will be attenuated from depth setting when operating at modulation frequencies above 50 kHz.

3.11 Temperature sensor electrical characteristics

Table 27. Temperature sensor electrical characteristics

Symbol		C	Parameter	Conditions	Value			Unit
					min	typical	max	
—	CC	C	Temperature monitoring range		–40	—	150	°C
—	CC	C	Sensitivity		—	6.3	—	mV/°C
—	CC	P	Accuracy	T_J = –40 to 150 °C	–10	—	10	°C

3.12 eQADC electrical characteristics

Table 28. eQADC conversion specifications (operating)

Symbol		C	Parameter	Value		Unit
				min	max	
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	MHz
CC	CC	D	Conversion cycles	2+13	128+14	ADCLK cycles
T_{SR}	CC	C	Stop mode recovery time(1)	—	10	µs
f_{ADCLK}	SR	—	ADC clock (ADCLK) frequency	2	16	mV

1. Stop mode recovery time is the time from the setting of either of the enable bits in the ADC Control Register to the time that the ADC is ready to perform conversions.Delay from power up to full accuracy = 8 ms.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1),(2)

Max. Flash Operating Frequency (MHz)(3)	APC(4)	RWSC(4)	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. TBD: To Be Defined.
3. Max frequencies including 2% PLL FM.
4. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	45	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	55	160(4)	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	300	1000	5000	ms

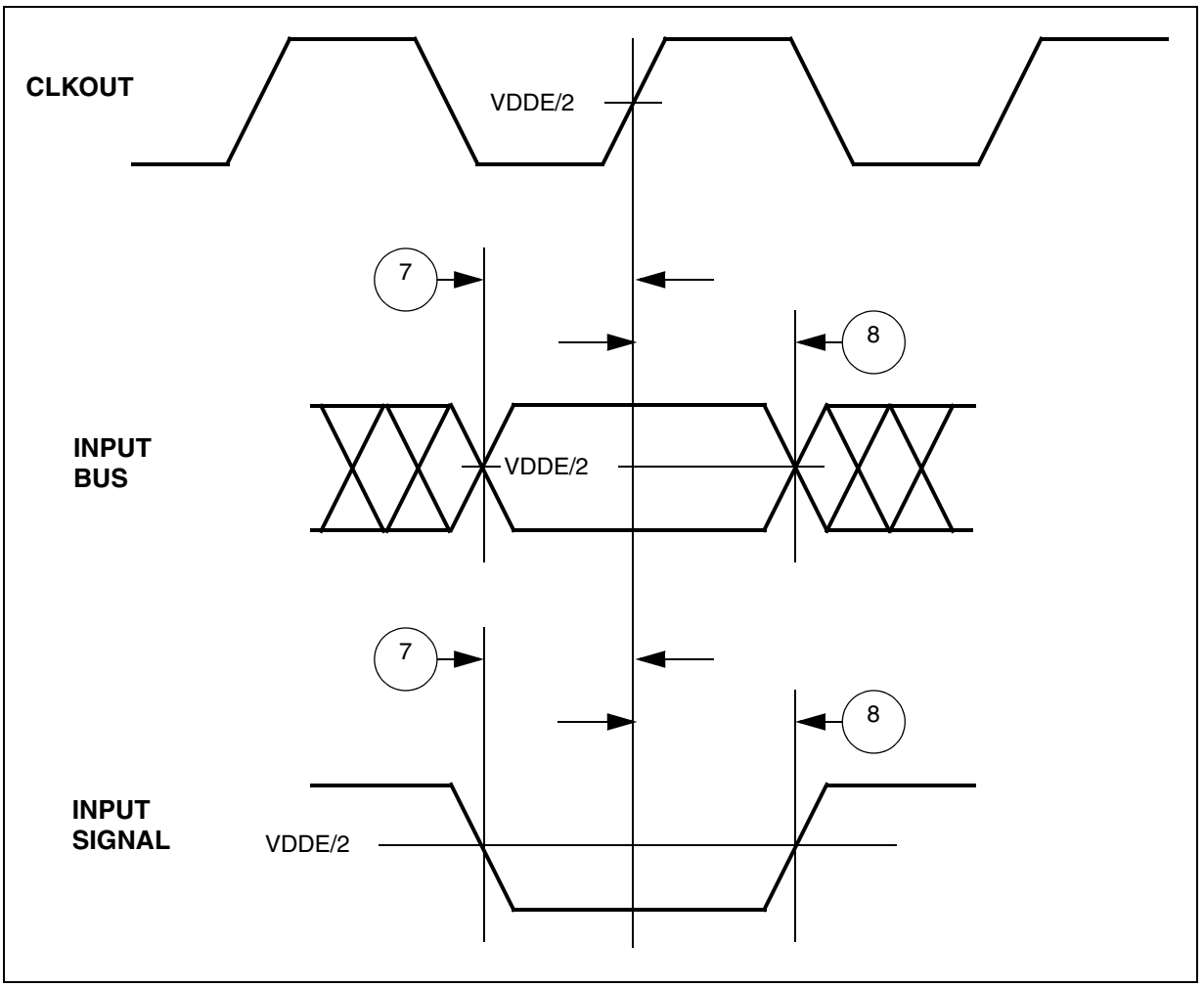


Figure 20. Synchronous input timing

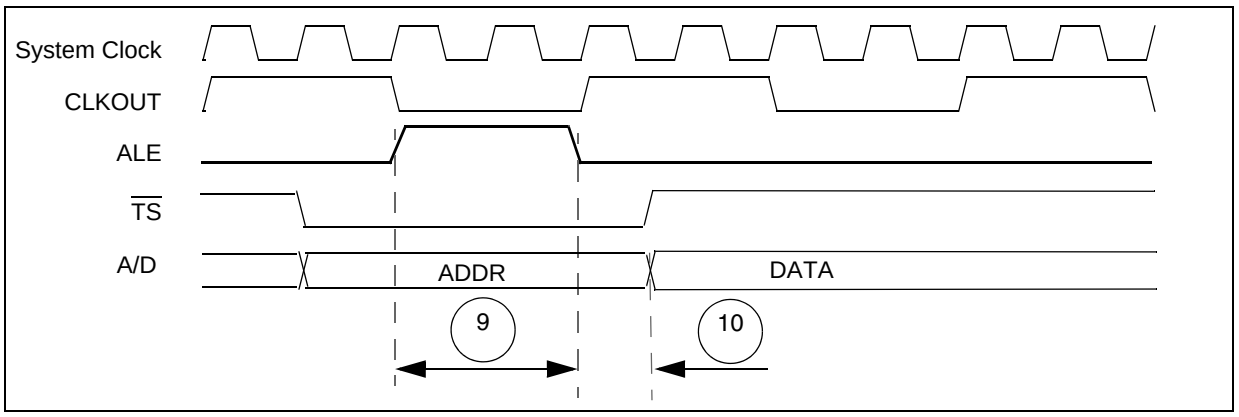
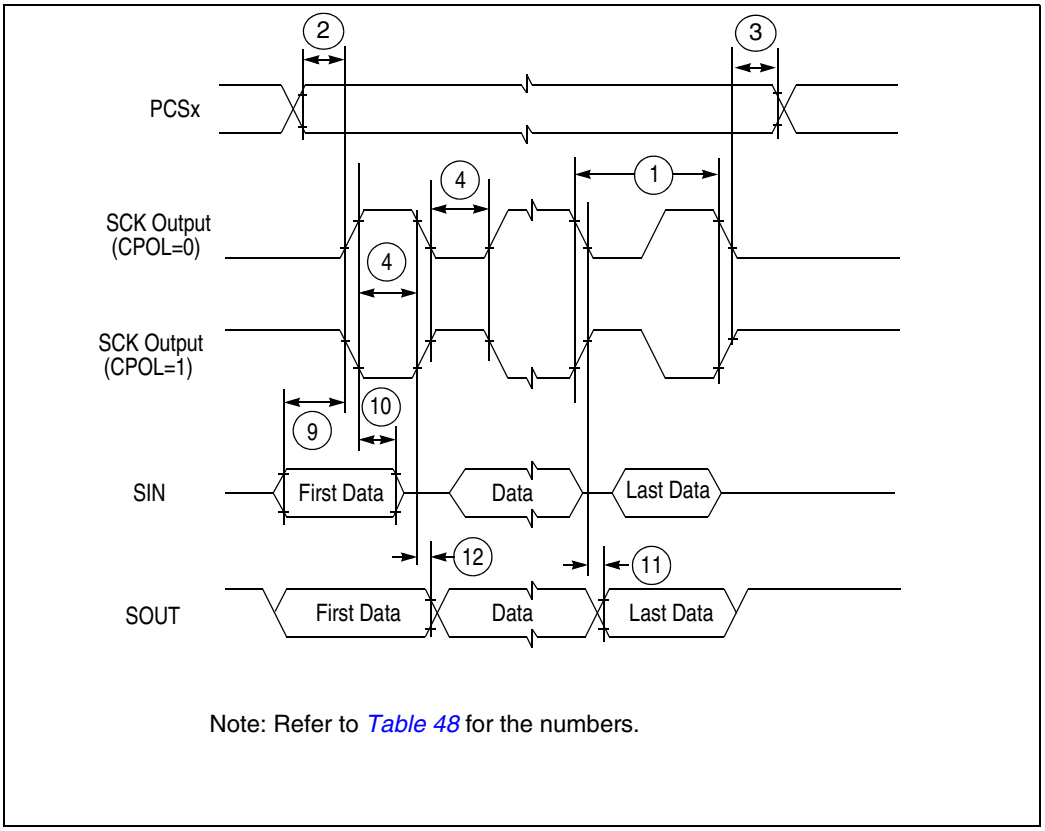


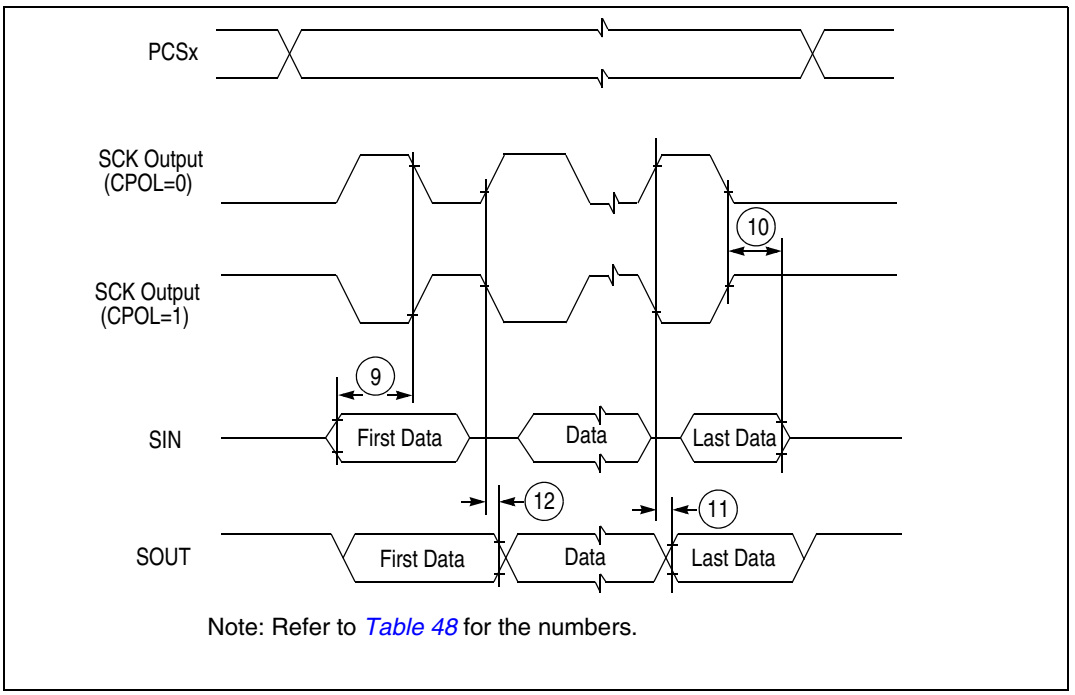
Figure 21. ALE signal timing

3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A80 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when pcssck = 3(01), and cssck =2 (0000).
8. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9. Timing met when ASC = 2 (0000), and PASC = 3 (01).
10. Timing met when pcssck = 3.
11. Timing met when ASC = 3.
12. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



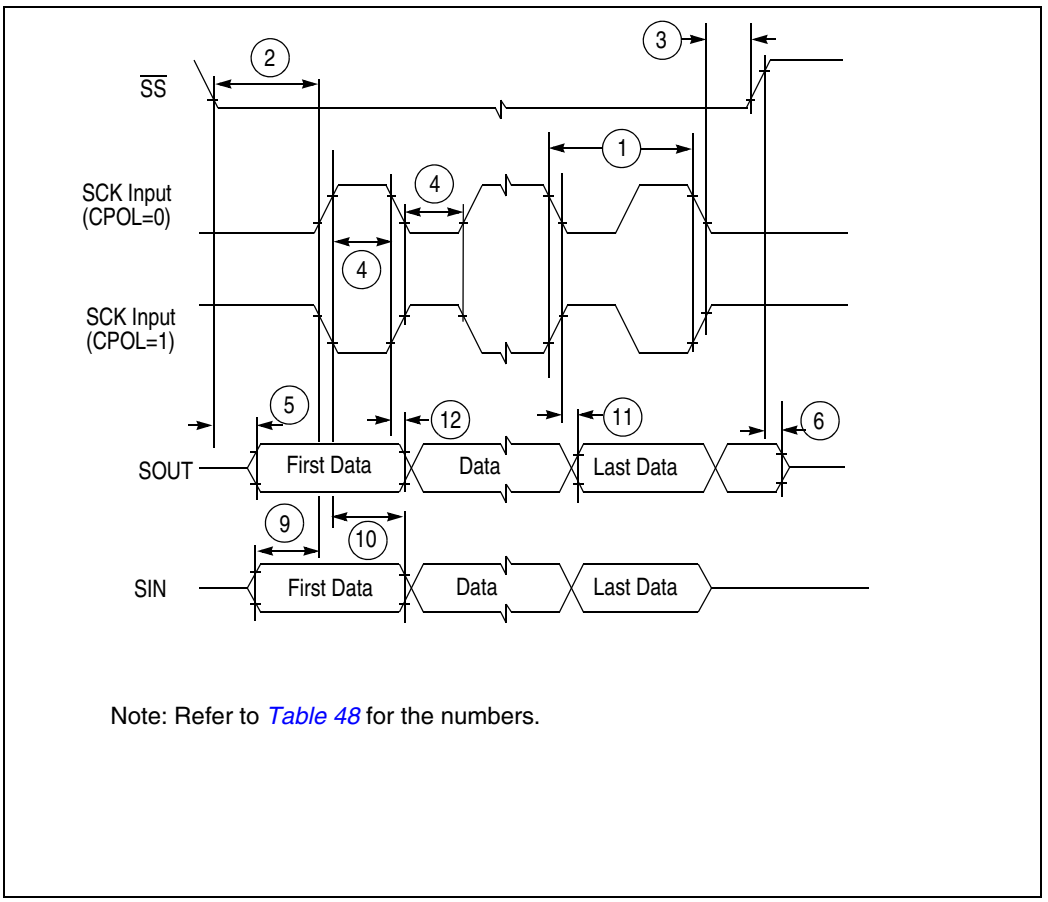
Note: Refer to *Table 48* for the numbers.

Figure 23. DSPI classic SPI timing — master, CPHA = 0



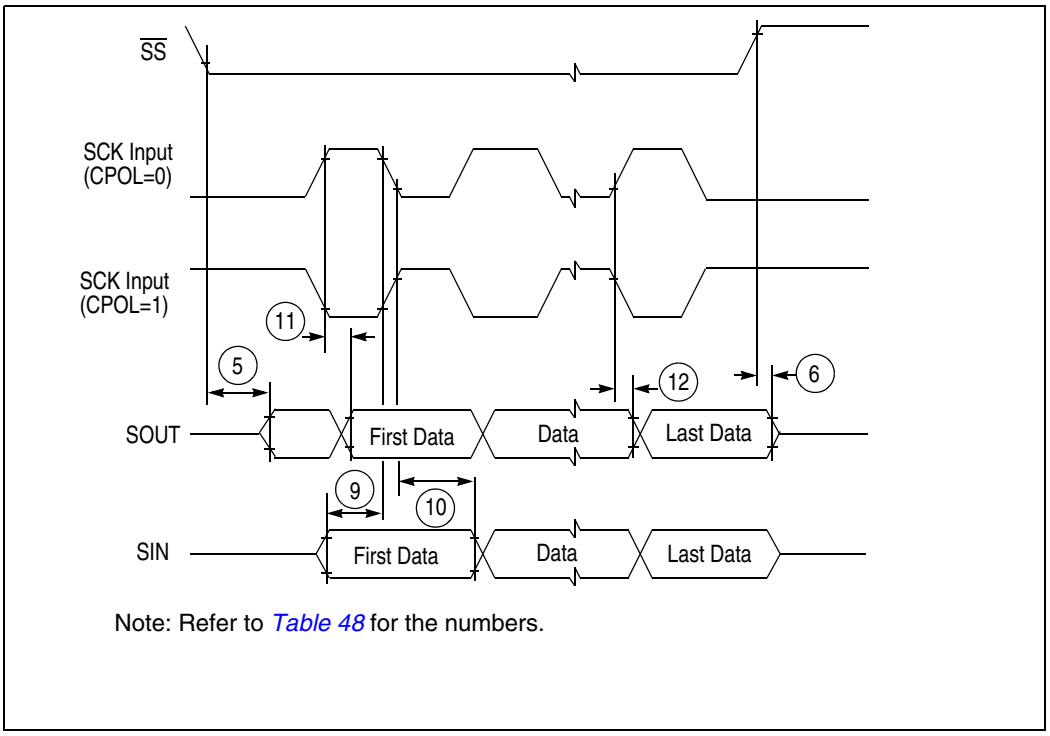
Note: Refer to *Table 48* for the numbers.

Figure 24. DSPI classic SPI timing — master, CPHA = 1



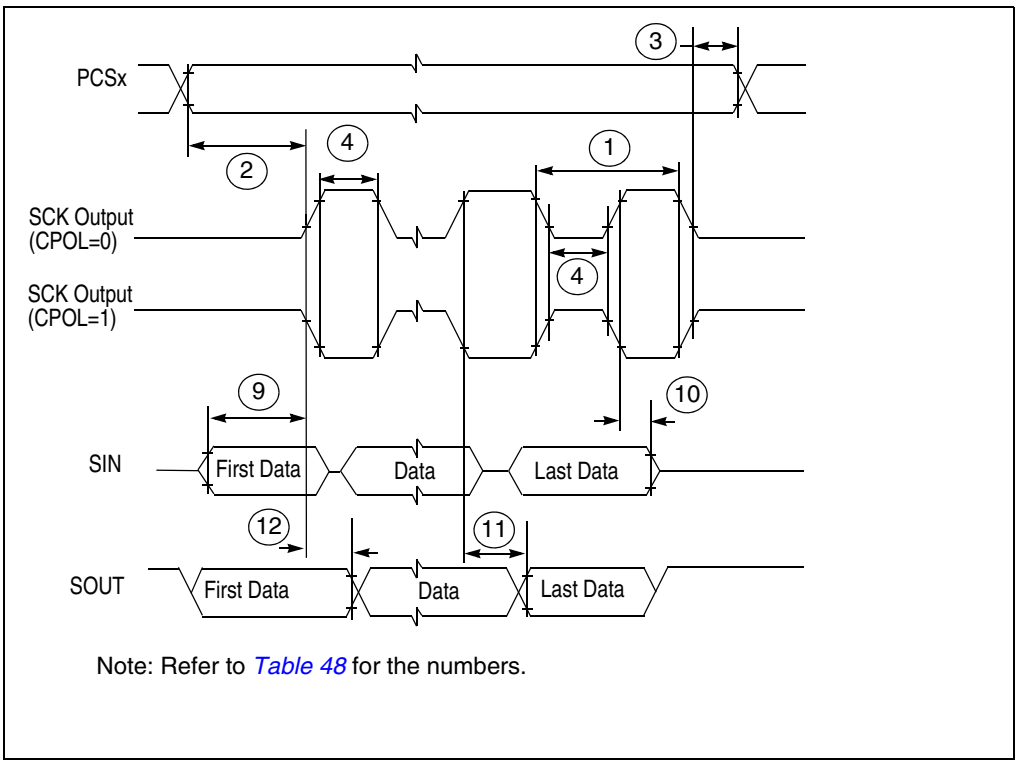
Note: Refer to *Table 48* for the numbers.

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Refer to *Table 48* for the numbers.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Refer to *Table 48* for the numbers.

6 Document revision history

Table 56. Revision history

Date	Revision	Changes
23-Feb-2009	1	Initial release
09-Dec-2009	2	Maximum device speed is 145 MHz (was 150 MHz) 16-entry Memory Protection Unit (MPU). Was incorrectly listed as 8-entry. 288-ball BGA package deleted Feature details section added Changes to signal summary table: – Added ANY function to AN[10] – Added ANW function to AN[8] Changes to 208 ball BGA ballmap: – A12 is AN12-SDS (was AN12) – A15 is VRC33 (was VDD33) – B12 is AN13-SDO (was AN13) – C12 is AN14SDI (was AN14) – C13 is AN15-FCK (was AN15) – D1 is VRC33 (was VDD33) – F13 is VDDEH6AB (was VDDEH6) – H13 is GPIO99 (was PCSA3) – J15 is GPIO98 (was PCSA2) – K4 is now VDDEH1AB (was VDDEH1) – N6 is now VRC33 (was VDD33) – N9 is VDDEH4AB (was VDDEH4) – N12 is now VRC33 (was VDD33) – P6 is now NC – T13 is VDDE5 (was NC) Changes to 324 ball BGA ballmap: – A6 is VDDA (was VDDA1) – A7 is VSSA (was VSSA1) – A15 is VSSA (was VSSA0) – A16 is AN12_SDS (was AN12) – A17 is MDO11_ETPUA29O (was MDO11) – A18 is MDO10_ETPUA27O (was MDO10) – A19 is MDO8_ETPUA21O (was MDO8) – A21 is VRC33 (was VDD33) – B1 is VRC33 (was VDD33) – B15 is VSSA (was VSSA0) – B16 is AN13_SDO (was AN13) – B17 is MDO9_ETPUA25O (was MDO9) – B18 is MDO7_ETPUA19O (was MDO7) – B19 is MDO4_ETPUA2O (was MDO4) – B22 is NIC (was VDDE7)

Table 56. Revision history (continued)

Date	Revision	Changes
10-Feb-2011 (cont)	5 (cont)	– Added DATA[0:15] to V_{DDE5} in the “signal properties” table. – Updated VSTBY parameters in the “Power/ground segmentation” table. – Updated the parameter symbols and classifications throughout the document. – Updated footnote instances in the “Absolute maximum ratings“ table. – Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. – Updated the format of the “EMI (electromagnetic interference) characteristics” table. – Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications“ table. – Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. – Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. – Removed the “VRC electrical specifications” table as it contained redundant information. – Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. – Updated V_{IH_LS} in the “DC electrical specifications” table. – Updated the V_{OH_LS} min value in the “DC electrical specifications” table. – Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. – Updated the I_{DDA}/I_{REF}/I_{DDREG} max value in the “DC electrical specifications” table. – Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. – Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. – Updated values for V_{OD} in the “DSPI LVDS pad specification“ table. – Removed the footnotes from the “DSPI LVDS pad specifications“ table. – Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. – Updated footnotes in the “PLLMRFM electrical specifications” table. – Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)“ table. – Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. – Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. – Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Updated the Typical values for $T_{dwprogram}$,, $T_{pprogram}$, and $T_{16kpperase}$, and updated the Initial Max values for $T_{128kpperase}$ and $T_{256kpperase}$ in the “Flash program and erase specifications” table. – Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. – Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)“ table.