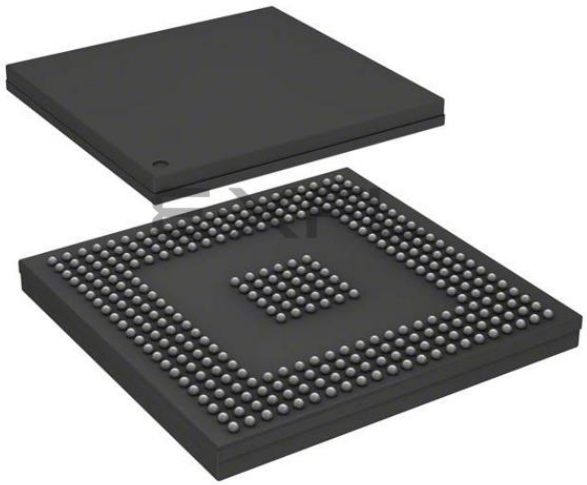

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80b4cfby

  - Four-entry 256-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (four words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by ST and is identical for all SPC564A80 MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on external bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC564A80 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture embedded category (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using standard protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or VLE code

  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Hardware implementation of four semaphores support coherent parameter sharing between both eTPU engines
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC - multiple input signature calculator), runs concurrently with eTPU2 normal operation

1.5.12 Reaction module

The reaction module provides the ability to modulate output signals to manage closed loop control without CPU assistance. It works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.

The reaction module has the following features:

- Six reaction channels
- Each channel output is a bus of three signals, providing ability to control 3 inputs.
- Each channel can implement a peak and hold waveform, making it possible to implement up to six independent peak and hold control channels

Target applications include solenoid control for direct injection systems and valve control in automatic transmissions

1.5.13 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features

include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The eQADC provides the following features:

- Dual on-chip ADCs
  - 2 × 12-bit ADC resolution
  - Programmable resolution for increased conversion speed (12-bit, 10-bit, 8-bit)
    12-bit conversion time: 938 ns (1 M sample/sec)
    10-bit conversion time: 813 ns (1.2 M sample/second)
    8-bit conversion time: 688 ns (1.4 M sample/second)
  - Up to 10-bit accuracy at 500 KSample/s and 8-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (×1, ×2, ×4)
  - Sample times of 2 (default), 8, 64 or 128 ADC clock cycles
  - Provides time stamp information when requested
  - Allows time stamp information relative to eTPU clock sources, such as an angle clock
  - Parallel interface to eQADC CFIFOs and RFIFOs
  - Supports both right-justified unsigned and signed formats for conversion results
- 40 single-ended input channels, expandable to 56 channels with external multiplexers (supports four external 8-to-1 muxes)
- 8 channels can be used as 4 pairs of differential analog input channels
- Differential channels include variable gain amplifier for improved dynamic range
- Differential channels include programmable pull-up and pull-down resistors for biasing and sensor diagnostics (200 kΩ, 100 kΩ, 5 kΩ)
- Additional internal channels for monitoring voltages (such as core voltage, I/O voltage, LVI voltages, etc.) inside the device
- An internal bandgap reference to allow absolute voltage measurements
- Silicon die temperature sensor
  - Provides temperature of silicon as an analog value
  - Read using an internal ADC analog channel
  - May be read with either ADC
- 2 Decimation Filters
  - Programmable decimation factor (1 to 16)
  - Selectable IIR or FIR filter
  - Up to 4th order IIR or 8th order FIR
  - Programmable coefficients

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A80.

The sources of the ECC errors are:

- Flash
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 Parameter RAM)

1.5.22 External bus interface (EBI)

The SPC564A80 device features an external bus interface that is available in PBGA324 and calibration packages.

The EBI supports operation at frequencies of system clock /1, /2 and /4, with a maximum frequency support of 80 MHz. Customers running the device at 120 MHz or 132 MHz will use the /2 divider, giving an EBI frequency of 60 MHz or 66 MHz. Customers running the device at 80 MHz will be able to use the /1 divider to have the EBI run at the full 80 MHz frequency.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller with support for various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing included to support 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The Calibration EBI is only available in the calibration tool.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

1.5.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the SPC564A80 Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

1.5.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

1.5.27 Development Trigger Semaphore (DTS)

SPC564A80 devices include a system development feature, the Development Trigger Semaphore (DTS) module, that enables software to signal an external tool by driving a persistent (affected only by reset or an external tool) signal on an external device pin. There

2 Pinout and signal description

This section contains the pinouts for all production packages for the SPC564A80 family of devices.

Caution: Any pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

2.2 LBGA208 ballmap

Figure 3. 208-pin LBGA package ballmap (viewed from above)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	AN9	AN11	VDDA1	VSSA1	AN1	AN5	VRH	VRL	AN27	VSSA0	AN12-SDS	MDO2	MDO0	VRC33	VSS	A
B	VDD	VSS	AN8	AN21	AN0	AN4	REFBYPC	AN22	AN25	AN28	VDDA0	AN13-SDO	MDO3	MDO1	VSS	VDD	B
C	VSTBY	VDD	VSS	AN17	AN34	AN16	AN3	AN7	AN23	AN32	AN33	AN14-SDI	AN15-FCK	VSS	MSEO0	TCK	C
D	VRC33	AN39	VDD	VSS	AN18	AN2	AN6	AN24	AN30	AN31	AN35	VDDEH7	VSS	TMS	EVTO	NC	D
E	ETPUA30	ETPUA31	AN37	VDD									NC	TDI	EVTI	MSEO1	E
F	ETPUA28	ETPUA29	ETPUA26	AN36									VDDEH6AB	TDO	MCKO	JCOMP	F
G	ETPUA24	ETPUA27	ETPUA25	ETPUA21			VSS	VSS	VSS	VSS			DSPI_B_SOUT	DSPI_B_PCS3	DSPI_B_SIN	DSPI_B_PCS0	G
H	ETPUA23	ETPUA22	ETPUA17	ETPUA18			VSS	VSS	VSS	VSS			GPIO99	DSPI_B_PCS4	DSPI_B_PCS2	DSPI_B_PCS1	H
J	ETPUA20	ETPUA19	ETPUA14	ETPUA13			VSS	VSS	VSS	VSS			DSPI_B_PCS5	SCI_A_TX	GPIO98	DSPI_B_SCK	J
K	ETPUA16	ETPUA15	ETPUA7	VDDEH1AB			VSS	VSS	VSS	VSS			CAN_C_TX	SCI_A_RX	RSTOUT	VDDREG	K
L	ETPUA12	ETPUA11	ETPUA6	TCRCLKA									SCI_B_TX	CAN_C_RX	WKPCFG	RESET	L
M	ETPUA10	ETPUA9	ETPUA1	ETPUA5									SCI_B_RX	PLLREF	BOOTCFG1	VSS	M
N	ETPUA8	ETPUA4	ETPUA0	VSS	VDD	VRC33	EMIOS2	EMIOS10	VDDEH4AB	EMIOS12	MDO7_ETPUA19_O	VRC33	VSS(1)	VRCCTL	NC	EXTAL	N
P	ETPUA3	ETPUA2	VSS	VDD	GPIO207	NC	EMIOS6	EMIOS8	MDO11_ETPUA29_O	MDO4_ETPUA2_O	MDO8_ETPUA21_O	CAN_A_TX	VDD	VSS	NC	XTAL	P
R	NC	VSS	VDD	GPIO206	EMIOS4	EMIOS3	EMIOS9	EMIOS11	EMIOS14	MDO10_ETPUA27_O	EMIOS23	CAN_A_RX	CAN_B_RX	VDD	VSS	VDDPLL	R
T	VSS	VDD	NC	EMIOS0	EMIOS1	GPIO219	MDO9_ETPUA25_O	EMIOS13	EMIOS15	MDO5_ETPUA4_O	MDO6_ETPUA13_O	CAN_B_TX	VDDE5	ENGCLK	VDD	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

1. This pin (N13) should be tied low.

2.3 PBGA324 ballmap

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	VSTBY	AN37	AN11	VDDA0	VSSA0	AN1	AN5	VRH	VRL
B	VRC33	VSS	VDD	AN36	AN39	AN19	AN16	AN0	AN4	REFBYPC	AN23
C	ETPUA30	ETPUA31	VSS	VDD	AN38	AN17	AN20	AN21	AN3	AN7	AN22
D	ETPUA28	ETPUA29	ETPUA26	VSS	VDD	AN8 ANW	AN9	AN10 ANY	AN18	AN2	AN6
E	ETPUA24	ETPUA27	ETPUA25	ETPUA21							
F	ETPUA23	ETPUA22	ETPUA17	ETPUA18							
G	ETPUA20	ETPUA19	ETPUA14	ETPUA13							
H	ETPUA16	ETPUA15	ETPUA10	VDDEH1AB							
J	ETPUA12	ETPUA11	ETPUA6	ETPUA9					VSS	VSS	VSS
K	ETPUA8	ETPUA7	ETPUA2	ETPUA5					VSS	VSS	VSS
L	ETPUA4	ETPUA3	ETPUA0	ETPUA1					VSS	VSS	VSS

Figure 4. 324-pin PBGA package ballmap (northwest, viewed from above)

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7] During Reset	Status[7] After Reset	Package pin # 176	Package pin # 208	Package pin # 324
$\overline{BDIP}$ GPIO[63]	External burst data in progress GPIO	P G	01 00	63	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	M1
$\overline{WE}$[0]/$\overline{BE}$[0] GPIO[64]	External write/byte enable GPIO	P G	01 00	64	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	N4
$\overline{WE}$[1]/$\overline{BE}$[1] GPIO[65]	External write/byte enable GPIO	P G	01 00	65	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	N3
$\overline{OE}$ GPIO[68]	External output enable GPIO	P G	01 00	68	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	AB9
$\overline{TS}$ ALE GPIO[69]	External transfer start Address latch enable GPIO[69]	P A1 G	001 010 000	69	I/O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	T4
$\overline{TA}$ TS[8] GPIO[70]	External transfer acknowledge External transfer start GPIO	P A1 G	001 010 000	70	I/O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	R4
Calibration Bus											
CAL_$\overline{CS0}$	Calibration chip select	P	01	336	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{CS2}$ CAL_ADDR[10] CAL_$\overline{WE}$[2]/$\overline{BE}$[2]	Calibration chip select Calibration address bus Calibration write/byte enable	P A A2	001 010 100	338	O I/O O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{CS3}$ CAL_ADDR[11] CAL_$\overline{WE}$[3]/$\overline{BE}$[3]	Calibration chip select Calibration address bus Calibration write/byte enable	P A A2	001 010 100	339	O I/O O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[12] CAL_$\overline{WE}$[2]/$\overline{BE}$[2]	Calibration address bus Calibration write/byte enable	P A	01 10	340	I/O O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[13] CAL_$\overline{WE}$[3]/$\overline{BE}$[3]	Calibration address bus Calibration write/byte enable	P A	01 10	340	I/O O	VDDE12 Fast		— / —	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0[18] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[0] / —	172	B5	B8
AN1[18] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[1] / —	171	A6	A8
AN2[18] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[2] / —	170	D6	D10

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	C1
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	C2
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AB10
EMIOS1 ETPUA1_O[8] GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 Slow	— / Up	— / Up	64	T5	AB11
EMIOS2 ETPUA2_O[8] RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	65	N7	W12
EMIOS3 ETPUA3_O[8] GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	66	R6	AA11
EMIOS4 ETPUA4_O[8] RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	67	R5	AB12

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA14
EMIOS14 $\overline{\text{IRQ}}$[0] ETPUA29_O[8] GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	AB15
EMIOS15 $\overline{\text{IRQ}}$[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	Y14
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA15
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y15
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AB16
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA16
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	W16
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y16
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	AA17
Clock Synthesizer											

3.2 Maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage(2)		–0.3	1.32	V
V_{FLASH}	SR	Flash core voltage(3),(4)		–0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage(5)		–0.3	6	V
V_{DDPLL}	SR	Clock synthesizer voltage		–0.3	1.32	V
V_{RC33}	SR	Voltage regulator control input voltage(4)		–0.3	3.6	V
V_{DDA}	SR	Analog supply voltage(5)	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage(4),(6)		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage(5)		–0.3	5.5	V
V_{IN}	SR	DC input voltage(7)	V_{DDEH} powered I/O pads	–1.0(8)	V_{DDEH} + 0.3 V(9)	V
			V_{DDE} powered I/O pads	–1.0(10)	V_{DDE} + 0.3 V(10)	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current(11)	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current(12)	Per pin, applies to all analog pins	—	5	mA

Table 10. Thermal characteristics for 176-pin QFP(1) (continued)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JCtop}$	CC	D	Junction-to-Case(4)		5	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 11. Thermal characteristics for 208-pin LBGA(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2),(3)	One layer board - 1s	39	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2),(4)	Four layer board - 2s2p	24	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2),(4)	at 200 ft./min., one layer board	31	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2),(4)	at 200 ft./min., four layer board 2s2p	20	°C/W
$R_{\theta JB}$	CC	D	Junction-to-board(5)	Four layer board - 2s2p	13	°C/W
$R_{\theta JC}$	CC	D	Junction-to-case(6)		6	°C/W
Ψ_{JT}	CC	D	Junction-to-package top natural convection(7)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
3. Per SEMI G38-87 and JEDEC JESD51-2 with the single-layer board horizontal.
4. Per JEDEC JESD51-6 with the board horizontal.
5. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
6. Indicates the average thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1) with the cold plate temperature used for the case temperature.
7. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Table 12. Thermal characteristics for 324-pin PBGA(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Single layer board - 1s	31	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board - 2s2p	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., single layer board	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., four layer board 2s2p	17	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board(3)		11	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case(4)		7	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{OL_HS}	CC	P	Multi-voltage pad I/O output low voltage in high-swing mode(9)		—	—	0.2*V_{DDEH}	V
V_{OH_S}	CC	P	Slow/medium pad I/O output high voltage(9)		0.8 V_{DDEH}	—	—	V
V_{OH_F}	CC	P	Fast pad I/O output high voltage(9)		0.8 V_{DDE}	—	—	V
V_{OH_LS}	CC	P	Multi-voltage pad I/O output high voltage in low-swing mode(5),(6),(7),(8)	I_{OH_LS} = 0.5 mA	2.1	3.1	3.7	V
V_{OH_HS}	CC	P	Multi-voltage pad I/O output high voltage in high-swing mode(9)		0.8 V_{DDEH}	—	—	V
V_{HYS_S}	CC	C	Slow/medium/multi-voltage I/O input hysteresis	—	0.1 * V_{DDEH}	—	—	V
V_{HYS_F}	CC	C	Fast I/O input hysteresis	—	0.1 * V_{DDE}	—	—	V
V_{HYS_LS}	CC	C	Low-Swing-Mode Multi-Voltage I/O Input Hysteresis	hysteresis enabled	0.25	—	—	v
I_{DD}+I_{DDPLL}	CC	P	Operating current 1.2 V supplies	V_{DD} at 1.32 V at 80 MHz	—		380	mA
		P		V_{DD} at 1.32V at 120 MHz	—		400	mA
		P		V_{DD} at 1.32V at 150 MHz	—		445	mA
I_{DDSTBY}	CC	T	Operating current 0.95-1.2 V	V_{STBY} at 55 °C	—	35	100	µA
		T	Operating current 2–5.5 V	V_{STBY} at 55 °C	—	45	110	µA
$I_{DDSTBY27}$	CC	P	Operating current 0.95-1.2 V	V_{STBY} 27 °C		25	90	µA
		P	Operating current 2-5.5 V	V_{STBY} 27 °C		35	100	µA

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[16]	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7][17]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins[17]	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)[18]	DSC(PCR[8:9]) = 0b00	—		10	pF
		D		DSC(PCR[8:9]) = 0b01	—		20	
		D		DSC(PCR[8:9]) = 0b10	—		30	
		D		DSC(PCR[8:9]) = 0b11	—		50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—		7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—		10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[19])	—	—		12	pF
$R_{PUPD200K}$	SR	P	Weak Pull-Up/Down Resistance[20], 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPD100K}$	SR	P	Weak Pull-Up/Down Resistance[20], 100 kΩ Option	—	65	—	140	kΩ

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6],[7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.
3. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.
4. This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.
5. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
6. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
8. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

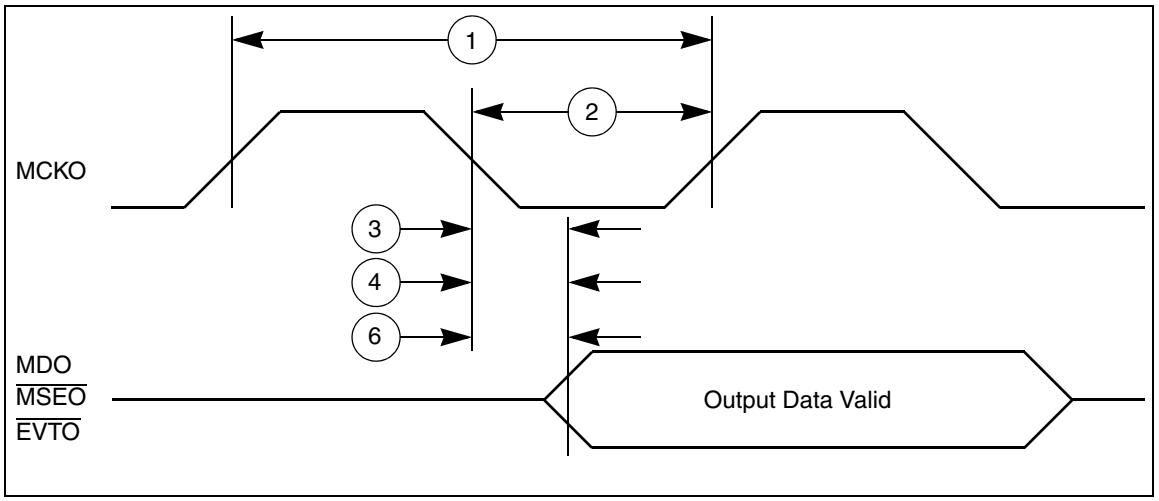

Figure 15. Nexus output timing

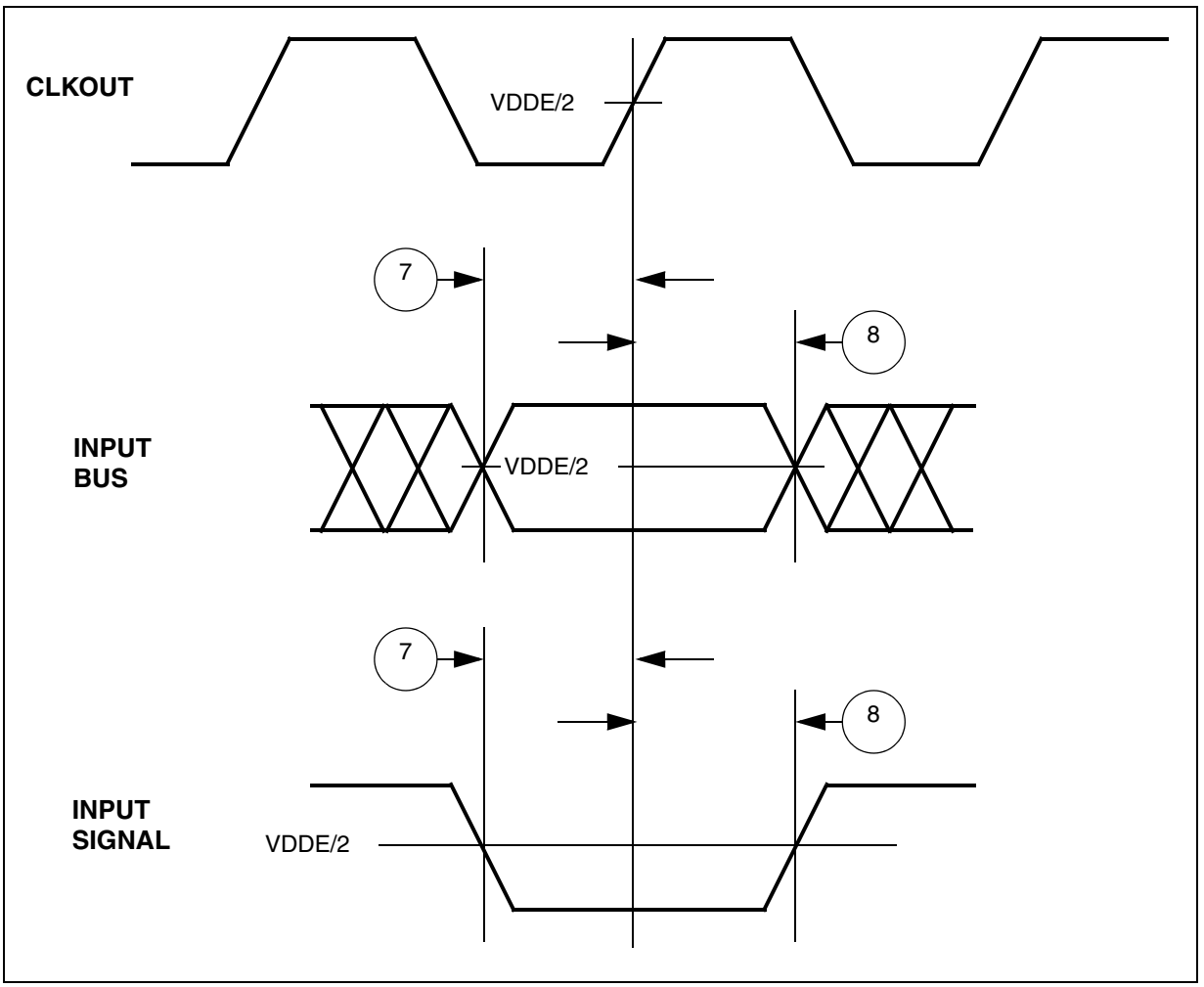

Figure 20. Synchronous input timing

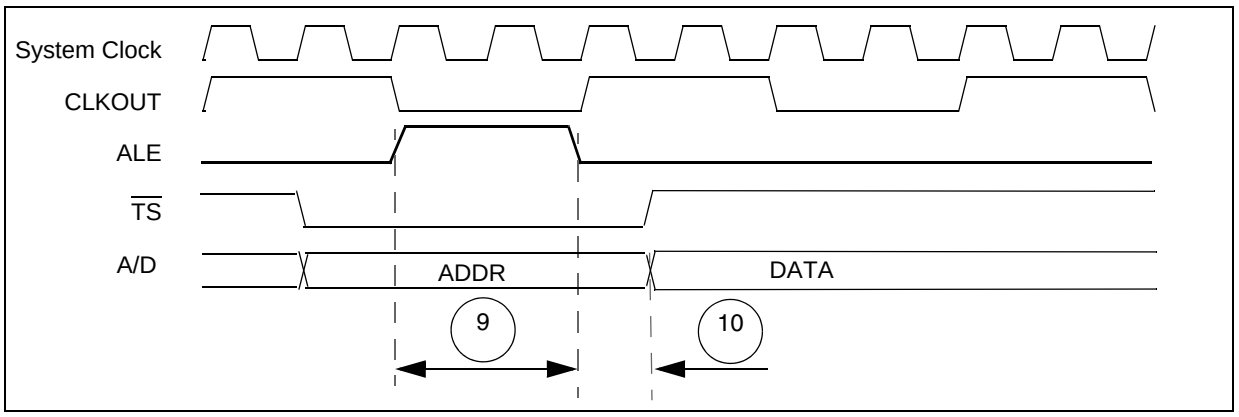

Figure 21. ALE signal timing