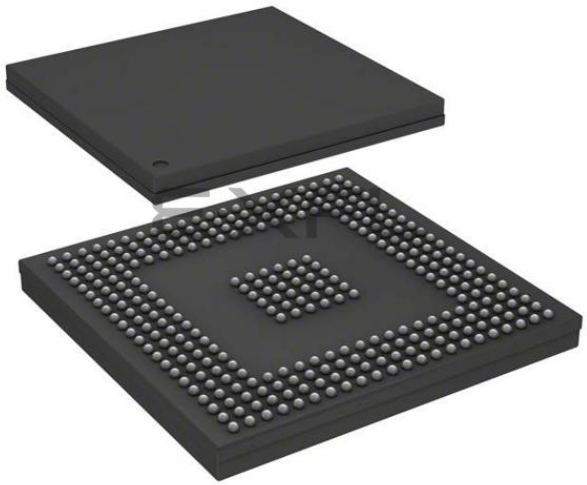

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	190
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 40x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	324-BGA
Supplier Device Package	324-PBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80b4coby

1.5.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.16 FlexCAN

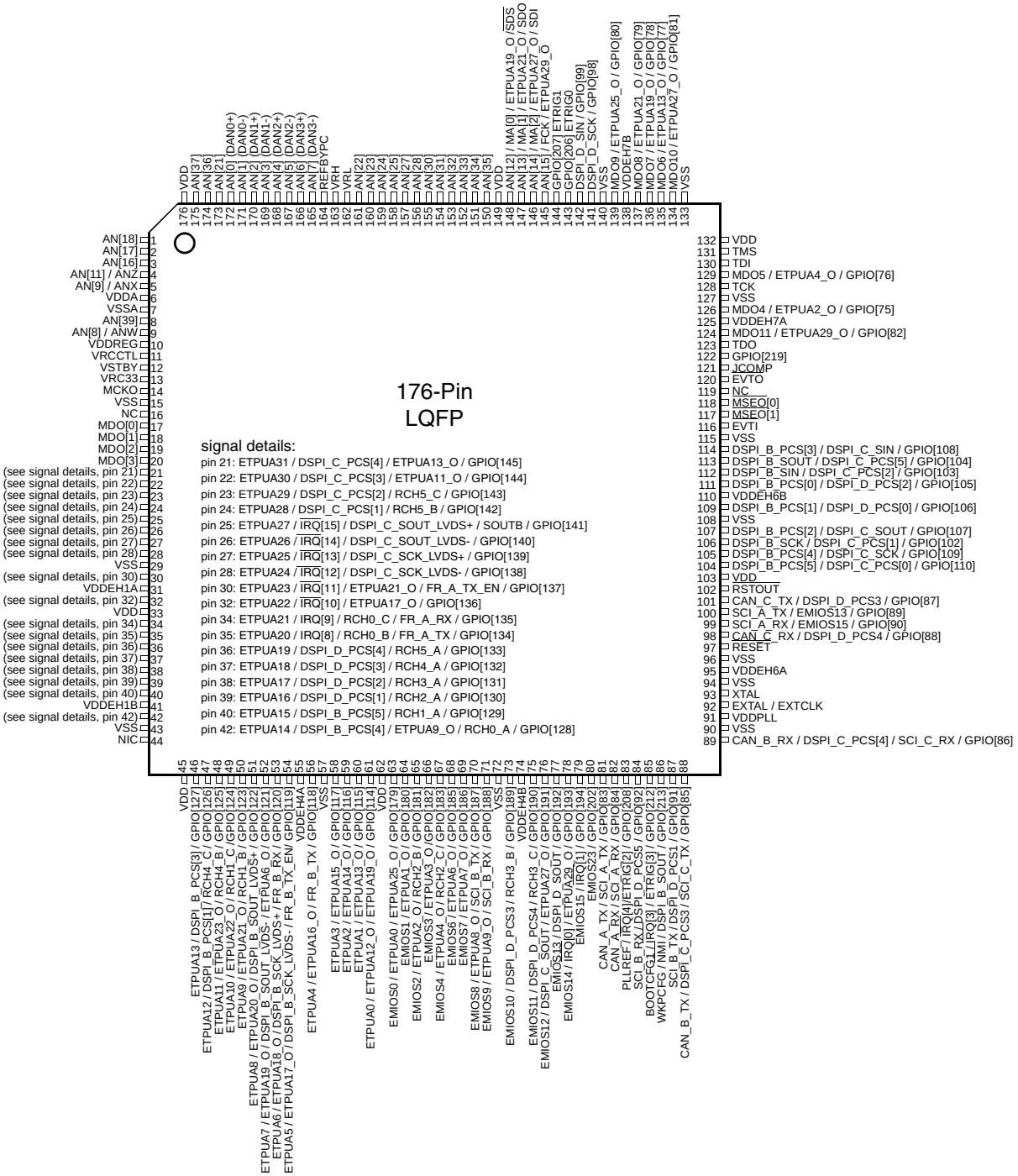
The SPC564A80 MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

2 Pinout and signal description

This section contains the pinouts for all production packages for the SPC564A80 family of devices.

Caution: Any pins labeled “NC” are to be left unconnected. Any connection to an external circuit or voltage may cause unpredictable device behavior or damage.

2.1 LQFP176 pinout



Note: Pin 96 (VSS) should be tied low.

Figure 2. 176-pin LQFP pinout (top view)

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DSPI_B_SOUT DSPI_C_PCS[5] GPIO[104]	DSPI B data output DSPI C peripheral chip select GPIO	P A1 G	01 10 00	104	O O I/O	VDDEH6 Medium	— / Up	— / Up	113	G13	J19
DSPI_B_PCS[0] DSPI_D_PCS[2] GPIO[105]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	105	I/O O I/O	VDDEH6 Medium	— / Up	— / Up	111	G16	J21
DSPI_B_PCS[1] DSPI_D_PCS[0] GPIO[106]	DSPI B peripheral chip select DSPI D peripheral chip select GPIO	P A1 G	01 10 00	106	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	109	H16	J22
DSPI_B_PCS[2] DSPI_C_SOUT GPIO[107]	DSPI B peripheral chip select DSPI C data output GPIO	P A1 G	01 10 00	107	O O I/O	VDDEH6 Medium	— / Up	— / Up	107	H15	K22
DSPI_B_PCS[3] DSPI_C_SIN GPIO[108]	DSPI B peripheral chip select DSPI C data input GPIO	P A1 G	01 10 00	108	O I I/O	VDDEH6 Medium	— / Up	— / Up	114	G14	J20
DSPI_B_PCS[4] DSPI_C_SCK GPIO[109]	DSPI B peripheral chip select SPI clock pin for DSPI module GPIO	P A1 G	01 10 00	109	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	105	H14	K20
DSPI_B_PCS[5] DSPI_C_PCS[0] GPIO[110]	DSPI B peripheral chip select DSPI C peripheral chip select GPIO	P A1 G	01 10 00	110	O I/O I/O	VDDEH6 Medium	— / Up	— / Up	104	J13	L19
eQADC											
AN0[18] DAN0+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[0] / —	172	B5	B8
AN1[18] DAN0-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[1] / —	171	A6	A8
AN2[18] DAN1+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[2] / —	170	D6	D10

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	C1
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	C2
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AB10
EMIOS1 ETPUA1_O[8] GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 Slow	— / Up	— / Up	64	T5	AB11
EMIOS2 ETPUA2_O[8] RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	65	N7	W12
EMIOS3 ETPUA3_O[8] GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	66	R6	AA11
EMIOS4 ETPUA4_O[8] RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	67	R5	AB12

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
XTAL	Crystal oscillator output	P	01	—	O	VDDEH6 Analog	—	—	93	P16	V22
EXTAL EXTCLK	Crystal oscillator input External clock input	P A	01 10	—	I	VDDEH6 Analog	—	—	92	N16	U22
CLKOUT	System clock output	P	01	229	O	VDDE5 Fast	—	CLKOUT	—	—	AA20
ENGCLK	Engineering clock output	P	01	214	O	VDDE5 Fast	—	ENGCLK	—	T14	AB21
Power / Ground											
VDDREG	Voltage Regulator Supply	—		—	I	5 V	I / —	VDDREG	10	K16	M22
VRCCTL	Voltage Regulator Control Output	—		—	O	—	O / —	VRCCTL	11	N14	V20
VRC33[20]	Internal regulator output	—		—	O	3.3 V	I/O / —	VRC33	13	A15, D1, N6, N12	A21, B1, P4, W7, Y22
	Input for external 3.3 V supply	—		—		3.3 V					
VDDA	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA	6	—	—
VSSA	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA	7	—	—
VDDA0[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA0	—	B11	A6
VSSA0[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA0	—	A11	A7
VDDA1[21]	eQADC high reference voltage	—		—	I	5 V	I / —	VDDA1	—	A4	C15
VSSA1[22]	eQADC ground/low reference voltage	—		—	I	—	I / —	VSSA1	—	A5	A15, B15
VDDPLL	FMPLL Supply Voltage	—		—	I	1.2	I / —	VDDPLL	91	R16	W22
VSTBY	Power Supply for Standby RAM	—		—	I	0.9 V - 6 V	I / —	VSTBY	12	C1	A3

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDD	Core supply for input or decoupling	—		—	I	1.2 V	I / —	VDD	33, 45, 62, 103, 132, 149, 176	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15	A2, A20, B3, C4, C22, D5, V19, W5, W20, Y4, Y21, AA3, AA22, AB2
VDDE12	External supply input for calibration bus interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE12	—	—	—
VDDE2[23]	External supply input for EBI interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE2[24]	—	—	M9, M10, N11, P11, W6, W8, Y5, AA4, AA6, AA10, AB3
VDDE5	External supply input for ENGCLK, CLKOUT and EBI signals DATA[0:15]	—		—	I	1.8 V - 3.3 V	I / —	VDDE5	—	T13	W17, Y18, AA19, AB20
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V - 5 V	I / —	VDDE-EH	—	—	R3, W2
VDDEH1A[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1A[25]	31	—	—
VDDEH1B[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1B[25]	41	—	—
VDDEH1AB[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1AB[25]	—	K4	H4
VDDEH4[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4[26]	—	—	—
VDDEH4A[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4A[26]	55	—	—
VDDEH4B[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4B[26]	74	—	—

Table 5. Pad types

Pad Type	Name	I/O Voltage Range
Slow	pad_ssr_hv	3.0V - 5.5 V
Medium	pad_msr_hv	3.0 V - 5.5 V
Fast	pad_fc	3.0 V - 3.6 V
MultiV(1),(2)	pad_multv_hv	3.0 V - 5.5 V (high swing mode) 3.0 V - 3.6 V (low swing mode)
Analog	pad_ae_hv	0.0 - 5.5 V
LVDS	pad_lo_lv	—

1. Multivoltage pads are automatically configured in low swing mode when a JTAG or Nexus function is selected, otherwise they are high swing.
2. VDDEH7 supply cannot be below 4.5 V when in low-swing mode.

2.5 Signal details

Table 6. Signal details

Signal	Module or Function	Description
CLKOUT	Clock Generation	SPC564A80 clock output for the external/calibration bus interface
ENGCLK	Clock Generation	Clock for external ASIC devices
EXTAL	Clock Generation	Input pin for an external crystal oscillator or an external clock source based on the value driven on the PLLREF pin at reset.
PLLREF	Clock Generation Reset/Configuration	PLLREF is used to select whether the oscillator operates in xtal mode or external reference mode from reset. PLLREF=0 selects external reference mode. On the 324BGA package, PLLREF is bonded to the ball used for PLLCFG[0] for compatibility with previous devices . For the 176-pin QFP and 208-ball BGA packages: 0: External reference clock is selected. 1: XTAL oscillator mode is selected For the 324 ball BGA package: If RSTCFG is 0: 0: External reference clock is selected. 1: XTAL oscillator mode is selected. If RSTCFG is 1, XTAL oscillator mode is selected.
XTAL	Clock Generation	Crystal oscillator input
DSPI_B_SCK_LVDS- DSPI_B_SCK_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission
DSPI_B_SOUT_LVDS- DSPI_B_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_B TSB mode transmission

Table 6. Signal details (continued)

Signal	Module or Function	Description
RCH0_[A:C] RCH1_[A:C] RCH2_[A:C] RCH3_[A:C] RCH4_[A:C] RCH5_[A:C]	eTPU2 Reaction Module	eTPU2 reaction channels. Used to control external actuators, e.g., solenoid control for direct injection systems and valve control in automatic transmissions
TCRCLKA	eTPU2	Input clock for TCR time base
CAN_A_TX CAN_B_TX CAN_C_TX	FlexCan_A - FlexCAN_C	FlexCAN transmit
CAN_A_RX CAN_B_RX CAN_C_RX	FlexCAN_A - FlexCAN_C	FlexCAN receive
FR_A_RX FR_B_RX	FlexRay	FlexRay receive (Channels A, B)
$\overline{\text{FR\_A\_TX\_EN}}$ $\overline{\text{FR\_B\_TX\_EN}}$	FlexRay	FlexRay transmit enable (Channels A, B)
FR_A_TX FR_B_TX	FlexRay	Flexray transmit (Channels A, B)
JCOMP	JTAG	Enables the JTAG TAP controller.
TCK	JTAG	Clock input for the on-chip test logic.
TDI	JTAG	Serial test instruction and data input for the on-chip test logic.
TDO	JTAG	Serial test data output for the on-chip test logic.
TMS	JTAG	Controls test mode operations for the on-chip test logic.
$\overline{\text{EVTI}}$	Nexus	$\overline{\text{EVTI}}$ is an input that is read on the negation of $\overline{\text{RESET}}$ to enable or disable the Nexus Debug port. After reset, the $\overline{\text{EVTI}}$ pin is used to initiate program synchronization messages or generate a breakpoint.
$\overline{\text{EVTO}}$	Nexus	Output that provides timing to a development tool for a single watchpoint or breakpoint occurrence.
MCKO	Nexus	MCKO is a free running clock output to the development tools which is used for timing of the MDO and $\overline{\text{MSEO}}$ signals.
MDO[0:11](1)	Nexus	Trace message output to development tools. This pin also indicates the status of the crystal oscillator clock following a power-on reset, when MDO[0] is driven high until the crystal oscillator clock achieves stability and is then negated.
$\overline{\text{MSEO}}$[0:1](1)	Nexus	Output pin—Indicates the start or end of the variable length message on the MDO pins
$\overline{\text{RDY}}$	Nexus	Nexus Ready Output ($\overline{\text{RDY}}$) is an output that indicates to the development tools the data is ready to be read from or written to the Nexus read/write access registers.

3.2 Maximum ratings

Table 9. Absolute maximum ratings(1)

Symbol		Parameter	Conditions	Value		Unit
				min	max	
V_{DD}	SR	1.2 V core supply voltage(2)		–0.3	1.32	V
V_{FLASH}	SR	Flash core voltage(3),(4)		–0.3	3.6	V
V_{STBY}	SR	SRAM standby voltage(5)		–0.3	6	V
V_{DDPLL}	SR	Clock synthesizer voltage		–0.3	1.32	V
V_{RC33}	SR	Voltage regulator control input voltage(4)		–0.3	3.6	V
V_{DDA}	SR	Analog supply voltage(5)	Reference to V_{SSA}	–0.3	5.5	V
V_{DDE}	SR	I/O supply voltage(4),(6)		–0.3	3.6	V
V_{DDEH}	SR	I/O supply voltage(5)		–0.3	5.5	V
V_{IN}	SR	DC input voltage(7)	V_{DDEH} powered I/O pads	–1.0(8)	V_{DDEH} + 0.3 V(9)	V
			V_{DDE} powered I/O pads	–1.0(10)	V_{DDE} + 0.3 V(10)	
			V_{DDA} powered I/O pads	–1.0	5.5	
V_{DDREG}	SR	Voltage regulator supply voltage		–0.3	5.5	V
V_{RH}	SR	Analog reference high voltage	Reference to VRL	–0.3	5.5	V
$V_{SS} – V_{SSA}$	SR	V_{SS} differential voltage		–0.1	0.1	V
$V_{RH} – V_{RL}$	SR	V_{REF} differential voltage		–0.3	5.5	V
$V_{RL} – V_{SSA}$	SR	VRL to V_{SSA} differential voltage		–0.3	0.3	V
$V_{SSPLL} – V_{SS}$	SR	V_{SSPLL} to V_{SS} differential voltage		–0.1	0.1	V
I_{MAXD}	SR	Maximum DC digital input current(11)	Per pin, applies to all digital pins	–3	3	mA
I_{MAXA}	SR	Maximum DC analog input current(12)	Per pin, applies to all analog pins	—	5	mA

Table 16. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
5c	—	CC	D	Voltage regulator 3.3 V output impedance at maximum DC load	—	—	2	Ω	
5d	Idd3p3	CC	P	Voltage regulator 3.3 V maximum DC output current (internal regulator enabled)(6)	80(7)	—	—	mA	
5e	Vdd33 ILim	CC	C	Voltage regulator 3.3 V DC current limit	—	130	—	mA	
6	Lvi3p3	CC	C	Nominal LVI for rising 3.3 V supply	—	3.090	—	V	The Lvi3p3 specs are also valid for the Vddeh LVI
6a	—	CC	C	Variation of LVI for rising 3.3 V supply at power-on reset	Lvi3p3 - 6%	Lvi3p3	Lvi3p3 + 6%	V	See note (8)
6b	—	CC	C	Variation of LVI for rising 3.3 V supply after power-on reset	Lvi3p3 - 3%	Lvi3p3	Lvi3p3 + 3%	V	See note (8)
6c	—	CC	C	Trimming step LVI 3.3 V	—	20	—	mV	
6d	Lvi3p3_h	CC	C	LVI 3.3 V hysteresis	—	60	—	mV	
7	Por3.3V_r	CC	C	Nominal POR for rising 3.3 V supply	—	2.07	—	V	The 3.3V POR specs are also valid for the V_{DDEH} POR
7a	—	CC	C	Variation of POR for rising 3.3 V supply	Por3.3V_r-35%	Por3.3V_r	Por3.3V_r+35%	V	
7b	Por3.3V_f	CC	C	Nominal POR for falling 3.3 V supply	—	1.95	—	V	
7c	—	CC	C	Variation of POR for falling 3.3 V supply	Por3.3V_f - 35%	Por3.3V_f	Por3.3V_f + 35%	V	
8	Lvi5p0	CC	C	Nominal LVI for rising 5 V V_{DDREG} supply	—	4.290	—	V	
8a	—	CC	C	Variation of LVI for rising 5 V V_{DDREG} supply at power-on reset	Lvi5p0 - 6%	Lvi5p0	Lvi5p0 + 6%	V	
8b	—	CC	C	Variation of LVI for rising 5 V V_{DDRE}G supply power-on reset	Lvi5p0 - 3%	Lvi5p0	Lvi5p0 + 3%	V	
8c	—	CC	C	Trimming step LVI 5 V	—	20	—	mV	
8d	Lvi5p0_h	CC	C	LVI 5 V hysteresis	—	60	—	mV	

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDE}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDE}	
V_{IL_LS}	CC	C	Multi-voltage I/O pad input low voltage in Low-swing-mode[5],[6],[7],[8]	Hysteresis enabled	V_{SS}-0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}-0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS}-0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage[9]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing-mode[5],[6],[7],[8]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[9]		—	—	0.2*V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage[9]		—	—	0.2*V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[5],[6],[7],[8],[9]		—	—	0.6	V

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
R_{PUPD5K}	SR	C	Weak Pull-Up/Down Resistance(20), 5 kΩ Option	5 V ± 5% supply	1.4	—	7.5	kΩ
$R_{PUPDMTCH}$	CC	C	Pull-up/Down Resistance matching ratios (100K/200K)	Pull-up and pull-down resistances both enabled and settings are equal.	–2.5	—	2.5	%
T_A (T_L to T_H)	SR	—	Operating temperature range - ambient (packaged)	—	–40.0		125.0	°C
—	SR	—	Slew rate on power supply pins	—	—		25	V/ms

1. These specifications apply when V_{RC33} is supplied externally, after disabling the internal regulator (V_{DDREG} = 0).
2. ADC is functional with 4 V ≤ V_{DDA} ≤ 4.75 V but with derated accuracy. This means the ADC will continue to function at full speed with no undesirable behavior, but the accuracy will be degraded.
3. The V_{DDF} supply is connected to V_{DD} in the package substrate. This specification applies to calibration package devices only.
4. V_{FLASH} is only available in the calibration package.
5. Power supply for multi-voltage pads cannot be below 4.5 V when in low-swing mode.
6. The slew rate (SRC) setting must be 0b11 when in low-swing mode.
7. While in low-swing mode there are no restrictions in transitioning to high-swing mode.
8. Pin in low-swing mode can accept a 5 V input.
9. All V_{OL}/V_{OH} values 100% tested with ± 2 mA load except where noted.
10. Bypass mode, system clock at 1 MHz (using system clock divider), PLL shut down, CPU running simple executive code, 4 x ADC conversion every 10 ms, 2 x PWM channels 1 kHz, all other modules stopped.
11. Bypass mode, system clock at 1 MHz (using system clock divider), CPU stopped, PIT running, all other modules stopped.
12. This current will be consumed for external regulation and internal regulation, when 3.3V regulator is switched off by shadow flash
13. If 1.2V and 3.3V internal regulators are on,then iddreg=70mA

    If supply is external that is 3.3V internal regulator is off, then iddreg=15mA
14. Power requirements for each I/O segment are dependent on the frequency of operation and load of the I/O pins on a particular I/O segment, and the voltage of the I/O segment. See *Table 22* for values to calculate power dissipation for specific operation. The total power consumption of an I/O segment is the sum of the individual power consumptions for each pin on the segment.
15. Absolute value of current, measured at V_{IL} and V_{IH}.
16. Weak pull up/down inactive. Measured at V_{DDE} = 3.6 V and V_{DDEH} = 5.25 V. Applies to fast, slow, and medium pads.
17. Maximum leakage occurs at maximum operating temperature. Leakage current decreases by approximately one-half for each 8 to 12 °C, in the ambient temperature range of 50 to 125 °C. Applies to analog pads.
18. Applies to CLKOUT, external bus pins, and Nexus pins.
19. Applies to the FCK, SDI, SDO, and $\overline{SDS}$ pins.
20. This programmable option applies only to eQADC differential input channels and is used for biasing and sensor diagnostics.

Table 33. Flash program and erase specifications(1) (continued)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	3000	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5300	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

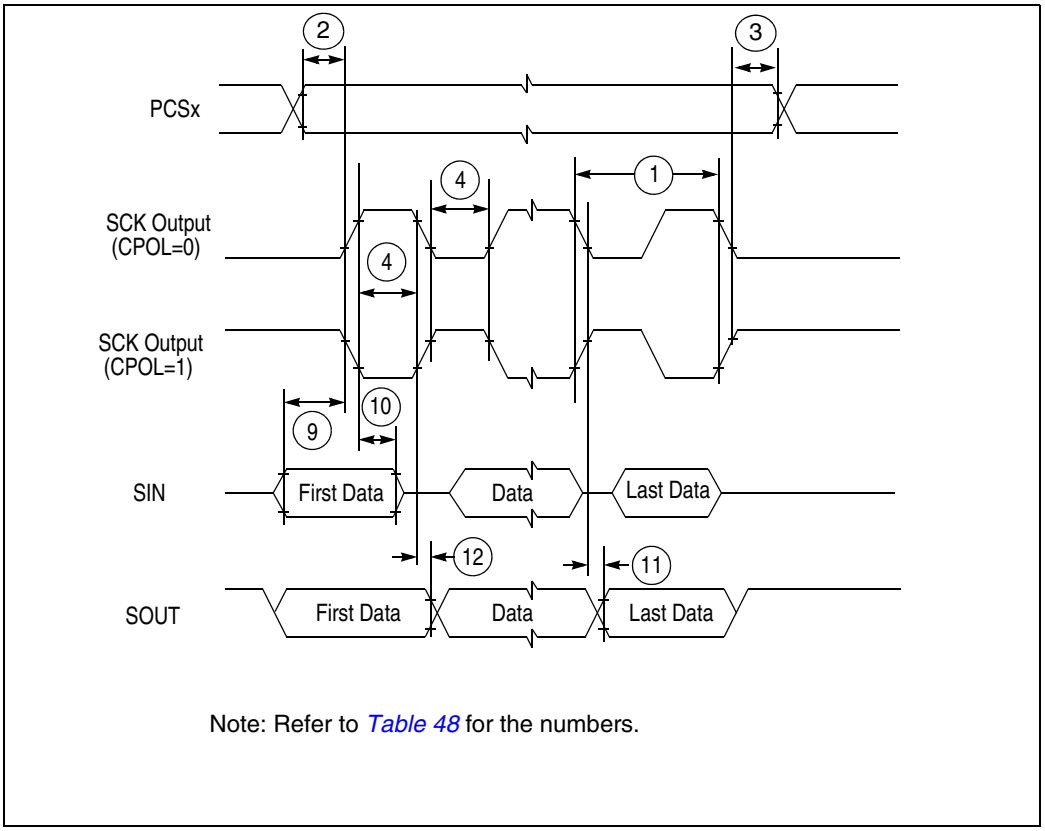
1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.
4. Page size is 128 bits (4 words).
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A80 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when pcssck = 3(01), and cssck =2 (0000).
8. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9. Timing met when ASC = 2 (0000), and PASC = 3 (01).
10. Timing met when pcssck = 3.
11. Timing met when ASC = 3.
12. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



Note: Refer to *Table 48* for the numbers.

Figure 23. DSPI classic SPI timing — master, CPHA = 0

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

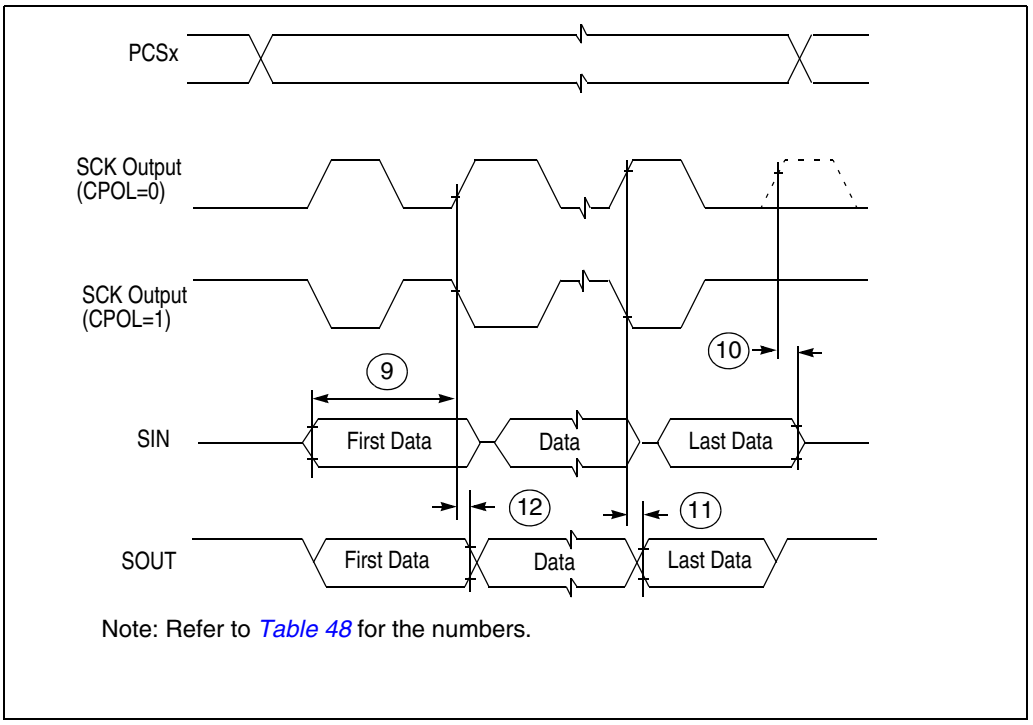


Figure 28. DSPI modified transfer format timing — master, CPHA = 1

3.17.10 FlexCAN system clock source

Table 50. FlexCAN engine system clock divider threshold

#	Symbol	Characteristic	Value	Unit
1	F_{CAN_TH}	FlexCAN engine system clock threshold	100	MHz

Table 51. FlexCAN engine system clock divider

System Frequency	Required SIU_SYSDIV[CAN_SRC] Value
<= F_{CAN_TH}	0(1),(2)
> F_{CAN_TH}	1(2),(3)

1. Divides system clock source for FlexCAN engine by 1.
2. System clock is only selected for FlexCAN when CAN_CR[CLK_SRC] = 1.
3. Divides system clock source for FlexCAN engine by 2.

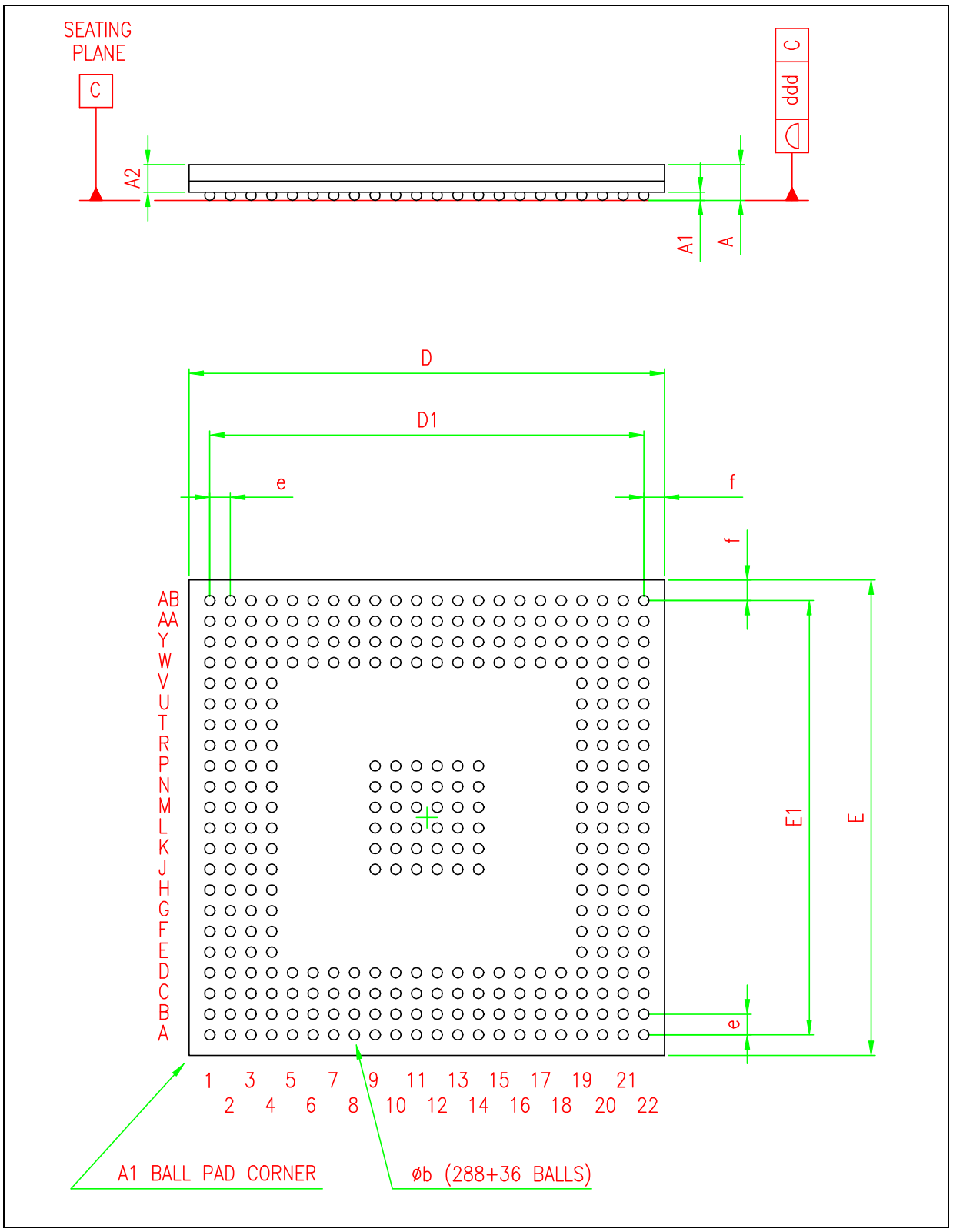


Figure 34. PBGA324 package mechanical drawing

Table 56. Revision history (continued)

Date	Revision	Changes
10-Feb-2011 (cont)	5 (cont)	– Added DATA[0:15] to V_{DDE5} in the “signal properties” table. – Updated VSTBY parameters in the “Power/ground segmentation” table. – Updated the parameter symbols and classifications throughout the document. – Updated footnote instances in the “Absolute maximum ratings“ table. – Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. – Updated the format of the “EMI (electromagnetic interference) characteristics” table. – Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications“ table. – Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. – Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. – Removed the “VRC electrical specifications” table as it contained redundant information. – Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. – Updated V_{IH_LS} in the “DC electrical specifications” table. – Updated the V_{OH_LS} min value in the “DC electrical specifications” table. – Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. – Updated the I_{DDA}/I_{REF}/I_{DDREG} max value in the “DC electrical specifications” table. – Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. – Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. – Updated values for V_{OD} in the “DSPI LVDS pad specification“ table. – Removed the footnotes from the “DSPI LVDS pad specifications“ table. – Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. – Updated footnotes in the “PLLMRFM electrical specifications” table. – Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)“ table. – Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. – Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. – Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Updated the Typical values for $T_{dwprogram}$,, $T_{pprogram}$, and $T_{16kpperase}$, and updated the Initial Max values for $T_{128kpperase}$ and $T_{256kpperase}$ in the “Flash program and erase specifications” table. – Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. – Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)“ table.