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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	150MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7cfay

providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - Two types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay, and EBI[1]) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only[(a)]
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the pre-programmed memory region descriptors

- An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
- 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 SIU

The SPC564A80 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The

a. EBI not available on all packages and is not available, as a master, for customer.

  - Four-entry 256-bit wide line read buffer
  - Prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing usable in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) usable for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 128 bits (four words) to accelerate programming
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.5.9 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by ST and is identical for all SPC564A80 MCUs. The BAM program is executed every time the MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on external bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC564A80 hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping of all physical addresses to logical addresses with minimum address translation
- Sets up MMU to allow user boot code to execute as either Power Architecture embedded category (default) or as VLE code
- Location and detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using standard protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or VLE code

1.5.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.16 FlexCAN

The SPC564A80 MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

1.6.2 Block summary

Table 3 summarizes the functions of the blocks present on the SPC564A80 series microcontrollers.

Table 3. SPC564A80 series block summary

Block	Function
Boot assist module (BAM)	Block of read-only memory containing executable code that searches for user-supplied boot code and, if none is found, executes the BAM boot code resident in device ROM.
Calibration Bus interface	Transfers data across the crossbar switch to/from peripherals attached to the calibration tool connector.
Controller area network (FlexCAN)	Supports the standard CAN communications protocol.
Crossbar switch (XBAR)	Internal busmaster.
Cyclic redundancy check (CRC)	CRC checksum generator.
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices.
e200z4 core	Executes programs and interrupt handlers.
Enhanced direct memory access (eDMA)	Performs complex data movements with minimal intervention from the core.
Enhanced modular input-output system (eMIOS)	Provides the functionality to generate or measure events.
Enhanced queued analog-to-digital converter (eQADC)	Provides accurate and fast conversions for a wide range of applications.
Enhanced serial communication interface (eSCI)	Provides asynchronous serial communication capability with peripheral devices and other microcontroller units.
Enhanced time processor unit (eTPU2)	Second-generation co-processor processes real-time input events, performs output waveform generation, and accesses shared data without host intervention.
Error Correction Status Module (ECSM)	The Error Correction Status Module supports a number of miscellaneous control functions for the platform, and includes registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
External bus interface (EBI)	Enables expansion of internal bus to enable connection of external memory or peripherals.
Flash memory	Provides storage for program code, constants, and variables.
FlexRay	Provides high-speed distributed control for advanced automotive applications.
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests.
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode.
Memory protection unit (MPU)	Provides hardware access control for all memory references generated.
Nexus port controller (NPC)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard.

2.3 PBGA324 ballmap

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	VDD	VSTBY	AN37	AN11	VDDA0	VSSA0	AN1	AN5	VRH	VRL
B	VRC33	VSS	VDD	AN36	AN39	AN19	AN16	AN0	AN4	REFBYPC	AN23
C	ETPUA30	ETPUA31	VSS	VDD	AN38	AN17	AN20	AN21	AN3	AN7	AN22
D	ETPUA28	ETPUA29	ETPUA26	VSS	VDD	AN8 ANW	AN9	AN10 ANY	AN18	AN2	AN6
E	ETPUA24	ETPUA27	ETPUA25	ETPUA21							
F	ETPUA23	ETPUA22	ETPUA17	ETPUA18							
G	ETPUA20	ETPUA19	ETPUA14	ETPUA13							
H	ETPUA16	ETPUA15	ETPUA10	VDDEH1AB							
J	ETPUA12	ETPUA11	ETPUA6	ETPUA9					VSS	VSS	VSS
K	ETPUA8	ETPUA7	ETPUA2	ETPUA5					VSS	VSS	VSS
L	ETPUA4	ETPUA3	ETPUA0	ETPUA1					VSS	VSS	VSS

Figure 4. 324-pin PBGA package ballmap (northwest, viewed from above)

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DATA7 ADDR23 GPIO[35]	External data bus External address bus GPIO	P A1 G	001 010 000	35	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA9
DATA8 ADDR24 GPIO[36]	External data bus External address bus GPIO	P A1 G	001 010 000	36	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y6
DATA9 ADDR25 GPIO[37]	External data bus External address bus GPIO	P A1 G	001 010 000	37	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y7
DATA10 ADDR26 GPIO[38]	External data bus External address bus GPIO	P A1 G	001 010 000	38	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y8
DATA11 ADDR27 GPIO[39]	External data bus External address bus GPIO	P A1 G	001 010 000	39	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W9
DATA12 ADDR28 GPIO[40]	External data bus External address bus GPIO	P A1 G	001 010 000	40	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W10
DATA13 ADDR29 GPIO[41]	External data bus External address bus GPIO	P A1 G	001 010 000	41	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y10
DATA14 ADDR30 GPIO[42]	External data bus External address bus GPIO	P A1 G	001 010 000	42	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W11
DATA15 ADDR31 GPIO[43]	External data bus External address bus GPIO	P A1 G	001 010 000	43	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y11
RD_$\overline{WR}$ GPIO[62]	External read/write GPIO	P G	01 00	62	I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	P3

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field (3)	PCR (4)	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDEH7B	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4,W19, Y3, Y20, AA2, AA21, AB1, AB22

1. For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.
2. The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.
3. The Pad Configuration Register (PCR) PA field is used by software to select pin function.
4. Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.
5. The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (-10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/- 10%).
6. See *Table 5* for details on pad types.

Table 6. Signal details (continued)

Signal	Module or Function	Description
$\overline{\text{IRQ}}$[0:5] $\overline{\text{IRQ}}$[7:15]	SIU - External Interrupts	The $\overline{\text{IRQ}}$[0:15] pins connect to the SIU IRQ inputs. IMUX Select Register 1 is used to select the $\overline{\text{IRQ}}$[0:15] pins as inputs to the IRQs. See the *SPC564A80 Microcontroller Reference Manual* for more information.
$\overline{\text{NMI}}$	SIU - External Interrupts	Non-Maskable Interrupt
GPIO[0:3] GPIO[8:43] GPIO[62:65] GPIO[68:70] GPIO[75:145] GPIO[179:204] GPIO[208:213] GPIO[219] GPIO[244:245]	SIU - GPIO	Configurable general purpose I/O pins. Each GPIO input and output is separately controlled by an 8-bit input (GPDI) or output (GPDO) register. Additionally, each GPIO pins is configured using a dedicated SIU_PCR register. The GPIO pins are generally multiplexed with other I/O pin functions. See The *SPC564A80 Microcontroller Reference Manual* for more information. –
$\overline{\text{RESET}}$	SIU - Reset	The $\overline{\text{RESET}}$ pin is an active low input. The $\overline{\text{RESET}}$ pin is asserted by an external device during a power-on or external reset. The internal reset signal asserts only if the $\overline{\text{RESET}}$ pin asserts for 10 clock cycles. Assertion of the $\overline{\text{RESET}}$ pin while the device is in reset causes the reset cycle to start over. The $\overline{\text{RESET}}$ pin has a glitch detector which detects spikes greater than two clock cycles in duration that fall below the switch point of the input buffer logic of the VDDEH input pins. The switch point lies between the maximum VIL and minimum VIH specifications for the VDDEH input pins.
RSTCFG	SIU - Reset	Used to enable or disable the PLLREF and the BOOTCFG[0:1] configuration signals. 0:Get configuration information from BOOTCFG[0:1] and PLLREF 1:Use default configuration of booting from internal flash with crystal clock source For the 176-pin QFP and 208-ball BGA packages RSTCFG is always 0, so PLLREF and BOOTCFG signals are used.
$\overline{\text{RSTOUT}}$	SIU - Reset	The $\overline{\text{RSTOUT}}$ pin is an active low output that uses a push/pull configuration. The $\overline{\text{RSTOUT}}$ pin is driven to the low state by the MCU for all internal and external reset sources. There is a delay between initiation of the reset and the assertion of the RSTOUT pin.

1. Do not connect pin directly to a power supply or ground.

3.9 I/O pad current specifications

The power consumption of an I/O segment depends on the usage of the pins on a particular segment. The power consumption is the sum of all output pin currents for a particular segment. The output pin current can be calculated from *Table 22* based on the voltage, frequency, and load on the pin. Use linear scaling to calculate pin currents for voltage, frequency, and load parameters that fall outside the values given in *Table 22*.

Table 22. I/O pad average I_{DDE} specifications(1)

Pad Type	Symbol		C	Period (ns)	Load(2) (pF)	V_{DDE} (V)	Drive/Slew Rate Select	I_{DDE} Avg (mA)(3)	I_{DDE} RMS (mA)
Slow	$I_{DRV\_SSR\_HV}$	CC	D	37	50	5.5	11	9	—
		CC	D	130	50	5.5	01	2.5	—
		CC	D	650	50	5.5	00	0.5	—
		CC	D	840	200	5.5	00	1.5	—
Medium	$I_{DRV\_MSR\_HV}$	CC	D	24	50	5.5	11	14	—
		CC	D	62	50	5.5	01	5.3	—
		CC	D	317	50	5.5	00	1.1	—
		CC	D	425	200	5.5	00	3	—
Fast	I_{DRV_FC}	CC	D	10	50	3.6	11	22.7	68.3
		CC	D	10	30	3.6	10	12.1	41.1
		CC	D	10	20	3.6	01	8.3	27.7
		CC	D	10	10	3.6	00	4.44	14.3
		CC	D	10	50	1.98	11	12.5	31
		CC	D	10	30	1.98	10	7.3	18.6
		CC	D	10	20	1.98	01	5.42	12.6
		CC	D	10	10	1.98	00	2.84	6.4
MultiV (High Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	20	50	5.5	11	9	—
		CC	D	30	50	5.5	01	6.1	—
		CC	D	117	50	5.5	00	2.3	—
		CC	D	212	200	5.5	00	5.8	—
MultiV (Low Swing Mode)	$I_{DRV\_MULTV\_HV}$	CC	D	30	30	5.5	11	3.4	—

1. Numbers from simulations at best case process, 150 °C.
2. All loads are lumped.
3. Average current is for pad configured as output only.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)(1)

Name		C	Output Delay (ns)(2),(3) Low-to-High / High-to-Low		Rise/Fall Edge (ns)(3),(4)		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5),(6),(7)	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11(8)
	N/A							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7),(10)	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11(8)
	N/A							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	N/A							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	N/A							
pad_i_hv(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

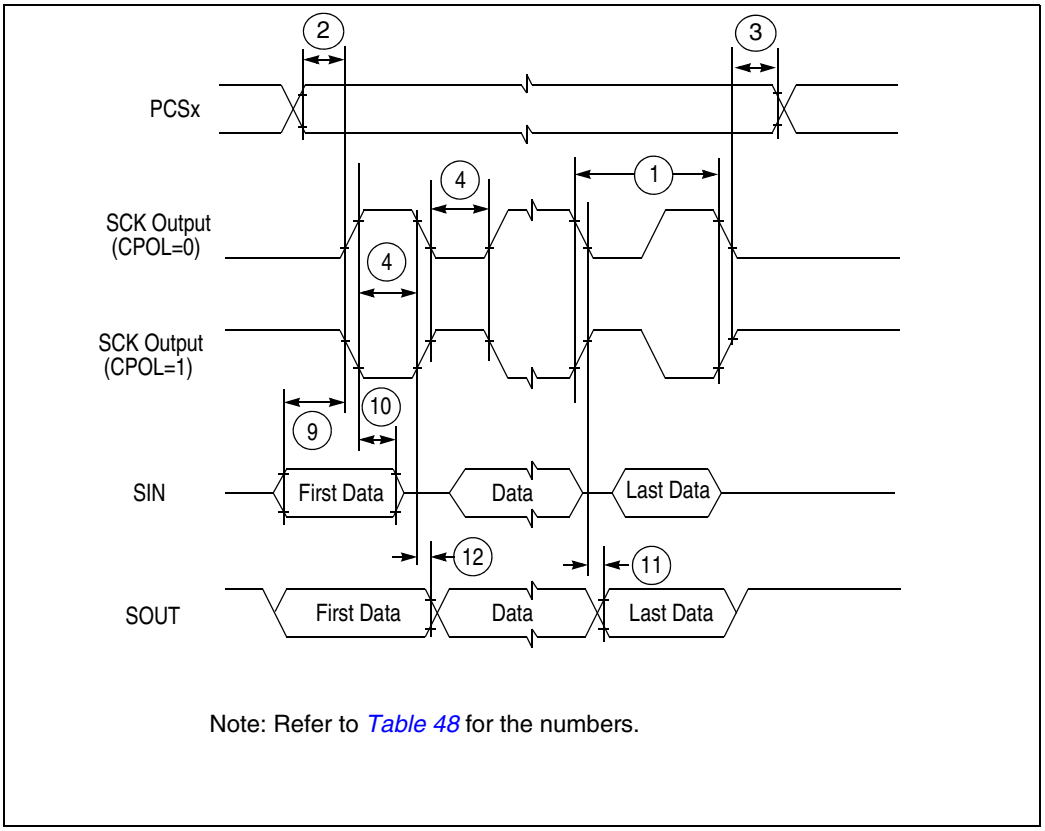
1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
7. Output delay is shown in *Figure 9: Pad output delay*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
11. Selectable high/low swing IO pad with selectable slew in high swing mode only.
12. Fast pads are 3.3 V pads.
13. Stand alone input buffer. Also has weak pull-up/pull-down.

Table 36. Pad AC specifications (V_{DDE} = 3.3 V)[1]

Pad Type		C	Output Delay (ns)[2],[3] Low-to-High / High-to-Low		Rise/Fall Edge (ns)[3],[4]		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium[5],[6],[7]	CC	D	5.8/4.4	18/17	2.7/2.1	10/10	50	11[8]
	CC	D	16/13	46/49	11.2/8.6	34/34	200	
	N/A							10[9]
	CC	D	14/16	37/45	6.5/6.7	19/19	50	01
	CC	D	27/27	69/82	15/13	43/43	200	
	CC	D	83/86	200/210	38/38	86/86	50	00
	CC	D	113/109	270/285	53/46	120/120	200	
Slow[7],[10]	CC	D	9.2/6.9	27/28	5.5/4.1	20/20	50	11
	CC	D	30/23	81/87	21/16	63/63	200	
	N/A							10[9]
	CC	D	31/31	80/90	15.4/15.4	42/42	50	01
	CC	D	58/52	144/155	32/26	82/85	200	
	CC	D	162/168	415/415	80/82	190/190	50	00
	CC	D	216/205	533/540	106/95	250/250	200	
MultiV[7],[11] (High Swing Mode)	CC	D		3.7/3.1		10/10	30	11[8]
	CC	D		46/49		37/37	200	
	N/A							10[9]
	CC	D		32		15/15	50	01
	CC	D		72		46/46	200	
	CC	D		210		100/100	50	00
	CC	D		295		134/134	200	
MultiV (Low Swing Mode)	Not a valid operational mode							
Fast	CC	D		2.5/2.5		1.2/1.2	10	00
	CC	D		2.5/2.5		1.2/1.2	20	01
	CC	D		2.5/2.5		1.2/1.2	30	10
	CC	D		2.5/2.5		1.2/1.2	50	11[8]
pad_i_hv[12]	CC	D	0.5/0.5	3/3	0.4/0.4	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDE} = 3 V to 3.6 V, V_{DDEH} = 3 V to 3.6 V, $T_A = T_L$ to T_H.
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.

3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A80 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when pcssck = 3(01), and cssck =2 (0000).
8. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9. Timing met when ASC = 2 (0000), and PASC = 3 (01).
10. Timing met when pcssck = 3.
11. Timing met when ASC = 3.
12. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



Note: Refer to *Table 48* for the numbers.

Figure 23. DSPI classic SPI timing — master, CPHA = 0

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

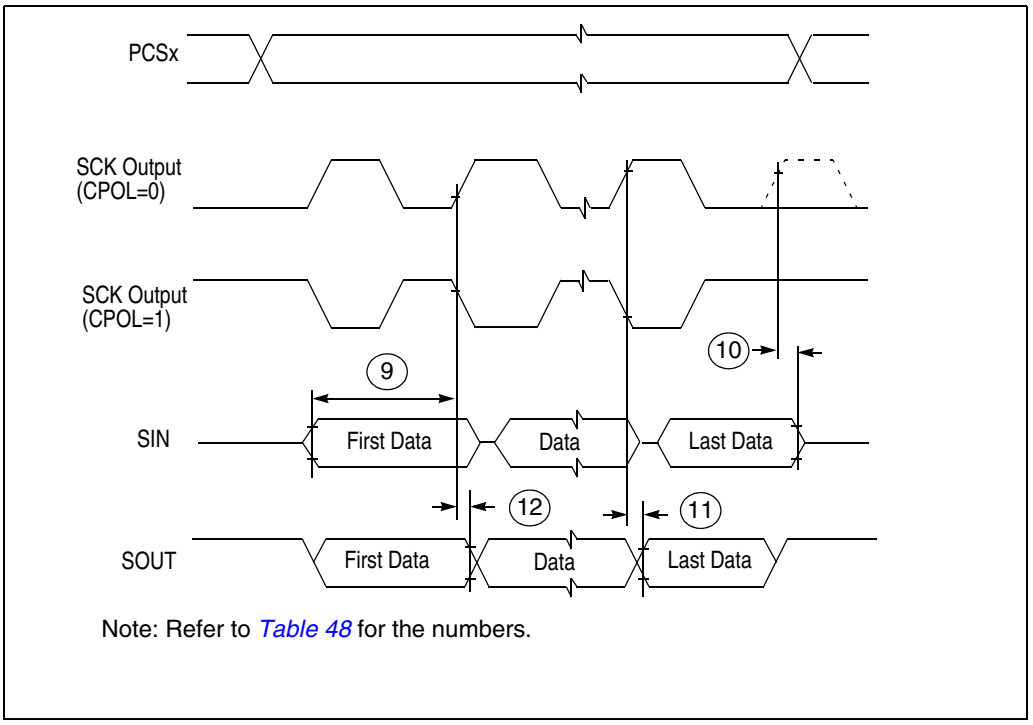


Figure 28. DSPI modified transfer format timing — master, CPHA = 1

3.17.9 eQADC SSI timing

Table 49. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency (2), (3)	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	-7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	-7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1. SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
3. FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

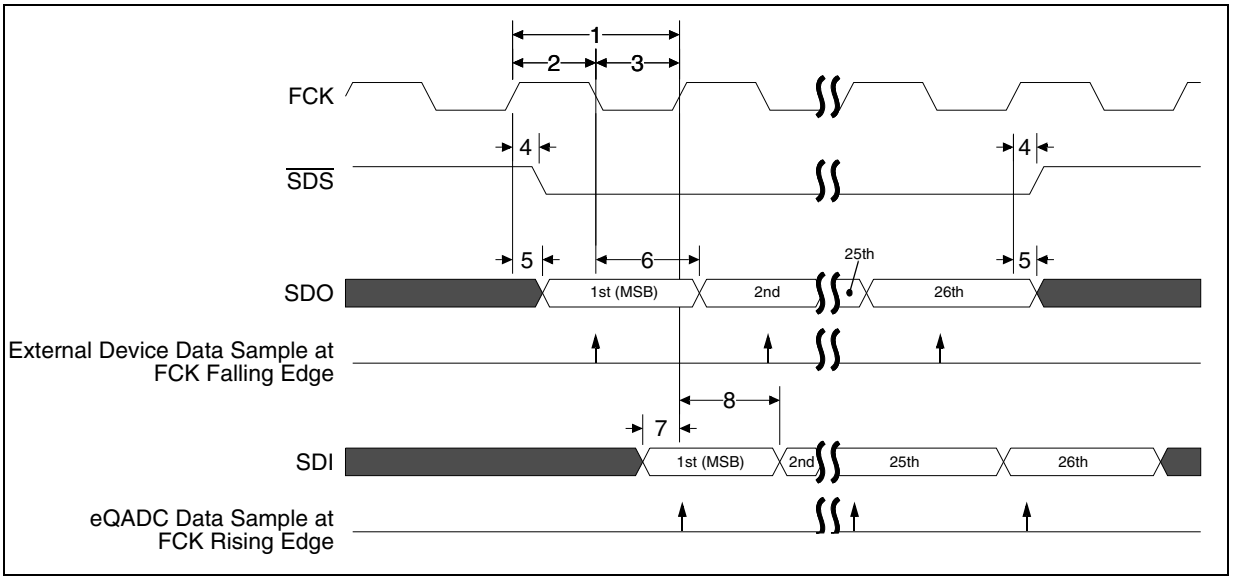
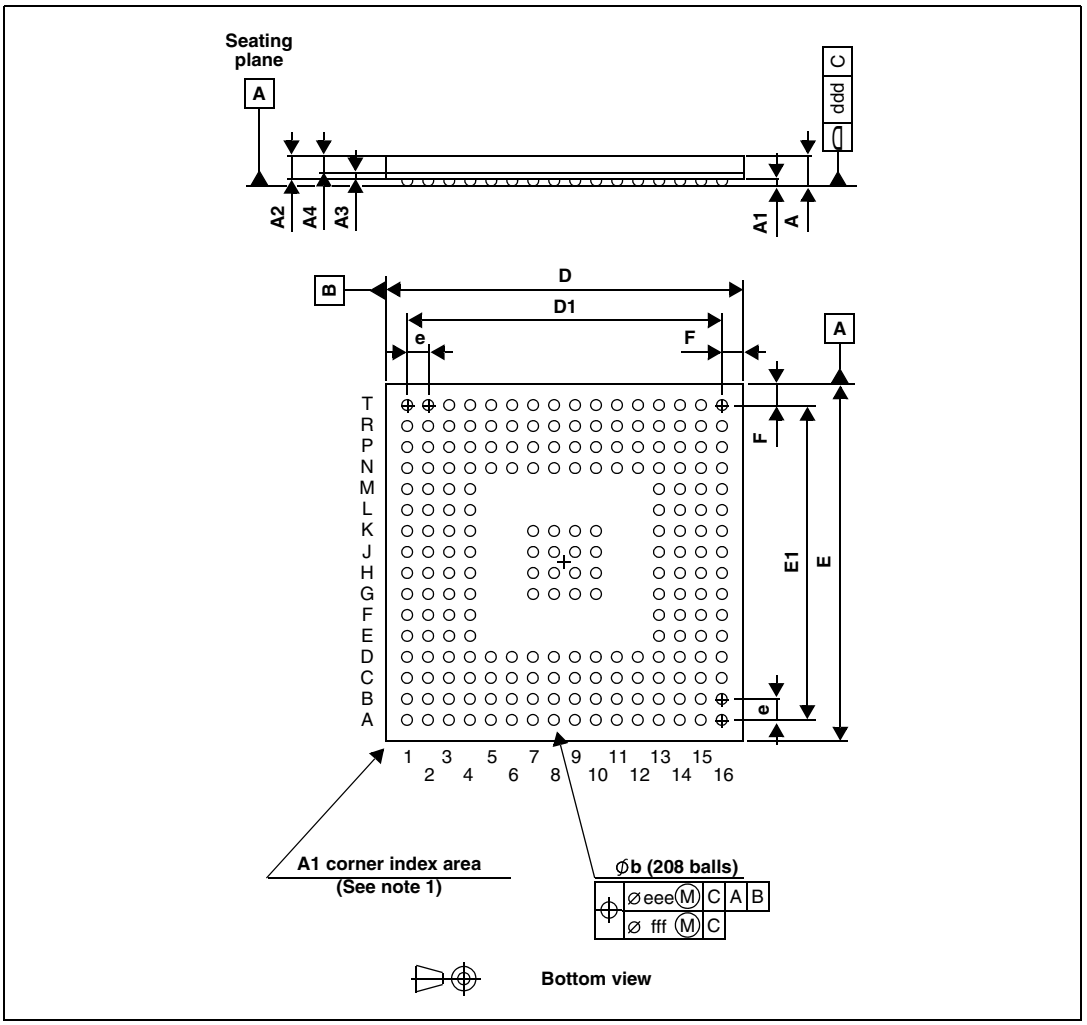


Figure 32. eQADC SSI timing

4.2.2 BGA208



1. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug.
A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1 corner. Exact shape of each corner is optional.

Table 53. LBGA208 mechanical data

Symbol	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A(2)			1.70			0.0669
A1	0.30			0.0118		
A2		1.085			0.0427	
A3		0.30			0.0118	
A4			0.80			0.0315
b(3)	0.50	0.60	0.70	0.0197	0.0236	0.0276

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010	3	Internal release. Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: – WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) – WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: – CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) – CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) – CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: – AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball). AN[8] was on C5 (324-ball) on previous devices. AN[38] Is now on C5 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball) on previous devices. – ANZ function added to AN11 pin Reaction channels added to eTPU2: – RCH0_A (A3) added to ETPU_A[14] (PCR 128) – RCH0_B (A2) added to ETPU_A[20] (PCR 134) – RCH0_C (A2) added to ETPU_A[21] (PCR 135) – RCH1_A (A2) added to ETPU_A[15] (PCR 129) – RCH1_B (A2) added to ETPU_A[9] (PCR 123) – RCH1_C (A2) added to ETPU_A[10] (PCR 124) – RCH2_A (A2) added to ETPU_A[16] (PCR 130) – RCH3_A (A2) added to ETPU_A[17] (PCR 131 – RCH4_A (A2) added to ETPU_A[18] (PCR 132)) – RCH4_B (A2) added to ETPU_A[11] (PCR 125) – RCH4_C (A2) added to ETPU_A[12] (PCR 126) – RCH5_A (A2) added to ETPU_A[19] (PCR 133) – RCH5_B (A2) added to ETPU_A[28] (PCR 142) – RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: – RCH2_B (A2) added to EMIOS[2] (PCR 181) – RCH2_C (A2) added to EMIOS[4] (PCR 183) – RCH3_B (A2) added to EMIOS[10] (PCR 189) – RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: – ETPUA16 (PCR 130) has Medium (was Slow) pad – ETPUA17 (PCR 131) has Medium (was Slow) pad – ETPUA18 (PCR 132) has Medium (was Slow) pad – ETPUA19 (PCR 133) has Medium (was Slow) pad – ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads

Table 56. Revision history (continued)

Date	Revision	Changes
10-Feb-2011 (cont)	5 (cont)	– Added DATA[0:15] to V_{DDE5} in the “signal properties” table. – Updated VSTBY parameters in the “Power/ground segmentation” table. – Updated the parameter symbols and classifications throughout the document. – Updated footnote instances in the “Absolute maximum ratings“ table. – Removed I_{MAXA} footnote in the “Absolute Maximum Ratings” table. – Updated the format of the “EMI (electromagnetic interference) characteristics” table. – Removed the footnote on V_{DDREG} in the “Power management control (PMC) and power on reset (POR) electrical specifications“ table. – Updated values for Vbg, Idd3p3, Por3.3V_r, Por3.3V_f, Por5V_r, and Por5V_f in the “PMC electrical characteristics” table. – Updated “Bandgap reference supply voltage variation” in the “PMC Electrical Characteristics” table. – Removed the “VRC electrical specifications” table as it contained redundant information. – Updated VCE_{SAT} and V_{BE}in the “Recommended power transistors” operating characteristics” table. – Updated V_{IH_LS} in the “DC electrical specifications” table. – Updated the V_{OH_LS} min value in the “DC electrical specifications” table. – Updated I_{DDSTBY} and $I_{DDSTBY150}$ in the “DC electrical specifications” table. – Updated the I_{DDA}/I_{REF}/I_{DDREG} max value in the “DC electrical specifications” table. – Updated I_{ACT_F}, $I_{ACT\_MV\_PU}$, $I_{ACT\_MV\_PD}$, R_{PUPD5K}, $R_{PUPDMTCH}$, and footnotes in the “DC electrical specifications” table. – Updated Medium pad type I_{DD33} values in the “I/O pad V_{RC33} average I_{DDE} specifications” table. – Updated values for V_{OD} in the “DSPI LVDS pad specification“ table. – Removed the footnotes from the “DSPI LVDS pad specifications“ table. – Removed the redundant “XTAL Load Capacitance” parameter instance from the “PLLMRFM electrical specifications” table. – Updated footnotes in the “PLLMRFM electrical specifications” table. – Updated values for OFFNC and GAINNC in the “eQADC conversion specifications (operating)“ table. – Added $DIFF_{max}$, $DIFF_{max2}$, $DIFF_{max4}$, and $DIFF_{cmv}$ parameters to the “eQADC conversion specifications (operating)” table. – Added the maximum operating frequency values in the “Cutoff frequency for additional SRAM wait state” table. – Updated multiple entries in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Removed footnote in the “APC, RWSC, WWSC settings vs. frequency of operation” table. – Updated the Typical values for $T_{dwprogram}$,, $T_{pprogram}$, and $T_{16kpperase}$, and updated the Initial Max values for $T_{128kpperase}$ and $T_{256kpperase}$ in the “Flash program and erase specifications” table. – Changed the voltage in the “Pad AC specifications” table title from 4.5 V to 5.0 V. – Added the maximum LH/HL output delay values for pad type MultiV in the “Pad AC specifications (V_{DDE} = 3.3 V)“ table.

Table 56. Revision history (continued)

Date	Revision	Changes
03-Feb-2012 (cont)	6 (cont)	– Added *Table 17: SPC564A80 External network specification*. – Updated *Figure 8: Core voltage regulator controller external components preferred configuration*. – Changed External Network Parameter Ce min value to “3*2.35µF+5µF” from “2*2.35µF+5µF” in *Table 17: SPC564A80 External network specification*. – Changed Trans. Line (differential Zo) unit to Ω from W in *Table 25: DSPI LVDS pad specification*.
07-Mar-2012	7	– Update table footnotes in *Table 21: DC electrical specifications*.
21-Mar-2012	8	– Minor editorial changes. – In *Section 1.4, “SPC564A80 feature list*, moved “24 unified channels” after “1 x eMIOS”. – In *Table 4,“SPC564A80 signal properties”*/Column “Name” updated the following rows: DSPI_D_SCK /GPIO [98] -Changed “-” to CS[2] DSPI_D_SIN /GPIO[99] -Changed “-” to CS[3]. – In *Table 12,“Thermal characteristics for 324-pin PBGA”*/ Column “Value” added conditional text. – In *Table 21,“DC electrical specifications”* made the following changes: -For the value “V_{OL_S}” parameter changed from “Slow/ medium/multi-voltage pad I/O output low voltage” to “Slow/medium pad I/O output low voltage”. -Added a new row for “$I_{DDSTBY27}$”. -For row “I_{DDSTBY}(operating current 0.95 -1.2V)” added max value “100” and changed typ value from “125” to “35”. -For row “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “110” and changed typ value from “135” to “45”. -For symbol “$I_{DDSTBY\ 150}$(operating current 0.95 -1.2V)” added max value “2000”, changed typ value from “1050” to “790”,C cell changed from “T” to “P” and for symbol “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “2000”, changed typ value from “1050” to “760”, C cell changed from “T” to “P”. -Removed note 9 and note 10 (Characterization based capability) from symbol “V_{OL_HS}”. – Splitted *Table 28,“eQADC conversion specifications (operating)”*into *Table 29,“eQADC single ended conversion specifications (operating)”* and *Table 30,“eQADC differential ended conversion specifications (operating)”*. – In *Table 30 ,“eQADC differential ended conversion specifications (operating)”*made the following changes: -Added the note of $DIFF_{cmv}$ on all of the DIFF specs. -Min value changed from (VRH-VRL)/2-5% to (VRH+VRL)/2-5 % and max value changed from (VRH-VRL)/2+5 % to (VRH+VRL)/2+5 %for DIFFcmv. – In *Table 31 ,“Cutoff frequency for additional SRAM wait state”*made the following changes: -Added note “Max frequencies including 2% PLL FM”. -Max operating frequency changed from “96” to “98” and “150” to “153”. – In *Section 3.13, “Configuring SRAM wait states*, changed text from “SPC564A80 4M Microcontroller Reference Manual “ to “device reference manual”.