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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7cfbr

- 4 slave ports
  - Flash
  - Calibration and EBI bus
  - SRAM
  - Peripheral bridge
- 32-bit internal address, 64-bit internal data paths

1.5.3 eDMA

The enhanced direct memory access (eDMA) controller is a second-generation module capable of performing complex data movements via 64 programmable channels, with minimal intervention from the host processor. The hardware micro-architecture includes a DMA engine which performs source and destination address calculations, and the actual data movement operations, along with an SRAM-based memory containing the transfer control descriptors (TCD) for the channels. This implementation is utilized to minimize the overall block size. The eDMA module provides the following features:

- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- Transfer control descriptor organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a “minor” byte transfer count
- An outer data transfer loop defined by a “major” iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for fixed-priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts optionally enabled
- Support for scatter/gather DMA processing
- Ability to suspend channel transfers by a higher priority channel

1.5.4 Interrupt controller

The INTC (interrupt controller) provides priority-based preemptive scheduling of interrupt requests, suitable for statically scheduled hard real-time systems.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.19 Software watchdog timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.20 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC features:

- Support for CRC-16-CCITT (x25 protocol):
  - $X^{16} + X^{12} + X^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.21 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

1.5.24 Power management controller (PMC)

The power management controller contains circuitry to generate the internal 3.3 V supply and to control the regulation of 1.2 V supply with an external NPN ballast transistor. It also contains low voltage inhibit (LVI) and power-on reset (POR) circuits for the 1.2 V supply, the 3.3 V supply, the 3.3 V/5 V supply of the closest I/O segment (VDDEH1) and the 5 V supply of the regulators (VDDREG).

1.5.25 Nexus port controller

The NPC (Nexus Port Controller) block provides real-time Nexus Class3+ development support capabilities for the SPC564A80 Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 and 2010 standards. MDO port widths of 4 pins and 12 pins are available in all packages.

1.5.26 JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

1.5.27 Development Trigger Semaphore (DTS)

SPC564A80 devices include a system development feature, the Development Trigger Semaphore (DTS) module, that enables software to signal an external tool by driving a persistent (affected only by reset or an external tool) signal on an external device pin. There

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR12 GPIO[8]	External address bus GPIO	P G	01 00	8	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	T3
ADDR13 $\overline{WE}$[2] GPIO[9]	External address bus Write/byte enable GPIO	P A2 G	001 100 000	9	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U3
ADDR14 $\overline{WE}$[3] GPIO[10]	External address bus Write/byte enables GPIO	P A2 G	001 100 000	10	I/O O I/O	VDDE3 Fast	— / Up	— / Up	—	—	U4
ADDR15 GPIO[11]	External address bus GPIO	P G	01 00	11	I/O I/O	VDDE3 Fast	— / Up	— / Up	—	—	V3
ADDR16 FR_A_TX DATA16 GPIO[12]	External address bus Flexray TX data channel A External data bus GPIO	P A1 A2 G	001 010 100 000	12	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P1
ADDR17 $\overline{FR\_A\_TX\_EN}$ DATA17 GPIO[13]	External address bus FlexRay ch. A TX data enable External data bus GPIO	P A1 A2 G	001 010 100 000	13	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	P2
ADDR18 FR_A_RX DATA18 GPIO[14]	External address bus Flexray RX data ch. A External data bus GPIO	P A1 A2 G	001 010 100 000	14	I/O I I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R1
ADDR19 FR_B_TX DATA19 GPIO[15]	External address bus Flexray TX data ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	15	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	R2
ADDR20 $\overline{FR\_B\_TX\_EN}$ DATA20 GPIO[16]	External address bus Flexray TX data enable for ch. B External data bus GPIO	P A1 A2 G	001 010 100 000	16	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	T1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
CAN_C_RX DSPI_D_PCS[4] GPIO[88]	FlexCAN C RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	88	I O I/O	VDDEH6 Slow	— / Up	— / Up	98	L14	R20
eSCI											
SCI_A_TX EMIOS13[8] GPIO[89]	eSCI A TX eMIOS channel GPIO	P A1 G	01 10 00	89	O O I/O	VDDEH6 Medium	— / Up	— / Up	100	J14	N20
SCI_A_RX EMIOS15[8] GPIO[90]	eSCI A RX eMIOS channel GPIO	P A1 G	01 10 00	90	I O I/O	VDDEH6 Medium	— / Up	— / Up	99	K14	P20
SCI_B_TX DSPI_D_PCS[1] GPIO[91]	eSCI B TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	91	O O I/O	VDDEH6 Medium	— / Up	— / Up	87	L13	R21
SCI_B_RX DSPI_D_PCS[5] GPIO[92]	eSCI B RX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	92	I O I/O	VDDEH6 Medium	— / Up	— / Up	84	M13	T19
SCI_C_TX GPIO[244]	eSCI C TX GPIO	P G	01 00	244	O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	W18
SCI_C_RX GPIO[245]	eSCI C RX GPIO	P G	01 00	245	I I/O	VDDEH6 Medium	— / Up	— / Up	—	—	Y19
DSPI											
DSPI_A_SCK[17] DSPI_C_PCS[1] GPIO[93]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	93	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	L22
DSPI_A_SIN[17] DSPI_C_PCS[2] GPIO[94]	— DSPI C peripheral chip select GPIO	— A1 G	— 10 00	94	— O I/O	VDDEH7 Medium	— / Up	— / Up	—	—	L21

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA30 DSPI_C_PCS[3] ETPUA11_O[8] GPIO[144]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	144	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	22	E1	C1
ETPUA31 DSPI_C_PCS[4] ETPUA13_O[8] GPIO[145]	eTPU A channel DSPI C peripheral chip select eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	145	I/O O O I/O	VDDEH1 Medium	— / WKPCFG	— / WKPCFG	21	E2	C2
eMIOS											
EMIOS0 ETPUA0_O[8] ETPUA25_O[8] GPIO[179]	eMIOS channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	179	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	63	T4	AB10
EMIOS1 ETPUA1_O[8] GPIO[180]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	180	I/O O I/O	VDDEH4 Slow	— / Up	— / Up	64	T5	AB11
EMIOS2 ETPUA2_O[8] RCH2_B GPIO[181]	eMIOS channel eTPU A channel (output only) Reaction channel 2B GPIO	P A1 A2 G	001 010 100 000	181	I/O O O I/O	VDDEH4 Slow	— / Up	— / Up	65	N7	W12
EMIOS3 ETPUA3_O[8] GPIO[182]	eMIOS channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	182	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	66	R6	AA11
EMIOS4 ETPUA4_O[8] RCH2_C GPIO[183]	eMIOS channel eTPU A channel (output only) Reaction channel 2C GPIO	P A1 A2 G	001 010 100 000	183	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	67	R5	AB12

Table 6. Signal details (continued)

Signal	Module or Function	Description
DSPI_C_SCK_LVDS- DSPI_C_SCK_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
DSPI_C_SOUT_LVDS- DSPI_C_SOUT_LVDS+	DSPI	LVDS pair used for DSPI_C TSB mode transmission
PCS_B[0] PCS_C[0] PCS_D[0]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—slave select when used in slave mode
PCS_B[1:5] PCS_C[1:5] PCS_D[1:5]	DSPI_B - DSPI_D	Peripheral chip select when device is in master mode—not used in slave mode
SCK_B SCK_C SCK_D	DSPI_B - DSPI_D	DSPI clock—output when device is in master mode; input when in slave mode
SIN_B SIN_C SIN_D	DSPI_B - DSPI_D	DSPI data in
SOUT_B SOUT_C SOUT_D	DSPI_B - DSPI_D	DSPI data out
ADDR[10:31]	EBI	The ADDR[10:31] signals specify the physical address of the bus transaction. The 26 address lines correspond to bits 3-31 of the EBI's 32-bit internal address bus. ADDR[15:31] can be used as Address and Data signals when configured appropriately for a multiplexed external bus. This allows 32-bit data operations, or 16-bit data operations without using DATA[0:15] signals.
ALE	EBI	The Address Latch Enable (ALE) signal is used to demultiplex the address from the data bus. It is asserted while the least significant 16 bits of the address are present in the multiplexed address/data bus.
$\overline{\text{BDIP}}$	EBI	$\overline{\text{BDIP}}$ is asserted to indicate that the master is requesting another data beat following the current one.
$\overline{\text{CS}}$[0:3]	EBI	$\overline{\text{CS}}$x is asserted by the master to indicate that this transaction is targeted for a particular memory bank on the Primary external bus.
DATA[0:31]	EBI	The DATA[0:31] signals contain the data to be transferred for the current transaction.
$\overline{\text{OE}}$	EBI	$\overline{\text{OE}}$ is used to indicate when an external memory is permitted to drive back read data. External memories must have their data output buffers off when $\overline{\text{OE}}$ is negated. $\overline{\text{OE}}$ is only asserted for chip-select accesses.

Table 16. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
9	Por5V_r	CC	C	Nominal POR for rising 5 V V_{DDREG} supply	—	2.67	—	V	
9a	—	CC	C	Variation of POR for rising 5 V V_{DDREG} supply	Por5V_r - 35%	Por5V_r	Por5V_r + 50%	V	
9b	Por5V_f	CC	C	Nominal POR for falling 5 V V_{DDREG} supply	—	2.47	—	V	
9c	—	CC	C	Variation of POR for falling 5 V V_{DDREG} supply	Por5V_f - 35%	Por5V_f	Por5V_f + 50%	V	

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal Vdd regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum Vdd DC target respectively.
5. Minimum loading (<10 mA) for reading trim values from flash, powering internal RC oscillator, and IO consumption during POR.
6. No external load is allowed, except for use as a reference for an external tool.
7. This value is valid only when the internal regulator is bypassed. When the internal regulator is enabled, the maximum external load allowed on the Nexus pads is 30 pF at 40 MHz.
8. Lvi3p3 tracks DC target variation of internal Vdd33 regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum Vdd33 DC target respectively.

3.6.1 Regulator Example

In designs where the SPC564A80 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

3.8 DC electrical specifications

Table 21. DC electrical specifications

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{DD}	SR	—	Core supply voltage	—	1.14		1.32	V
V_{DDE}	SR	—	I/O supply voltage	—	1.62		3.6	V
V_{DDEH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{DDE-EH}	SR	—	I/O supply voltage	—	3.0		5.25	V
V_{RC33}	SR	—	3.3 V regulated voltage(1)	—	3.0	—	3.6	V
V_{DDA}	SR	—	Analog supply voltage	—	4.75(2)	—	5.25	V
V_{INDC}	SR	—	Analog input voltage	—	V_{SSA}-0.3	—	V_{DDA}+0.3	V
$V_{SS} – V_{SSA}$	SR	—	V_{SS} differential voltage	—	–100	—	100	mV
V_{RL}	SR	—	Analog reference low voltage	—	V_{SSA}	—	V_{SSA}+0.1	V
$V_{RL} – V_{SSA}$	SR	—	VRL differential voltage	—	–100	—	100	mV
V_{RH}	SR	—	Analog reference high voltage	—	V_{DDA}-0.1	—	V_{DDA}	V
$V_{RH} – V_{RL}$	SR	—	V_{REF} differential voltage	—	4.75	—	5.25	V
V_{DDF}	SR	—	Flash operating voltage(3)	—	1.14	—	1.32	V
V_{FLASH}(4)	SR	—	Flash read voltage	—	3.0	—	3.6	V
V_{STBY}	SR	—	SRAM standby voltage	Unregulated mode	0.95	—	1.2	V
			Keep-out Range: 1.2V–2V	Regulated mode	2.0	—	5.5	
V_{DDREG}	SR	—	Voltage regulator supply voltage	—	4.75	—	5.25	V
V_{DDPLL}	SR	—	Clock synthesizer operating voltage	—	1.14	—	1.32	V
$V_{SSPLL} – V_{SS}$	SR	—	V_{SSPLL} to V_{SS} differential voltage	—	–100	—	100	mV
V_{IL_S}	CC	C	Slow/medium I/O pad input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDEH}	

Table 24. V_{RC33} pad average DC current(1)

Pad Type	Symbol		C	Period (ns)	Load (2) (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$f_{LVDSCLK}$	CC	D	—		50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}	CC	P	SRC=0b00 or 0b11	150		400	mV
			CC	P	SRC=0b01	90		320	
			CC	P	SRC=0b10	160		480	
6	Common mode voltage (LVDS), VOS	V_{OD}	CC	P		1.06	1.2	1.39	V
7	Rise/Fall time	T_R/T_F	CC	D	—		2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D	—		4		ns

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA2 (1)	CC	–	Variable gain amplifier accuracy (gain=2)(2)				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4 (1)	CC	–	Variable gain amplifier accuracy (gain=4)(2)				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)(5)	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2(5)	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1. Applies only to differential channels.
2. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.
3. At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.
4. Guaranteed 10-bit mono tonicity.
5. Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

Table 33. Flash program and erase specifications(1) (continued)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	3000	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5300	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.
4. Page size is 128 bits (4 words).
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.16 AC specifications

3.16.1 Pad AC specifications

Table 35. Pad AC specifications (5.0 V)(1)

Name		C	Output Delay (ns)(2),(3) Low-to-High / High-to-Low		Rise/Fall Edge (ns)(3),(4)		Drive Load (pF)	SRC/DSC
			Min	Max	Min	Max		MSB,LSB
Medium(5),(6),(7)	CC	D	4.6/3.7	12/12	2.2/2.2	7/7	50	11(8)
	N/A							10(9)
	CC	D	12/13	28/34	5.6/6	15/15	50	01
	CC	D	69/71	152/165	34/35	74/74	50	00
Slow(7),(10)	CC	D	7.3/5.7	19/18	4.4/4.3	14/14	50	11(8)
	N/A							10(9)
	CC	D	26/27	61/69	13/13	34/34	50	01
	CC	D	137/142	320/330	72/74	164/164	50	00
MultiV(11) (High Swing Mode)	CC	D	4.1/3.6	10.3/8.9	3.28/2.98	8/8	50	11(8)
	N/A							10(9)
	CC	D	8.38/6.11	16/12.9	5.48/4.81	11/11	50	01
	CC	D	61.7/10.4	92.2/24.3	42.0/12.2	63/63	50	00
MultiV (Low Swing Mode)	CC	D	2.31/2.34	7.62/6.33	1.26/1.67	6.5/4.4	30	11(8)
Fast(12)	N/A							
pad_i_hv(13)	CC	D	0.5/0.5	1.9/1.9	0.3/0.3	±1.5/1.5	0.5	N/A
pull_hv	CC	D	NA	6000		5000/5000	50	N/A

1. These are worst case values that are estimated from simulation and not tested. The values in the table are simulated at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, $T_A = T_L$ to T_H
2. This parameter is supplied for reference and is not guaranteed by design and not tested.
3. Delay and rise/fall are measured to 20% or 80% of the respective signal.
4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
7. Output delay is shown in *Figure 9: Pad output delay*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
11. Selectable high/low swing IO pad with selectable slew in high swing mode only.
12. Fast pads are 3.3 V pads.
13. Stand alone input buffer. Also has weak pull-up/pull-down.

4. This parameter is guaranteed by characterization before qualification rather than 100% tested.
5. In high swing mode, high/low swing pad Vol and Voh values are the same as those of the slew controlled output pads
6. Medium Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
7. Output delay is shown in *Figure 9*. Add a maximum of one system clock to the output delay for delay with respect to system clock.
8. Can be used on the tester.
9. This drive select value is not supported. If selected, it will be approximately equal to 11.
10. Slow Slew-Rate Controlled Output buffer. Contains an input buffer and weak pullup/pulldown.
11. Selectable high/low swing IO pad with selectable slew in high swing mode only.
12. Stand alone input buffer. Also has weak pull-up/pull-down.

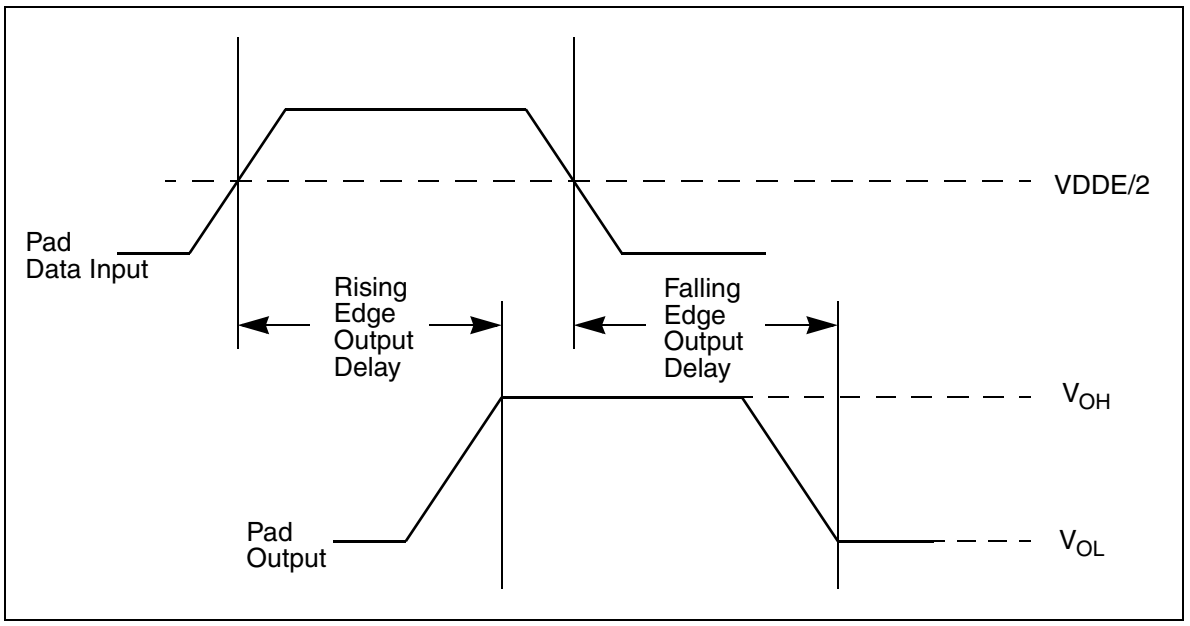


Figure 9. Pad output delay

Table 39. Nexus debug port timing[1] (continued)

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
9	t_{TCYC}	CC	D	TCK Cycle Time	4[6],[7]	—	t_{CYC}
9a	t_{TCYC}	CC	D	Absolute Minimum TCK Cycle Time	100[8]	—	ns
10	t_{TDC}	CC	D	TCK Duty Cycle	40	60	%
11	t_{NTDIS}	CC	D	TDI Data Setup Time	5	—	ns
12	t_{NTDIH}	CC	D	TDI Data Hold Time	25	—	ns
13	t_{NTMSS}	CC	D	TMS Data Setup Time	5	—	ns
14	t_{NTMSH}	CC	D	TMS Data Hold Time	25	—	ns
15	—	CC	D	TDO propagation delay from falling edge of TCK	—	19.5	ns
16	—	CC	D	TDO hold time with respect to TCK falling edge (minimum TDO propagation delay)	5.25	—	ns

1. All Nexus timing relative to MCKO is measured from 50% of MCKO and 50% of the respective signal. Nexus timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10.
2. Achieving the absolute minimum MCKO cycle time may require setting the MCKO divider to more than its minimum setting (NPC_PCR[MCKO_DIV] depending on the actual system frequency being used.
3. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum MCKO period specification.
4. This may require setting the MCO divider to more than its minimum setting (NPC_PCR[MCKO_DIV]) depending on the actual system frequency being used.
5. MDO, $\overline{\text{MSEO}}$, and $\overline{\text{EVTO}}$ data is held valid until next MCKO low cycle.
6. Achieving the absolute minimum TCK cycle time may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.
7. This is a functionally allowable feature. However, this may be limited by the maximum frequency specified by the Absolute minimum TCK period specification.
8. This may require a maximum clock speed (system frequency / 8) that is less than the maximum functional capability of the design (system frequency / 4) depending on the actual system frequency being used.

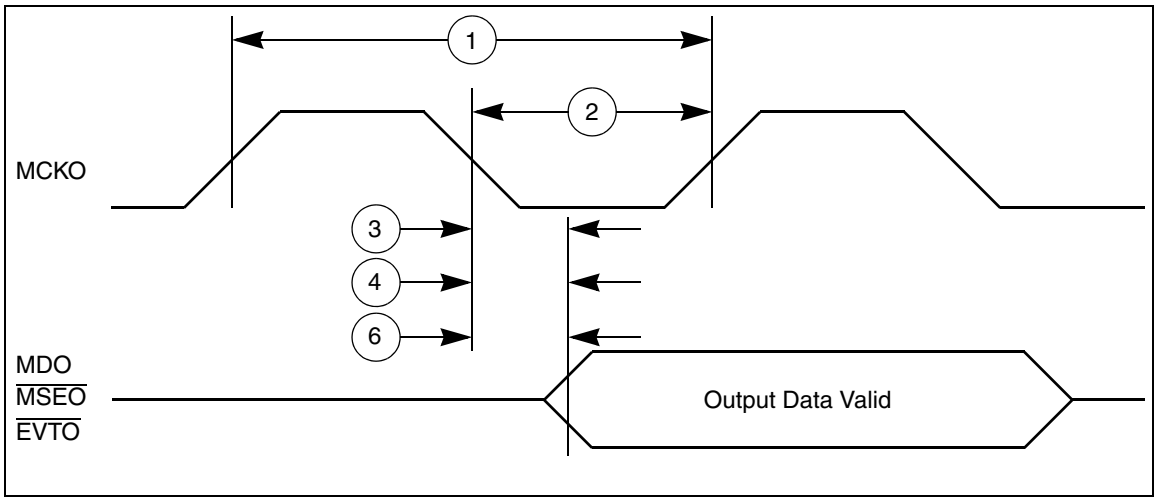
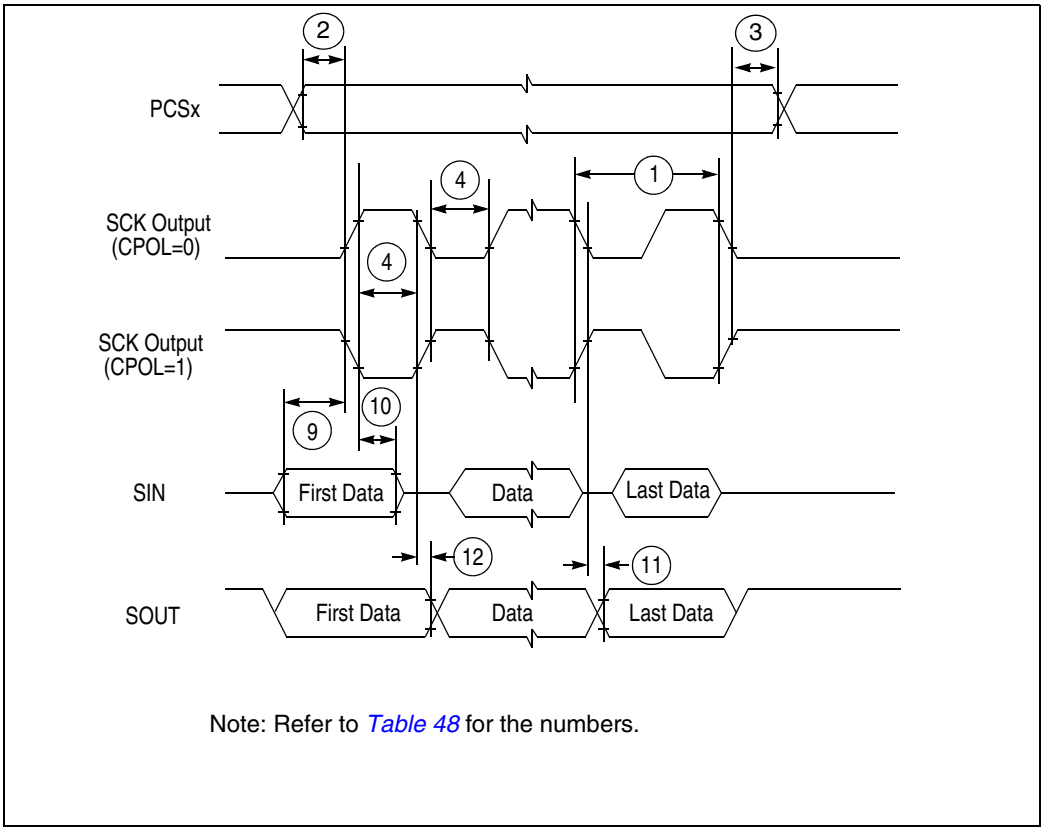


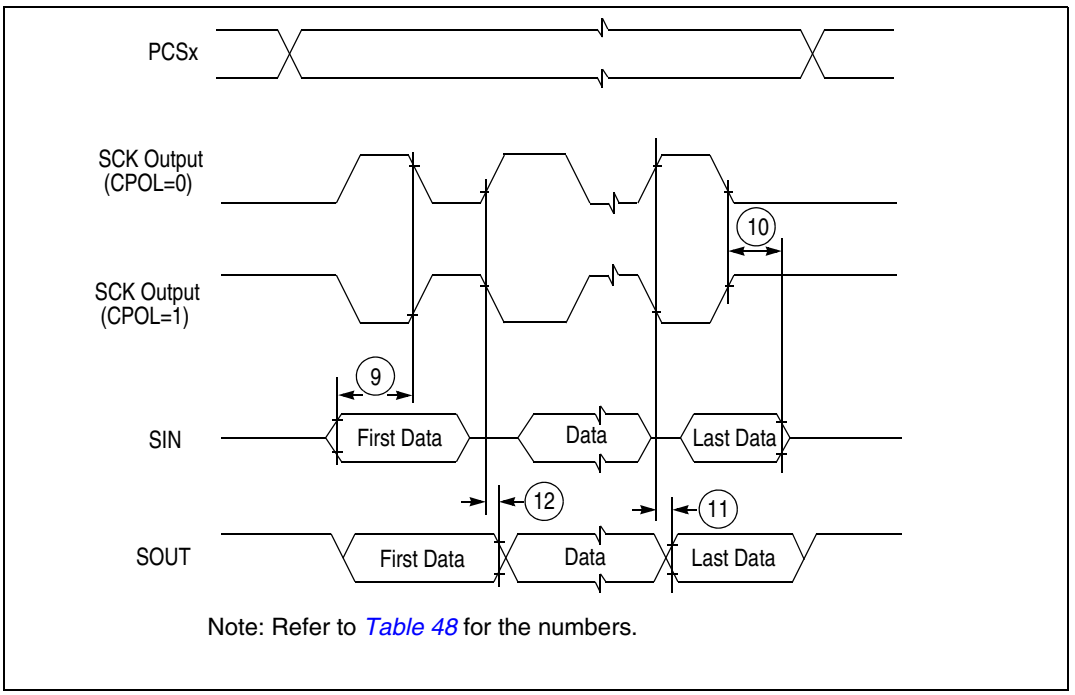
Figure 15. Nexus output timing

3. The minimum DSPI Cycle Time restricts the baud rate selection for given system clock rate. These numbers are calculated based on two SPC564A80 devices communicating over a DSPI link.
4. The actual minimum SCK cycle time is limited by pad performance.
5. For DSPI channels using LVDS output operation, up to 40 MHz SCK cycle time is supported. For non-LVDS output, maximum SCK frequency is 20 MHz. Appropriate clock division must be applied.
6. The maximum value is programmable in DSPI_CTARx[PSSCK] and DSPI_CTARx[CSSCK].
7. Timing met when pcssck = 3(01), and cssck =2 (0000).
8. The maximum value is programmable in DSPI_CTARx[PASC] and DSPI_CTARx[ASC].
9. Timing met when ASC = 2 (0000), and PASC = 3 (01).
10. Timing met when pcssck = 3.
11. Timing met when ASC = 3.
12. This number is calculated assuming the SMPL_PT bitfield in DSPI_MCR is set to 0b10.



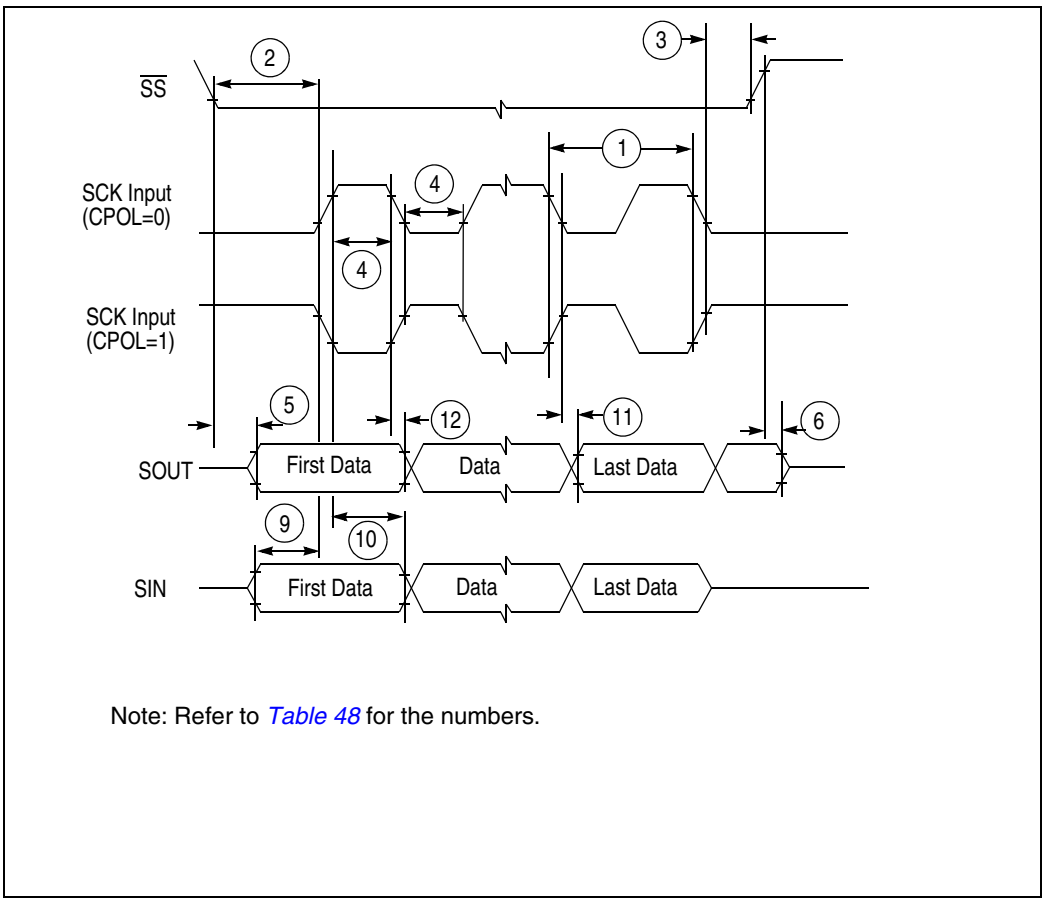
Note: Refer to *Table 48* for the numbers.

Figure 23. DSPI classic SPI timing — master, CPHA = 0



Note: Refer to *Table 48* for the numbers.

Figure 24. DSPI classic SPI timing — master, CPHA = 1



Note: Refer to *Table 48* for the numbers.

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010	3	Internal release. Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: – WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) – WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: – CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) – CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) – CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: – AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball). AN[8] was on C5 (324-ball) on previous devices. AN[38] Is now on C5 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball) on previous devices. – ANZ function added to AN11 pin Reaction channels added to eTPU2: – RCH0_A (A3) added to ETPU_A[14] (PCR 128) – RCH0_B (A2) added to ETPU_A[20] (PCR 134) – RCH0_C (A2) added to ETPU_A[21] (PCR 135) – RCH1_A (A2) added to ETPU_A[15] (PCR 129) – RCH1_B (A2) added to ETPU_A[9] (PCR 123) – RCH1_C (A2) added to ETPU_A[10] (PCR 124) – RCH2_A (A2) added to ETPU_A[16] (PCR 130) – RCH3_A (A2) added to ETPU_A[17] (PCR 131 – RCH4_A (A2) added to ETPU_A[18] (PCR 132)) – RCH4_B (A2) added to ETPU_A[11] (PCR 125) – RCH4_C (A2) added to ETPU_A[12] (PCR 126) – RCH5_A (A2) added to ETPU_A[19] (PCR 133) – RCH5_B (A2) added to ETPU_A[28] (PCR 142) – RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: – RCH2_B (A2) added to EMIOS[2] (PCR 181) – RCH2_C (A2) added to EMIOS[4] (PCR 183) – RCH3_B (A2) added to EMIOS[10] (PCR 189) – RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: – ETPUA16 (PCR 130) has Medium (was Slow) pad – ETPUA17 (PCR 131) has Medium (was Slow) pad – ETPUA18 (PCR 132) has Medium (was Slow) pad – ETPUA19 (PCR 133) has Medium (was Slow) pad – ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010 (cont)	3 (cont)	Signal Details table updated: – Added eTPU2 reaction channels – Changed IRQ[0:15] to two ranges, excluding IRQ6, which does not exist on this device – Changed TCR_A to TCRCLKA (TCR_A is the pin name, not the signal name) – Changed WE_BE[0:1] to WE_BE[0:3] (2 new signals added to Rev. 2). Also changed notation from “WE_BE[n]” to “WE[n]/BE[n]” to be consistent. Changes to Power/ground segmentation table: – ADDR[20:21] removed from VDDE2 segment; they are in VDDE-EH – CAL_CS1 removed from VDDE12 segment (there is no CAL_CS1 on this device) – CAL_EVTO and CAL_MCKO removed from VDDE12 segment. Those pins do not exist – VDDE-VDDEH renamed to VDDE-EH – EMIOS24 removed from VDDEH segment. That pin does not exist. – ETPUA[0:9] added to VDDEH4 segment – Renamed TCR_A in VDDEH4 segment to TCRCLKA. – EXTAL and XTAL added to VDDEH6 segment – AN15-FCK added to VDDEH7 segment – GPIO98, GPIO99, GPIO206, GPIO207 and GPIO219 added to VDDEH7 segment. – MSEO1 added to VDDEH7 segment – Power segment VDDEH1A renamed to VDDEH1 Changes to 176-pin package pinout: – Changed pin 9 from AN38 to AN8. – Added note that pin 96 (VSS) should be tied low. Changes to 208-ball package ballmap: – Changed ball B3 from AN38 to AN8. – Added note that ball N13 (VSS) should be tied low. 324-ball package ballmap updated for Rev. 2 silicon – Renamed VDDA (A6) to VDDA0 – Renamed VSSA (A7) to VSSA0 – AN8 was on ball C5; it is now on D6 – AN38 was on ball D6; it is now on C5 – Renamed VSSA (A15) to VSSA1 – Renamed VDDA (C15) to VDDA1 – Rename VSSA (B15) to VSSA1 BGA288 package is no longer offered Changes to features list: – Correction: there are 6 reaction channels (was noted as 5) – Development Trigger Semaphore (DTS) added to features list and feature details – FlexRay module now has 128 message buffers (was 64) and ECC support Added note after JTAG pin AC electrical characteristics table detailing JTAG EVTI and RDY signal clocking with TCK. This affects debuggers.