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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7cfby

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison (continued)

Feature		SPC564A80	SPC563M64	SPC564A70
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch.(1)	307 ch.	486 ch.(1)
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V(2)	5 V, 3.3 V(3)	5 V, 3.3 V(2)
Low-power modes		Stop Mode Slow Mode		
Packages		LQFP176(4) LBGA208(4) PBGA Known Good Die (KGD) 496-pin CSP(5)	LQFP100 LQFP144 LQFP176 LBGA208 496-pin CSP(5)	LQFP176(4) LBGA208(4) PBGAKnown Good Die (KGD) 496-pin CSP(5)

1. 199 interrupt vectors are reserved.
2. 5 V single supply only for LQFP176.
3. 5 V single supply only for LQFP144 and LQFP100.
4. Pinout compatible with STMicroelectronics' SPC563M64 devices.
5. For ST calibration tool only.

1.4 SPC564A80 feature list

- 150 MHz e200z4 Power Architecture core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 4 MB on-chip flash memory with ECC and Read While Write (RWW)
  - 192 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 5 × 4 crossbar switch (XBAR)
  - 24-entry MMU
  - External Bus Interface (EBI) with slave and master port
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 sub-modules
  - Junction temperature sensor
- Interrupts
  - Configurable interrupt controller (with NMI)
  - 64-channel DMA
- Serial channels
  - 3 × eSCI
  - 3 × DSPI (2 of which support downstream Micro Second Channel [MSC])
  - 3 × FlexCAN with 64 messages each
  - 1 × FlexRay module (V2.1) up to 10 Mbit/s with dual or single channel and 128 message objects and ECC
- 1 × eMIOS: 24 unified channels
- 1 × eTPU2 (second generation eTPU)
  - 32 standard channels
  - 1 × reaction module (6 channels with three outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- Nexus
  - Class 3+ for the e200z4 core
  - Class 1 for the eTPU
- JTAG (5-pin)

M	BDIP	TCRCLKA	CS1	CS0					VDDE2	VDDE2	VSS
N	CS3	CS2	WE1	WE0					VSS	VSS	VDDE2
P	ADDR16	ADDR17	RD_WR	VRC33					VSS	VSS	VDDE2
R	ADDR18	ADDR19	VDDE-EH	TA							
T	ADDR20	ADDR21	ADDR12	TS							
U	ADDR22	ADDR23	ADDR13	ADDR14							
V	ADDR24	ADDR25	ADDR15	ADDR31							
W	ADDR26	VDDE-EH	ADDR30	VSS	VDD	VDDE2	VRC33	VDDE2	DATA11	DATA12	DATA14
Y	ADDR28	ADDR27	VSS	VDD	VDDE2	DATA8	DATA9	DATA10	GPIO207	DATA13	DATA15
AA	ADDR29	VSS	VDD	VDDE2	DATA1	VDDE2	GPIO206	DATA5	DATA7	VDDE2	EMIOS3
AB	VSS	VDD	VDDE2	DATA0	DATA2	DATA3	DATA4	DATA6	OE	EMIOS0	EMIOS1
	1	2	3	4	5	6	7	8	9	10	11

Figure 5. 324-pin PBGA package ballmap (southwest, viewed from above)

2.4 Signal summary

Table 4. SPC564A80 signal properties

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7] During Reset	Status[7] After Reset	Package pin # 176	Package pin # 208	Package pin # 324
GPIO											
EMIOS14[8] GPIO[203]	eMIOS channel GPIO	P G	01 00	203	O I/O	VDDEH7 Slow	— / Up	— / Up	—	—	H20
EMIOS15[8] GPIO[204]	eMIOS channel GPIO	P G	01 00	204	O I/O	VDDEH7 Slow	— / Up	—/ Up	—	—	H21
GPIO[206] ETRIG0	GPIO / eQADC Trigger Input	G	00	206	I/O[9]	VDDEH7 Slow[10]	— / Up	— / Up	143	R4	AA7
GPIO[207] ETRIG1	GPIO / eQADC Trigger Input	G	00	207	I/O[9]	VDDEH7 Slow	— / Up	— / Up	144	P5	Y9
GPIO[219]	GPIO	G	—	219[11]	I/O	VDDEH7 MultiV[12]	— / Up	— / Up	122	T6	—
Reset / Configuration											
$\overline{\text{RESET}}$	External Reset Input	P	—	—	I	VDDEH6 Slow	$\overline{\text{RESET}}$ / Up	$\overline{\text{RESET}}$ / Up	97	L16	R22
$\overline{\text{RSTOUT}}$	External Reset Output	P	01	230	O	VDDEH6 Slow	$\overline{\text{RSTOUT}}$ / Down	$\overline{\text{RSTOUT}}$ / Down	102	K15	P21
PLLREF $\overline{\text{IRQ}}$[4] ETRIG2 GPIO[208]	FMPLL Mode Selection External Interrupt Request eQADC Trigger Input GPIO	P A1 A2 G	001 010 100 000	208	I I I I/O	VDDEH6 Slow	— / Up	PLLREF / Up	83	M14	V21
PLLCFG1[13] $\overline{\text{IRQ}}$[5] DSPI_D_SOUT GPIO[209]	— External interrupt request DSPI D data output GPIO	— A1 A2 G	— 010 100 000	209	— I O I/O	VDDEH6 Medium	— / Up	— / Up	—	—	U20
RSTCFG GPIO[210]	RSTCFG GPIO	P G	01 00	210	I I/O	VDDEH6 Slow	— / Down	—	—	—	P22

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
DATA7 ADDR23 GPIO[35]	External data bus External address bus GPIO	P A1 G	001 010 000	35	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA9
DATA8 ADDR24 GPIO[36]	External data bus External address bus GPIO	P A1 G	001 010 000	36	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y6
DATA9 ADDR25 GPIO[37]	External data bus External address bus GPIO	P A1 G	001 010 000	37	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y7
DATA10 ADDR26 GPIO[38]	External data bus External address bus GPIO	P A1 G	001 010 000	38	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y8
DATA11 ADDR27 GPIO[39]	External data bus External address bus GPIO	P A1 G	001 010 000	39	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W9
DATA12 ADDR28 GPIO[40]	External data bus External address bus GPIO	P A1 G	001 010 000	40	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W10
DATA13 ADDR29 GPIO[41]	External data bus External address bus GPIO	P A1 G	001 010 000	41	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y10
DATA14 ADDR30 GPIO[42]	External data bus External address bus GPIO	P A1 G	001 010 000	42	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	W11
DATA15 ADDR31 GPIO[43]	External data bus External address bus GPIO	P A1 G	001 010 000	43	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	Y11
RD_$\overline{WR}$ GPIO[62]	External read/write GPIO	P G	01 00	62	I/O I/O	VDDE2 Fast	— / Up	— / Up	—	—	P3

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7] During Reset	Status[7] After Reset	Package pin # 176	Package pin # 208	Package pin # 324
$\overline{BDIP}$ GPIO[63]	External burst data in progress GPIO	P G	01 00	63	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	M1
$\overline{WE}$[0]/$\overline{BE}$[0] GPIO[64]	External write/byte enable GPIO	P G	01 00	64	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	N4
$\overline{WE}$[1]/$\overline{BE}$[1] GPIO[65]	External write/byte enable GPIO	P G	01 00	65	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	N3
$\overline{OE}$ GPIO[68]	External output enable GPIO	P G	01 00	68	O I/O	VDDE2 Fast	— / Up	— / Up	—	—	AB9
$\overline{TS}$ ALE GPIO[69]	External transfer start Address latch enable GPIO[69]	P A1 G	001 010 000	69	I/O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	T4
$\overline{TA}$ TS[8] GPIO[70]	External transfer acknowledge External transfer start GPIO	P A1 G	001 010 000	70	I/O O I/O	VDDE2 Fast	— / Up	— / Up	—	—	R4
Calibration Bus											
CAL_$\overline{CS0}$	Calibration chip select	P	01	336	O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{CS2}$ CAL_ADDR[10] CAL_$\overline{WE}$[2]/$\overline{BE}$[2]	Calibration chip select Calibration address bus Calibration write/byte enable	P A A2	001 010 100	338	O I/O O	VDDE12 Fast		— / —	—	—	—
CAL_$\overline{CS3}$ CAL_ADDR[11] CAL_$\overline{WE}$[3]/$\overline{BE}$[3]	Calibration chip select Calibration address bus Calibration write/byte enable	P A A2	001 010 100	339	O I/O O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[12] CAL_$\overline{WE}$[2]/$\overline{BE}$[2]	Calibration address bus Calibration write/byte enable	P A	01 10	340	I/O O	VDDE12 Fast		— / —	—	—	—
CAL_ADDR[13] CAL_$\overline{WE}$[3]/$\overline{BE}$[3]	Calibration address bus Calibration write/byte enable	P A	01 10	340	I/O O	VDDE12 Fast		— / —	—	—	—

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN14 - SDI MA2 ETPUA27_O[8] SDI	Single-ended Analog Input MUX Address 2 eTPU A channel (output only) eQADC Serial Data In	P A1 A2 G	001 010 100 000	217	I O O I	VDDEH7[19] Medium	I / —	AN[14] / —	146	C12	C16
AN15 - FCK FCK ETPUA29_O[8]	Single-ended Analog Input eQADC Free Running Clock eTPU A channel (output only)	P A1 A2	001 010 100	218	I O O	VDDEH7[19] Medium	I / —	AN[15] / —	145	C13	D16
AN16	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[16] / —	3	C6	B7
AN17	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[17] / —	2	C4	C6
AN18	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[18] / —	1	D5	D9
AN19	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[19] / —	—	—	B6
AN20	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[20] / —	—	—	C7
AN21	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[21] / —	173	B4	C8
AN22	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[22] / —	161	B8	C11
AN23	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[23] / —	160	C9	B11
AN24	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[24] / —	159	D8	D12
AN25	Single-ended Analog Input	P	—	—	I	VDDA Analog	I / —	AN[25] / —	158	B9	C12

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ETPUA18 DSPI_D_PCS[3] RCH4_A GPIO[132]	eTPU A channel DSPI D peripheral chip select Reaction channel 4A GPIO	P A1 A2 G	001 010 100 000	132	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	37	H4	F4
ETPUA19 DSPI_D_PCS[4] RCH5_A GPIO[133]	eTPU A channel DSPI D peripheral chip select Reaction channel 5A GPIO	P A1 A2 G	001 010 100 000	133	I/O O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	36	J2	G2
ETPUA20 $\overline{\text{IRQ}}$[8] RCH0_B FR_A_TX GPIO[134]	eTPU A channel External interrupt request Reaction channel 0B Flexray TX data channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	134	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	35	J1	G1
ETPUA21 $\overline{\text{IRQ}}$[9] RCH0_C FR_A_RX GPIO[135]	eTPU A channel External interrupt request Reaction channel 0C Flexray RX channel A GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	135	I/O I O I I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	34	G4	E4
ETPUA22 $\overline{\text{IRQ}}$[10] ETPUA17_O[8] GPIO[136]	eTPU A channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	136	I/O I O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	32	H2	F2
ETPUA23 $\overline{\text{IRQ}}$[11] ETPUA21_O[8] $\overline{\text{FR\_A\_TX\_EN}}$ GPIO[137]	eTPU A channel External interrupt request eTPU A channel (output only) Flexray ch. A TX enable GPIO	P A1 A2 A3 G	0001 0010 0100 1000 0000	137	I/O I O O I/O	VDDEH1 Slow	— / WKPCFG	— / WKPCFG	30	H1	F1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field (3)	PCR (4)	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDDEH7B	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH7B	138	—	—
VSS	Ground	—		—	I	—	I / —	VSS	15, 29, 43, 57, 72, 90, 94, 96, 108, 115, 127, 133, 140	A1, A16, B2, B15, C3, C14, D4, D13, G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10, M16, N4, N13, P3, P14, R2, R15, T1, T16	A1, A22, B2, B21, C3, C20, D4, D19, J9, J10, J11, J12, J13, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M11, M12, M13, M14, N9, N10, N12, N13, N14, P9, P10, P12, P13, P14, T21, T22, W4,W19, Y3, Y20, AA2, AA21, AB1, AB22

1. For each pin in the table, each line in the Function column is a separate function of the pin. For all I/O pins the selection of primary pin function or secondary function or GPIO is done in the SIU except where explicitly noted. See the Signal details table for a description of each signal.
2. The P/A/G column indicates the position a signal occupies in the muxing order for a pin—Primary, Alternate 1, Alternate 2, Alternate 3, or GPIO. Signals are selected by setting the PA field value in the appropriate PCR register in the SIU module. The PA field values are as follows: P - 0b0001, A1 - 0b0010, A2 - 0b0100, A3 - 0b1000, or G - 0b0000. Depending on the register, the PA field size can vary in length. For PA fields having fewer than four bits, remove the appropriate number of leading zeroes from these values.
3. The Pad Configuration Register (PCR) PA field is used by software to select pin function.
4. Values in the PCR No. column refer to registers in the System Integration Unit (SIU). The actual register name is “SIU_PCR” suffixed by the PCR number. For example, PCR[190] refers to the SIU register named SIU_PCR190.
5. The VDDE and VDDEH supply inputs are broken into segments. Each segment of slow I/O pins (VDDEH) may have a separate supply in the 3.3 V to 5.0 V range (-10%/+5%). Each segment of fast I/O (VDDE) may have a separate supply in the 1.8 V to 3.3 V range (+/- 10%).
6. See *Table 5* for details on pad types.

3 Electrical characteristics

This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications for the SPC564A80 series of MCUs.

The electrical specifications are preliminary and are from previous designs, design simulations, or initial evaluation. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

3.1 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in *Table 8* are used and the parameters are tagged accordingly in the tables where appropriate.

Table 8. Parameter classifications

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

Note: The classification is shown in the column labeled “C” in the parameter tables where appropriate.

Table 16. PMC Electrical Characteristics (continued)

ID	Name			Parameter	Min	Typ	Max	Unit	Notes
9	Por5V_r	CC	C	Nominal POR for rising 5 V V_{DDREG} supply	—	2.67	—	V	
9a	—	CC	C	Variation of POR for rising 5 V V_{DDREG} supply	Por5V_r - 35%	Por5V_r	Por5V_r + 50%	V	
9b	Por5V_f	CC	C	Nominal POR for falling 5 V V_{DDREG} supply	—	2.47	—	V	
9c	—	CC	C	Variation of POR for falling 5 V V_{DDREG} supply	Por5V_f - 35%	Por5V_f	Por5V_f + 50%	V	

1. Using external ballast transistor.
2. Min range is extended to 10% since Lvi1p2 is reprogrammed from 1.2 V to 1.16 V after power-on reset.
3. LVI for falling supply is calculated as LVI rising – LVI hysteresis.
4. Lvi1p2 tracks DC target variation of internal Vdd regulator. Minimum and maximum Lvi1p2 correspond to minimum and maximum Vdd DC target respectively.
5. Minimum loading (<10 mA) for reading trim values from flash, powering internal RC oscillator, and IO consumption during POR.
6. No external load is allowed, except for use as a reference for an external tool.
7. This value is valid only when the internal regulator is bypassed. When the internal regulator is enabled, the maximum external load allowed on the Nexus pads is 30 pF at 40 MHz.
8. Lvi3p3 tracks DC target variation of internal Vdd33 regulator. Minimum and maximum Lvi3p3 correspond to minimum and maximum Vdd33 DC target respectively.

3.6.1 Regulator Example

In designs where the SPC564A80 microcontroller's internal regulators are used, a ballast is required for generation of the 1.2 V internal supply. No ballast is required when an external 1.2 V supply is used.

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1),(2)

Max. Flash Operating Frequency (MHz)(3)	APC(4)	RWSC(4)	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. TBD: To Be Defined.
3. Max frequencies including 2% PLL FM.
4. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	45	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	55	160(4)	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	300	1000	5000	ms

3.17.2 IEEE 1149.1 interface timing

Table 38. JTAG pin AC electrical characteristics[1]

#	Symbol		C	Characteristic	Min. Value	Max. Value	Unit
1	t_{JCYC}	CC	D	TCK Cycle Time	100	—	ns
2	t_{JDC}	CC	D	TCK Clock Pulse Width	40	60	ns
3	$t_{TCKRISE}$	CC	D	TCK Rise and Fall Times (40% - 70%)	—	3	ns
4	t_{TMSS}, t_{TDIS}	CC	D	TMS, TDI Data Setup Time	5	—	ns
5	t_{TMSH}, t_{TDIH}	CC	D	TMS, TDI Data Hold Time	25	—	ns
6	t_{TDOV}	CC	D	TCK Low to TDO Data Valid	—	22[2]	ns
7	t_{TDOI}	CC	D	TCK Low to TDO Data Invalid	0	—	ns
8	t_{TDOHZ}	CC	D	TCK Low to TDO High Impedance	—	22	ns
9	t_{JCMPPW}	CC	D	JCOMP Assertion Time	100	—	ns
10	t_{JCMPS}	CC	D	JCOMP Setup Time to TCK Low	40	—	ns
11	t_{BSDV}	CC	D	TCK Falling Edge to Output Valid	—	50	ns
12	t_{BSDVZ}	CC	D	TCK Falling Edge to Output Valid out of High Impedance	—	50	ns
13	t_{BSDHZ}	CC	D	TCK Falling Edge to Output High Impedance	—	50	ns
14	t_{BSDST}	CC	D	Boundary Scan Input Valid to TCK Rising Edge	25[3]	—	ns
15	t_{BSDHT}	CC	D	TCK Rising Edge to Boundary Scan Input Invalid	25[3]	—	ns

1. JTAG timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, $T_A = T_L$ to T_H, and C_L = 30 pF with DSC = 0b10, SRC = 0b11. These specifications apply to JTAG boundary scan only. See *Table 39* for functional specifications.
2. Pad delay is 8–10 ns. Remainder includes TCK pad delay, clock tree delay logic delay and TDO output pad delay.
3. For 20 MHz TCK.

Note: The Nexus/JTAG Read/Write Access Control/Status Register (RWCS) write (to begin a read access) or the write to the Read/Write Access Data Register (RWD) (to begin a write access) does not actually begin its action until 1 JTAG clock (TCK) after leaving the JTAG Update-DR state. This prevents the access from being performed and therefore will not signal its completion via the READY (RDY) output unless the JTAG controller receives an additional TCK. In addition, EVTI is not latched into the device unless there are clock transitions on TCK.

The tool/debugger must provide at least one TCK clock for the EVTI signal to be recognized by the MCU. When using the RDY signal to indicate the end of a Nexus read/write access, ensure that TCK continues to run for at least 1 TCK after leaving the Update-DR state. This can be just a TCK with TMS low while in the Run-Test/Idle state or by continuing with the

3.17.4 External Bus Interface (EBI) and calibration bus interface timing

Table 41. External Bus Interface maximum operating frequency

Port Width	Multiplexed Mode	ADDR[12:15] Pin Usage	ADDR[16:31] Pin Usage	DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	ADDR[12:15]	GPIO	ADDR[16:31] DATA[0:15]	66 MHz(1)
16-bit	No	ADDR[12:15]	ADDR[16:31]	DATA[0:15]	33 MHz(2),(3)
32-bit	Yes	ADDR[12:15]	ADDR[16:31] DATA[16:31]	DATA[0:15]	33 MHz(2),(3)

1. Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz.
2. System Frequency must be ≤132 MHz and SIU_ECCR[EBDF] set to divide by four.
3. Pad restrictions limit the maximum operating frequency.

Table 42. Calibration bus interface maximum operating frequency

Port Width	Multiplexed Mode	CAL_ADDR[12:15] Pin Usage	CAL_ADDR[16:30] Pin Usage	CAL_DATA[0:15] Pin Usage	Max. Operating Frequency
16-bit	Yes	GPIO	GPIO	CAL_ADDR[12:30] CAL_DATA[0:15]	66 MHz(1)
16-bit	No	CAL_ADDR[12:15]	CAL_ADDR[16:30]	CAL_DATA[0:15]	66 MHz(1)
32-bit	Yes	CAL_WE[2:3] CAL_DATA[31]	CAL_ADDR[16:30] CAL_DATA[16:30]	CAL_ADDR[0:15] CAL_DATA[0:15]	66 MHz(1)

1. Set SIU_ECCR[EBDF] to divide by two or divide by four if the system frequency is greater than 66 MHz

Table 43. External bus interface (EBI) and calibration bus operation timing (1)

#	Symbol		C	Characteristic	66 MHz (ext. bus)(2)		Unit	Notes
					Min	Max		
1	T_C	CC	P	CLKOUT Period	15.2	—	ns	Signals are measured at 50% V_{DDE}.
2	t_{CDC}	CC	D	CLKOUT duty cycle	45%	55%	T_C	
3	t_{CRT}	CC	D	CLKOUT rise time	—	(3)	ns	
4	t_{CFT}	CC	D	CLKOUT fall time	—	(3)	ns	
5	t_{COH}	CC	D	CLKOUT Posedge to Output Signal Invalid or High Z(Hold Time) – ADDR[8:31] – CS[0:3] – DATA[0:31] – OE – RD_$\overline{WR}$ – TS – $\overline{WE}$[0:3]/$\overline{BE}$[0:3]	1.3	—	ns	

Table 48. DSPI timing[1],[2] (continued)

#	Symbol		C	Characteristic	Condition	Min.	Max.	Unit
9	t_{SUI}	CC	Data Setup Time for Inputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.5–5.5 V	20	—	ns
			D		V_{DDEH}=3–3.6 V	23.5	—	
			D	Slave		2	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		8	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.5–5.5 V	20	—	
			D		V_{DDEH}=3–3.6 V	23.5	—	
10	t_{HI}	CC	Data Hold Time for Inputs					
			D	Master (MTFE = 0)		-4	—	ns
			D	Slave		7	—	
			D	Master (MTFE = 1, CPHA = 0)[12]		21	—	
			D	Master (MTFE = 1, CPHA = 1)		-4	—	
11	t_{SUO}	CC	Data Valid (after SCK edge)					
			D	Master (MTFE = 0)	V_{DDEH}=4.5–5.5 V	—	5	ns
			D		V_{DDEH}=3–3.6 V	—	6.3	
			D	Slave	V_{DDEH}=4.5–5.5 V	—	25	
			D		V_{DDEH}=3–3.6 V	—	27	
			D	Master (MTFE = 1, CPHA = 0)		—	21	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.5–5.5 V	—	5	
			D		V_{DDEH}=3–3.6 V	—	6.3	
12	t_{HO}	CC	Data Hold Time for Outputs					
			D	Master (MTFE = 0)	V_{DDEH}=4.5–5.5 V	–5	—	ns
			D		V_{DDEH}=3 –3.6 V	–7.5	—	
			D	Slave		5.5	—	
			D	Master (MTFE = 1, CPHA = 0)		3	—	
			D	Master (MTFE = 1, CPHA = 1)	V_{DDEH}=4.5–5.5 V	–5	—	
			D		V_{DDEH}=3–3.6 V	–7.5	—	

1. All DSPI timing specifications use the fastest slew rate (SRC = 0b11) on medium-speed pads. DSPI signals using slow pads have an additional delay based on the slew rate. DSPI timing is specified at V_{DDEH} = 3 to 3.6 V and V_{DDEH} = 4.5 to 5.5 V, $T_A = T_L$ to T_H, and C_L = 50 pF with SRC = 0b11.
2. Data is verified at f_{SYS} = 102 MHz and 153 MHz (100 MHz and 150 MHz + 2% frequency modulation).

3.17.9 eQADC SSI timing

Table 49. eQADC SSI timing characteristics (pads at 3.3 V or at 5.0 V)(1)

CLOAD = 25 pF on all outputs. Pad drive strength set to maximum.								
#	Symbol		C	Rating	Min	Typ	Max	Unit
1	f_{FCK}	CC	D	FCK Frequency (2), (3)	1/17		1/2	f_{SYS_CLK}
1	t_{FCK}	CC	D	FCK Period (t_{FCK} = 1/ f_{FCK})	2		17	t_{SYS_CLK}
2	t_{FCKHT}	CC	D	Clock (FCK) High Time	t_{SYS_CLK} − 6.5		$_{9*}$ t_{SYS_CLK} + 6.5	ns
3	t_{FCKLT}	CC	D	Clock (FCK) Low Time	t_{SYS_CLK} − 6.5		$_{8*}$ t_{SYS_CLK} + 6.5	ns
4	t_{SDS_LL}	CC	D	SDS Lead/Lag Time	-7.5		7.5	ns
5	t_{SDO_LL}	CC	D	SDO Lead/Lag Time	-7.5		7.5	ns
6	t_{DVFE}	CC	D	Data Valid from FCK Falling Edge (t_{FCKLT}+t_{SDO_LL})	1			ns
7	t_{EQ_SU}	CC	D	eQADC Data Setup Time (Inputs)	22			ns
8	t_{EQ_HO}	CC	D	eQADC Data Hold Time (Inputs)	1			ns

1. SS timing specified at f_{SYS} = 80 MHz, V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 4.5 V to 5.5 V, T_A = T_L to T_H, and C_L = 50 pF with SRC = 0b00.
2. Maximum operating frequency is highly dependent on track delays, master pad delays, and slave pad delays.
3. FCK duty is not 50% when it is generated through the division of the system clock by an odd number.

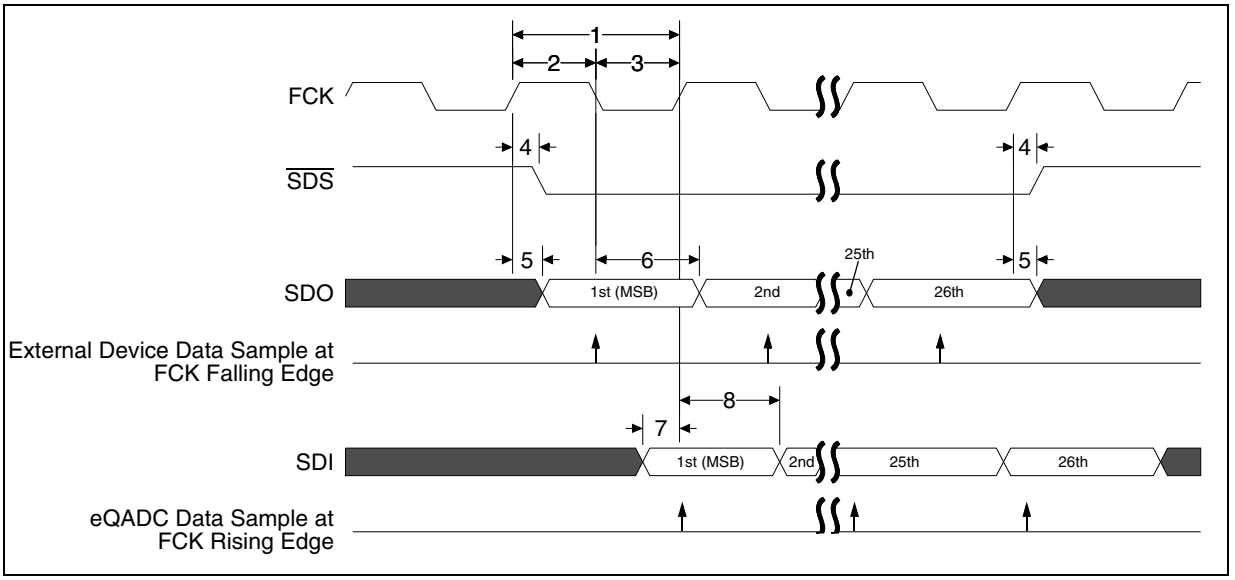

Figure 32. eQADC SSI timing

Figure 35. Product code structure

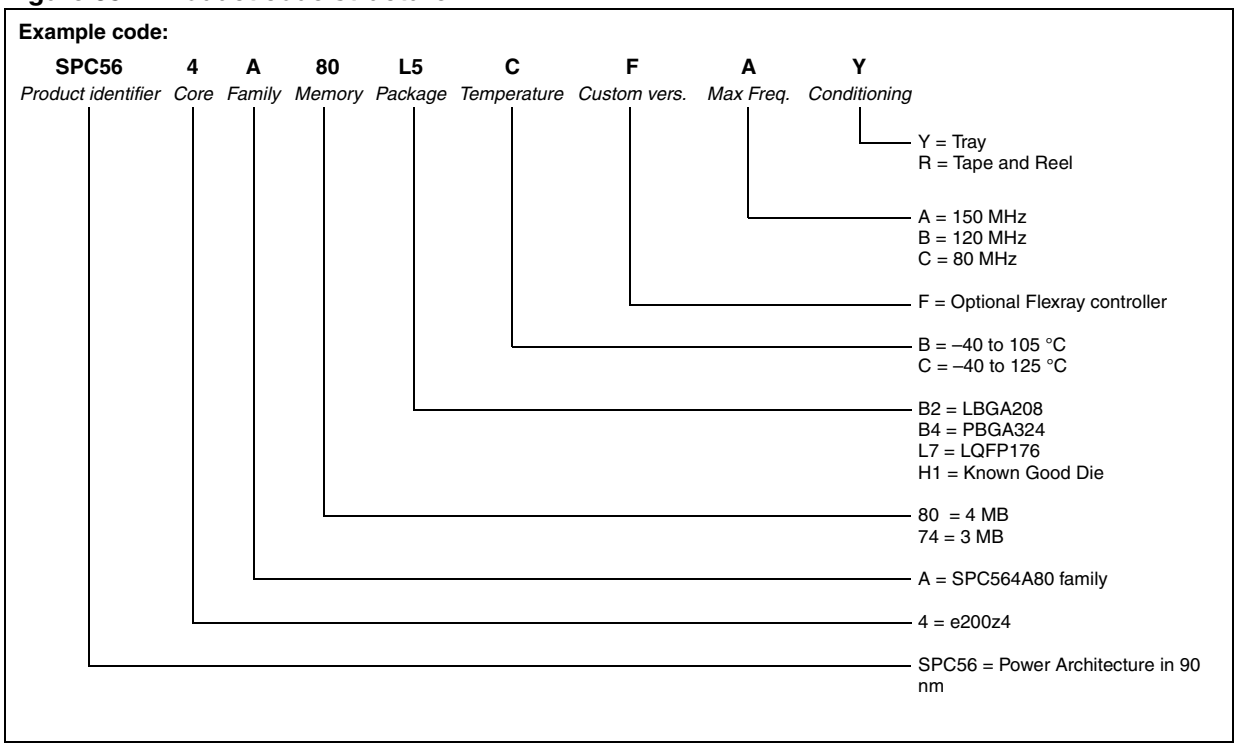

Table 56. Revision history (continued)

Date	Revision	Changes
01-Oct-2010 (cont)	4 (cont)	Updates to EBI timings: – Note added to t_{AAI}: When CAL_TS is used as CAL_ALE the hold time is 1 ns instead of 1.5 ns. – Correction: maximum calibration bus interface operating frequency is 66 MHz for all port configurations. – VDDE range in footnote 1 corrected to read, “External Bus and Calibration bus timing specified at f_{SYS} = 150 MHz and 100 MHz, VDD = 1.14 V to 1.32 V, VDDE = 3 V to 3.6 V (unless stated otherwise)” (VDDE range was 1.62 V to 3.6 V) Correction to IEEE 1149.1 timings: – SRC value in footnote 1 corrected to read, “JTAG timing specified at VDD = 1.14 V to 1.32 V, VDDEH = 4.5 V to 5.5 V with multi-voltage pads programmed to Low-Swing mode, TA = TL to TH, and CL = 30 pF with DSC = 0b10, SRC = 0b11.” (SRC value was 0b00) Correction to External interrupt timing (IRQ pin) timings: – Timings are specified at V_{DD} = 1.14 V to 1.32 V (was 1.08 V to 1.32 V). Update to DSPI timings: – Some of the timing parameters can vary depending on the value of V_{DDE}. For these parameters, ranges are now defined for two ranges of V_{DDE}. Change in signal name notation for DSPI, CAN and SCI signals: – DSPI: PCS_x[n] is now DSPI_x_PCS[n] SOUT_x is now DSPI_x_SOUT SIN_x is now DSPI_x_SIN SCK_x is now DSPI_x_SCK – CAN: CNTXx is now CAN_x_TX CNRXx is now CAN_x_RX – SCI: RXDx is now SCI_x_RX TXDx is now SCI_x_TX Updates to DC electrical specifications: – Slew rate on power supply pins specification changed to 25 V/ms (was 50 V/ms) V_{OH_LS} min spec changed to 2.0 V at 0.5 mA (was 2.7 V at 0.5 mA) Updated I/O pad current specifications Updated I/O pad V_{RC33} current specifications Corrections to Nexus timing: – Maximum Nexus debug port operating frequency is 40 MHz in all configurations – To route Nexus to MDO, clear NPC_PCR[NEXCFG] (formerly this was documented as NPC_PCR[CAL] – To route Nexus to CAL_MDO, set NPC_PCR[NEXCFG]=1 (formerly this was documented as NPC_PCR[CAL]
10-Feb-2011	5	– Minor editorial updates. – Re-organized the first few subsections of the “Overview” section. – Added ECSM to the block diagram. – Added information on the REACM, SIU, and ECS modules to the “Block summary” section.