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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7cfcr

  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.14 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the SPC564A80 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A80 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHZ for SOUT and SCK pins for DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI Module can generate and check parity in a serial frame

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.5.19 Software watchdog timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

1.5.20 Cyclic redundancy check (CRC) module

The CRC computing unit is dedicated to the computation of CRC off-loading the CPU. The CRC features:

- Support for CRC-16-CCITT (x25 protocol):
  - $X^{16} + X^{12} + X^5 + 1$
- Support for CRC-32 (Ethernet protocol):
  - $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$
- Zero wait states for each write/read operations to the CRC_CFG and CRC_INP registers at the maximum frequency

1.5.21 Error correction status module (ECSM)

The ECSM provides a myriad of miscellaneous control functions regarding program-visible information about the platform configuration and revision levels, a reset status register, a software watchdog timer, wakeup control for exiting sleep modes, and information on platform memory errors reported by error-correcting codes and/or generic access error information for certain processor cores.

is a variety of ways this module can be used, including as a component of an external real-time data acquisition system

1.6 SPC564A80 series architecture

1.6.1 Block diagram

Figure 1 shows a top-level block diagram of the SPC564A80 series.

Table 3. SPC564A80 series block summary (continued)

Block	Function
Reaction Module (REACM)	Works in conjunction with the eQADC and eTPU2 to increase system performance by removing the CPU from the current control loop.
System Integration Unit (SIU)	Controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation.
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables.
System timers	Includes periodic interrupt timer with real-time interrupt; output compare timer and system watchdog timer.
Temperature sensor	Provides the temperature of the device as an analog value.

M	BDIP	TCRCLKA	CS1	CS0					VDDE2	VDDE2	VSS
N	CS3	CS2	WE1	WE0					VSS	VSS	VDDE2
P	ADDR16	ADDR17	RD_WR	VRC33					VSS	VSS	VDDE2
R	ADDR18	ADDR19	VDDE-EH	TA							
T	ADDR20	ADDR21	ADDR12	TS							
U	ADDR22	ADDR23	ADDR13	ADDR14							
V	ADDR24	ADDR25	ADDR15	ADDR31							
W	ADDR26	VDDE-EH	ADDR30	VSS	VDD	VDDE2	VRC33	VDDE2	DATA11	DATA12	DATA14
Y	ADDR28	ADDR27	VSS	VDD	VDDE2	DATA8	DATA9	DATA10	GPIO207	DATA13	DATA15
AA	ADDR29	VSS	VDD	VDDE2	DATA1	VDDE2	GPIO206	DATA5	DATA7	VDDE2	EMIOS3
AB	VSS	VDD	VDDE2	DATA0	DATA2	DATA3	DATA4	DATA6	OE	EMIOS0	EMIOS1
	1	2	3	4	5	6	7	8	9	10	11

Figure 5. 324-pin PBGA package ballmap (southwest, viewed from above)

12	13	14	15	16	17	18	19	20	21	22	
AN27	AN28	AN35	VSSA1	AN12_ SDS	MDO11_ ETPUA29_O	MDO10_ ETPUA27_O	MDO8_ ETPUA21_O	VDD	VRC33	VSS	A
AN26	AN31	AN32	VSSA1	AN13_ SDO	MDO9_ ETPUA25_O	MDO7_ ETPUA19_O	MDO4_ ETPUA2_O	MDO0	VSS	NIC(1),(2)	B
AN25	AN30	AN33	VDDA1	AN14_ SDI	MDO5_ ETPUA4_O	MDO2	MDO1	VSS	NIC(1),(2)	VDD	C
AN24	AN29	AN34	VDDEH7	AN15_ FCK	MDO6_ ETPUA13_O	MDO3	VSS	NIC(1),(2)	TCK	TDI	D
							NIC(1),(2)	TMS	TDO	NIC(1)	E
							NIC(1),(2)	JCOMP	EVTI	EVTO	F
							RDY	MCKO	MSEO0	MSEO1	G
							VDDEH6AB	GPIO203	GPIO204	DSPI_B_ SIN	H
VSS	VSS	NIC(1),(2)					DSPI_B_ SOUT	DSPI_B_ PCS3	DSPI_B_ PCS0	DSPI_B_ PCS1	J
VSS	VSS	VSS					GPIO99	DSPI_B_ PCS4	DSPI_B_ SCK	DSPI_B_ PCS2	K
VSS	VSS	VSS					DSPI_B_ PCS5	DSPI_A_ SOUT	DSPI_A_ SIN	DSPI_A_ SCK	L

1. Pins marked “NIC” have no internal connection.
2. Balls B22, C21, D20, E19, F19 and J14 are shorted together inside the package.

Figure 6. 324-pin PBGA package ballmap (northeast, viewed from above)

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
ADDR30 ADDR6[8] DATA30 GPIO[26]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	26	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	W3
ADDR31 ADDR7[8] DATA31 GPIO[27]	External address bus External address bus External data bus GPIO	P A1 A2 G	001 010 100 000	27	I/O O I/O I/O	VDDE-EH Medium	— / Up	— / Up	—	—	V4
DATA0 ADDR16 GPIO[28]	External data bus External address bus GPIO	P A1 G	001 010 000	28	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB4
DATA1 ADDR17 GPIO[29]	External data bus External address bus GPIO	P A1 G	001 010 000	29	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA5
DATA2 ADDR18 GPIO[30]	External data bus External address bus GPIO	P A1 G	001 010 000	30	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB5
DATA3 ADDR19 GPIO[31]	External data bus External address bus GPIO	P A1 G	001 010 000	31	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB6
DATA4 ADDR20 GPIO[32]	External data bus External address bus GPIO	P A1 G	001 010 000	32	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB7
DATA5 ADDR21 GPIO[33]	External data bus External address bus GPIO	P A1 G	001 010 000	33	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AA8
DATA6 ADDR22 GPIO[34]	External data bus External address bus GPIO	P A1 G	001 010 000	34	I/O I/O I/O	VDDE5 Fast	— / Up	— / Up	—	—	AB8

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
TCK	JTAG test clock input	P	01	—	I	VDDEH7 MultiV[12]	TCK / Down	TCK / Down	128	C16	D21
TDI	JTAG test data input	P	01	232	I	VDDEH7 MultiV[12]	TDI / Up	TDI / Up	130	E14	D22
TDO	JTAG test data output	P	01	228	O	VDDEH7 MultiV[12]	TDO / Up	TDO / Up	123	F14	E21
TMS	JTAG test mode select input	P	01	—	I	VDDEH7 MultiV[12]	TMS / Up	TMS / Up	131	D14	E20
JCOMP	JTAG TAP controller enable	P	01	—	I	VDDEH7 MultiV[12]	JCOMP / Down	JCOMP / Down	121	F16	F20
FlexCAN											
CAN_A_TX SCI_A_TX GPIO[83]	FlexCAN A TX eSCI A TX GPIO	P A1 G	01 10 00	83	O O I/O	VDDEH6 Slow	— / Up	— / Up	81	P12	Y17
CAN_A_RX SCI_A_RX GPIO[84]	FlexCAN A RX eSCI A RX GPIO	P A1 G	01 10 00	84	I I I/O	VDDEH6 Slow	— / Up	— / Up	82	R12	AA18
CAN_B_TX DSPI_C_PCS[3] SCI_C_TX GPIO[85]	FlexCAN B TX DSPI C peripheral chip select eSCI C TX GPIO	P A1 A2 G	001 010 100 000	85	O O O I/O	VDDEH6 Slow	— / Up	— / Up	88	T12	AB18
CAN_B_RX DSPI_C_PCS[4] SCI_C_RX GPIO[86]	FlexCAN B RX DSPI C peripheral chip select eSCI C RX GPIO	P A1 A2 G	001 010 100 000	86	I O I I/O	VDDEH6 Slow	— / Up	— / Up	89	R13	AB19
CAN_C_TX DSPI_D_PCS[3] GPIO[87]	FlexCAN C TX DSPI D peripheral chip select GPIO	P A1 G	01 10 00	87	O O I/O	VDDEH6 Medium	— / Up	— / Up	101	K13	P19

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
AN3[18] DAN1-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[3] / —	169	C7	C9
AN4[18] DAN2+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[4] / —	168	B6	B9
AN5[18] DAN2-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[5] / —	167	A7	A9
AN6[18] DAN3+	Single Ended Analog Input Positive Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[6] / —	166	D7	D11
AN7[18] DAN3-	Single Ended Analog Input Negative Terminal Diff. Input	P	—	—	I I	VDDA Analog	I / —	AN[7] / —	165	C8	C10
AN8 ANW	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[8] / —	9	B3	D6
AN9 ANX	Single-ended Analog Input External Multiplexed Analog Input	P	01	—	I I	VDDA Analog	I / —	AN[9] / —	5	A2	D7
AN10 ANY	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[10] / —	—	—	D8
AN11 ANZ	Single-ended Analog Input Multiplexed Analog Input	P	01	—	I	VDDA Analog	I / —	AN[11] / —	4	A3	A5
AN12 - SDS MA0 ETPUA19_O[8] $\overline{SDS}$	Single-ended Analog Input MUX Address 0 eTPU A channel (output only) eQADC Serial Data Select	P A1 A2 G	001 010 100 000	215	I O O I/O	VDDEH7[19] Medium	I / —	AN[12] / —	148	A12	A16
AN13 - SDO MA1 ETPUA21_O[8] SDO	Single-ended Analog Input MUX Address 1 eTPU A channel (output only) eQADC Serial Data Out	P A1 A2 G	001 010 100 000	216	I O O O	VDDEH7[19] Medium	I / —	AN[13] / —	147	B12	B16

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
EMIOS13 DSPI_D_SOUT GPIO[192]	eMIOS channel DSPI D data output GPIO	P A1 G	01 10 00	192	I/O O I/O	VDDEH4 Medium	— / WKPCFG	— / WKPCFG	77	T8	AA14
EMIOS14 $\overline{\text{IRQ}}$[0] ETPUA29_O[8] GPIO[193]	eMIOS channel External interrupt request eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	193	I/O I O I/O	VDDEH4 Slow	— / Down	— / Down	78	R9	AB15
EMIOS15 $\overline{\text{IRQ}}$[1] GPIO[194]	eMIOS channel External interrupt request GPIO	P A1 G	01 10 00	194	I/O I I/O	VDDEH4 Slow	— / Down	— / Down	79	T9	Y14
EMIOS16 GPIO[195]	eMIOS channel GPIO	P G	01 00	195	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AA15
EMIOS17 GPIO[196]	eMIOS channel GPIO	P G	01 00	196	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	Y15
EMIOS18 GPIO[197]	eMIOS channel GPIO	P G	01 00	197	I/O I/O	VDDEH4 Slow	— / Up	— / Up	—	—	AB16
EMIOS19 GPIO[198]	eMIOS channel GPIO	P G	01 00	198	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AA16
EMIOS20 GPIO[199]	eMIOS channel GPIO	P G	01 00	199	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	AB17
EMIOS21 GPIO[200]	eMIOS channel GPIO	P G	01 00	200	I/O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	—	—	W16
EMIOS22 GPIO[201]	eMIOS channel GPIO	P G	01 00	201	I/O I/O	VDDEH4 Slow	— / Down	— / Down	—	—	Y16
EMIOS23 GPIO[202]	eMIOS channel GPIO	P G	01 00	202	I/O I/O	VDDEH4 Slow	— / Down	— / Down	80	R11	AA17
Clock Synthesizer											

Table 7. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDE2	1.8 V - 3.3 V	CS0, CS1, CS2, CS3,RD_WR, BDIP, WE0, WE1, OE, TS, TA
VDDE3	1.8 V - 3.3 V	ADDR12, ADDR13, ADDR14, ADDR15
VDDE5	1.8 V - 3.3 V	DATA0, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7, DATA8, DATA9, DATA10, DATA11, DATA12, DATA13, DATA14, DATA15, CLKOUT, ENGCLK
VDDE12	1.8 V - 3.3 V	CAL_CS0, CAL_CS2, CAL_CS3 CAL_ADDR12, CAL_ADDR13, CAL_ADDR14, CAL_ADDR15, CAL_ADDR16, CAL_ADDR17, CAL_ADDR18, CAL_ADDR19, CAL_ADDR20, CAL_ADDR21, CAL_ADDR22, CAL_ADDR23, CAL_ADDR24, CAL_ADDR25, CAL_ADDR26, CAL_ADDR27, CAL_ADDR28, CAL_ADDR29, CAL_ADDR30, CAL_DATA0, CAL_DATA1, CAL_DATA2, CAL_DATA3, CAL_DATA4, CAL_DATA5, CAL_DATA6, CAL_DATA7, CAL_DATA8, CAL_DATA9, CAL_DATA10, CAL_DATA11, CAL_DATA12, CAL_DATA13, CAL_DATA14, CAL_DATA15, CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V - 5 V	ADDR16, ADDR17, ADDR18, ADDR19, ADDR20, ADDR21, ADDR22, ADDR23, ADDR24, ADDR25, ADDR26, ADDR27, ADDR28, ADDR29, ADDR30, ADDR31
VDDEH1	3.3 V - 5.0 V	ETPUA10, ETPUA11, ETPUA12, ETPUA13, ETPUA14, ETPUA15, ETPUA16, ETPUA17, ETPUA18, ETPUA19, ETPUA20, ETPUA21, ETPUA22, ETPUA23, ETPUA24, ETPUA25, ETPUA26, ETPUA27, ETPUA28, ETPUA29, ETPUA30, ETPUA31
VDDEH4	3.3 V - 5.0 V	EMIOS0, EMIOS1, EMIOS2, EMIOS3, EMIOS4, EMIOS5, EMIOS6, EMIOS7, EMIOS8, EMIOS9, EMIOS10, EMIOS11, EMIOS12, EMIOS13, EMIOS14, EMIOS15, EMIOS16, EMIOS17, EMIOS18, EMIOS19, EMIOS20, EMIOS21, EMIOS22, EMIOS23, TCRCLKA, ETPUA0, ETPUA1, ETPUA2, ETPUA3, ETPUA4, ETPUA5, ETPUA6, ETPUA7, ETPUA8, ETPUA9, ETPUA0
VDDEH6	3.3 V - 5.0 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0], DSPI_B_PCS[1], DSPI_B_PCS[2], DSPI_B_PCS[3], DSPI_B_PCS[4], DSPI_B_PCS[5], SCI_B_RX, SCI_C_TX, EXTAL, XTAL
VDDEH7	3.3 V - 5.0 V	EMIOS14, EMIOS 15, GPIO98, GPIO99, GPIO203, GPIO204, GPIO206, GPIO207, GPIO219, EVTI, EVTO, MDO4, MDO5, MDO6, MDO7, MDO8, MDO9, MDO10, MDO11, MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0], DSPI_A_PCS[1], DSPI_A_PCS[4], DSPI_A_PCS[5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5 V	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7, AN8, AN9, AN10, AN11, AN16, AN17, AN18, AN19, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AN39, VRH, VRL, REFBYBC
VRC33[(1)]	3.3 V	MCKO, MDO0, MDO1, MDO2, MDO3

Table 12. Thermal characteristics for 324-pin PBGA(1)

Symbol		C	Parameter	Conditions	Value	Unit
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Single layer board - 1s	31	°C/W
$R_{\theta JA}$	CC	D	Junction-to-Ambient, Natural Convection(2)	Four layer board - 2s2p	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., single layer board	23	°C/W
$R_{\theta JMA}$	CC	D	Junction-to-Moving-Air, Ambient(2)	at 200 ft./min., four layer board 2s2p	17	°C/W
$R_{\theta JB}$	CC	D	Junction-to-Board(3)		11	°C/W
$R_{\theta JCtop}$	CC	D	Junction-to-Case(4)		7	°C/W
Ψ_{JT}	CC	D	Junction-to-Package Top, Natural Convection(5)		2	°C/W

1. Thermal characteristics are targets based on simulation that are subject to change per device characterization.
2. Junction-to-Ambient Thermal Resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package.
3. Junction-to-Board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-Case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer.
5. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

3.3.1 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

Equation 1 $T_J = T_A + (R_{\theta JA} * P_D)$

where:

T_A = ambient temperature for the package (^oC)

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

P_D = power dissipation in the package (W)

The thermal resistance values used are based on the JEDEC JESD51 series of standards to provide consistent values for estimations and comparisons. The difference between the values determined for the single-layer (1s) board compared to a four-layer board that has two signal layers, a power and a ground plane (2s2p), demonstrate that the effective thermal resistance is not a constant. The thermal resistance depends on the:

- Construction of the application board (number of planes)
- Effective size of the board which cools the component
- Quality of the thermal and electrical connections to the planes
- Power dissipated by adjacent components

Connect all the ground and power balls to the respective planes with one via per ball. Using fewer vias to connect the package to the planes reduces the thermal performance. Thinner planes also reduce the thermal performance. When the clearance between the vias leave the planes virtually disconnected, the thermal performance is also greatly reduced.

As a general rule, the value obtained on a single-layer board is within the normal range for the tightly packed printed circuit board. The value obtained on a board with the internal planes is usually within the normal range if the application board has:

- One oz. (35 micron nominal thickness) internal planes
- Components are well separated
- Overall power dissipation on the board is less than 0.02 W/cm^2

The thermal performance of any component depends on the power dissipation of the surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

Equation 2 $T_J = T_B + (R_{\theta JB} * P_D)$

where:

T_B = board temperature for the package perimeter (^oC)

$R_{\theta JB}$ = junction-to-board thermal resistance ($^oC/W$) per JESD51-8S

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air does not factor into the calculation, an acceptable value for the junction temperature is predictable. Ensure the application board is similar to the thermal test condition, with the component soldered to a board with internal planes.

The thermal resistance is expressed as the sum of a junction-to-case thermal resistance plus a case-to-ambient thermal resistance:

Equation 3 $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

where:

$R_{\theta JA}$ = junction-to-ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ = junction-to-case thermal resistance ($^oC/W$)

$R_{\theta CA}$ = case to ambient thermal resistance ($^oC/W$)

$R_{\theta JC}$ is device related and is not affected by other factors. The thermal environment can be controlled to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, change the air flow around the device, add a heat sink, change the mounting arrangement on the printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device. This description is most useful for packages with heat sinks where 90% of the heat flow is through the case to heat sink to ambient. For most packages, a better model is required.

A more accurate two-resistor thermal model can be constructed from the junction-to-board thermal resistance and the junction-to-case thermal resistance. The junction-to-case thermal resistance describes when using a heat sink or where a substantial amount of heat is dissipated from the top of the package. The junction-to-board thermal resistance describes the thermal performance when most of the heat is conducted to the printed circuit

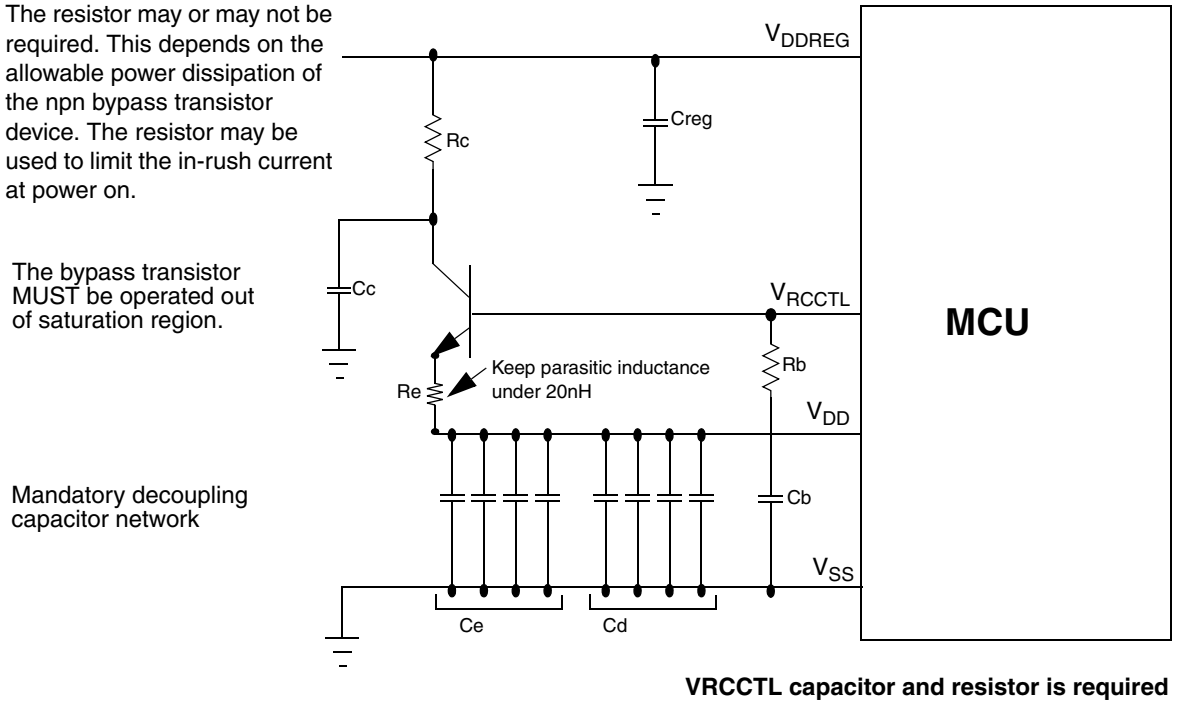

Figure 8. Core voltage regulator controller external components preferred configuration

Table 17. SPC564A80 External network specification

External Network Parameter	Min	Typ	Max	Comment
T1				NJD2873 or BCP68 only
Cb	1.1 µF	2.2µF	2.97µF	X7R,-50%/+35%
Ce	3*2.35µF+5µF	3*4.7µF+10µF	3*6.35µF+13.5µF	X7R, -50%/+35%
Equivalent ESR of Ce capacitors	5mΩ		50mΩ	
Cd	4*50nF	4*100nF	4*135nF	X7R, -50%/+35%
Rb	9Ω	10Ω	11Ω	+/-10%
Re	0.252Ω	0.280Ω	0.308Ω	+/-10%
Creg		10µF		It depends on external Vreg.
Cc	5µF	10µF	13.5µF	X7R, -50%/+35%
Rc	1.1Ω		5.6Ω	May or may not be required. It depends on the allowable power dissipation of T1.

Table 30. eQADC differential ended conversion specifications (operating) (continued)

Symbol		C	Parameter		Value		Unit
					min	max	
GAINVGA2 (1)	CC	–	Variable gain amplifier accuracy (gain=2)(2)				
	CC	D	INL	8 MHz ADC	–5	5	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–3	3	Counts
	CC	D		16 MHz ADC	–3	3	Counts
GAINVGA4 (1)	CC	–	Variable gain amplifier accuracy (gain=4)(2)				
	CC	D	INL	8 MHz ADC	–7	7	Counts
	CC	D		16 MHz ADC	–8	8	Counts
	CC	D	DNL	8 MHz ADC	–4	4	Counts
	CC	D		16 MHz ADC	–4	4	Counts
$DIFF_{max}$	CC	C	Maximum differential voltage (DANx+ - DANx-) or (DANx- - DANx+)(5)	PREGAIN set to 1X setting	—	(VRH - VRL)/2	V
$DIFF_{max2}$	CC	C		PREGAIN set to 2X setting	—	(VRH - VRL)/4	V
$DIFF_{max4}$	CC	C		PREGAIN set to 4X setting	—	(VRH - VRL)/8	V
$DIFF_{cmv}$	CC	C	Differential input Common mode voltage (DANx- + DANx+)/2(5)	—	$(V_{RH} + V_{RL})/2$ - 5%	$(V_{RH} + V_{RL})/2$ + 5%	V

1. Applies only to differential channels.
2. Variable gain is controlled by setting the PRE_GAIN bits in the ADC_ACR1-8 registers to select a gain factor of ×1, ×2, or ×4. Settings are for differential input only. Tested at ×1 gain. Values for other settings are guaranteed by as indicated.
3. At $V_{RH} - V_{RL}$ = 5.12 V, one LSB = 1.25 mV.
4. Guaranteed 10-bit mono tonicity.
5. Voltages between VRL and VRH will not cause damage to the pins. However, they may not be converted accurately if the differential voltage is above the maximum differential voltage. In addition, conversion errors may occur if the common mode voltage of the differential signal violates the Differential Input common mode voltage specification.

3.17.5 External interrupt timing (IRQ pin)

Table 44. External interrupt timing(1)

#	Characteristic	Symbol	Min	Max	Unit
1	IRQ Pulse Width Low	t_{IPWL}	3	—	t_{cyc}
2	IRQ Pulse Width High	t_{IPWH}	3	—	t_{cyc}
3	IRQ Edge to Edge Time(2)	t_{ICYC}	6	—	t_{cyc}

1. IRQ timing specified at V_{DD} = 1.14 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H.
2. Applies when IRQ pins are configured for rising edge or falling edge events, but not both.

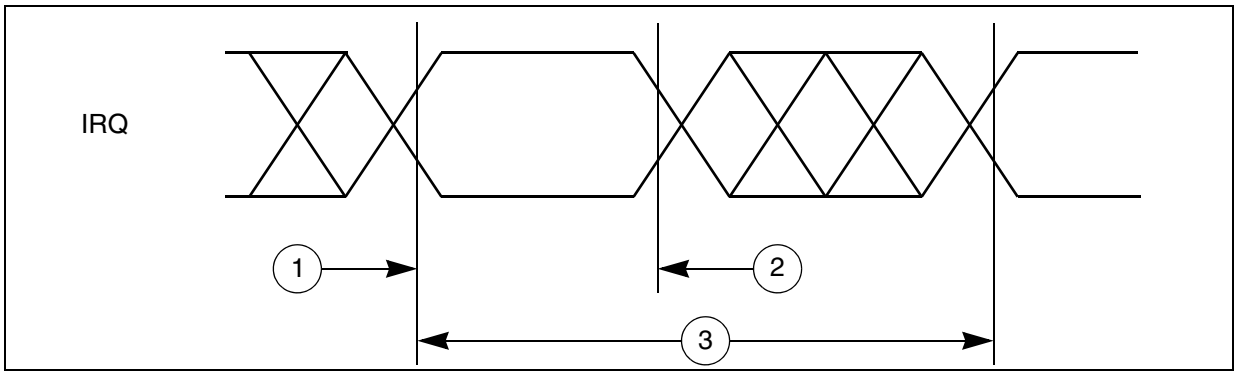

Figure 22. External Interrupt Timing

3.17.6 eTPU timing

Table 45. eTPU timing(1)

#	Characteristic	Symbol	Min	Max	Unit
1	eTPU Input Channel Pulse Width	t_{ICPW}	4	—	t_{cyc}
2	eTPU Output Channel Pulse Width	t_{OCPW}	2(2)	—	t_{cyc}

1. eTPU timing specified at V_{DD} = 1.08 V to 1.32 V, V_{DDEH} = 3.0 V to 5.5 V, V_{DD33} and V_{DDSYN} = 3.0 V to 3.6 V, $T_A = T_L$ to T_H, and C_L = 200 pF with SRC = 0b00.
2. This specification does not include the rise and fall times. When calculating the minimum eTPU pulse width, include the rise and fall times defined in the slew rate control fields (SRC) of the pad configuration registers (PCR).

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

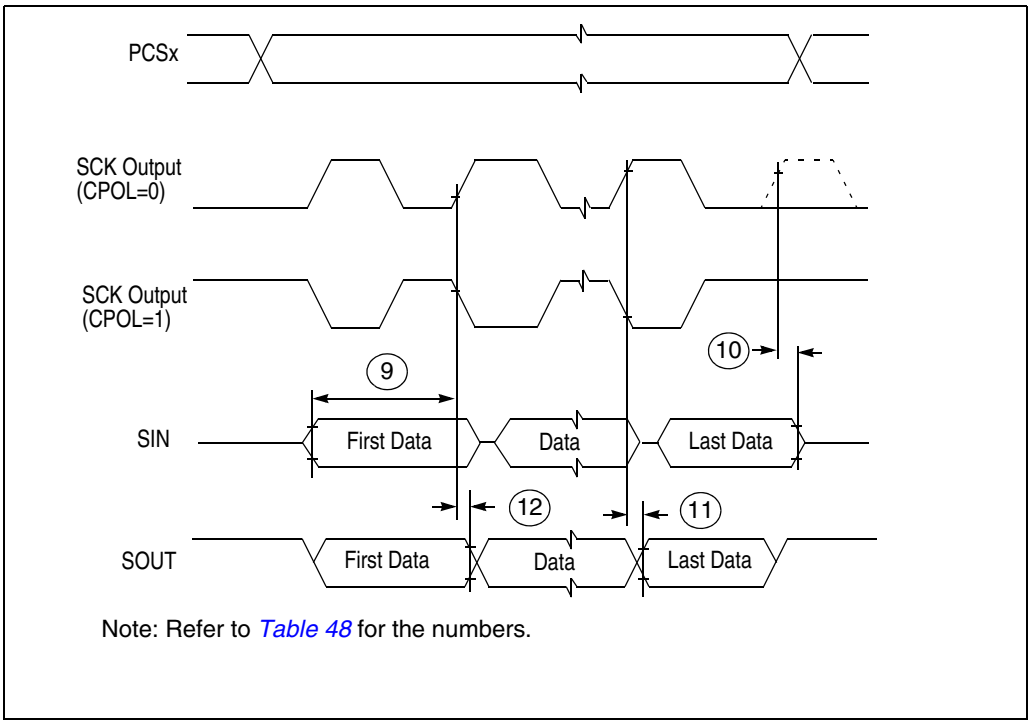

Figure 28. DSPI modified transfer format timing — master, CPHA = 1

4.2 Package mechanical data

4.2.1 LQFP176

Table 53. LBGA208 mechanical data (continued)

Symbol	mm			inches[1]		
	Min	Typ	Max	Min	Typ	Max
D	16.80	17.00	17.20	0.6614	0.6693	0.6772
D1		15.00			0.5906	
E	16.80	17.00	17.20	0.6614	0.6693	0.6772
E1		15.00			0.5906	
e		1.00			0.0394	
F		1.00			0.0394	
ddd			0.20			0.0079
eee[4]			0.25			0.0098
fff[5]			0.10			0.0039

1. Values in inches are converted from mm and rounded to 4 decimal digits.
2. LBGA stands for **L**ow profile **B**all **G**rid **A**rray.
   —Low profile: The total profile height (Dim A) is measured from the seating plane to the top of the component
   —The maximum total package height is calculated by the following methodology:
   A2 Typ+A1 Typ +√ ($A1^2$+$A3^2$+$A4^2$ tolerance values)
   — Low profile: 1.20mm < A ≤ 1.70mm
3. The typical ball diameter before mounting is 0.60mm.
4. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.
5. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above. The axis of each ball must lie simultaneously in both tolerance zones.

4.2.3 PBGA324