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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7cobr

List of figures

1.5 Feature details

1.5.1 e200z4 core

SPC564A80 devices have a high performance e200z448n3 core processor:

- Dual issue, 32-bit Power Architecture embedded category CPU
- Variable Length Encoding Enhancements
- 8 KB instruction cache: 2- or 4- way set associative instruction cache
- Thirty-two 64-bit general purpose registers (GPRs)
- Memory management unit (MMU) with 24-entry fully-associative translation look-aside buffer (TLB)
- Harvard Architecture: Separate instruction bus and load/store bus
- Vectored interrupt support
- Non-maskable interrupt input
- Critical Interrupt input
- New ‘Wait for Interrupt’ instruction, to be used with new low power modes
- Reservation instructions for implementing read-modify-write accesses
- Signal processing extension (SPE) APU
- Single Precision Floating point (scalar and vector)
- Nexus Class 3+ debug
- Process ID manipulation for the MMU using an external tool

1.5.2 Crossbar Switch (XBAR)

The XBAR multiport crossbar switch supports simultaneous connections between five master ports and four slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width.

The crossbar allows three concurrent transactions to occur from the master ports to any slave port but each master must access a different slave. If a slave port is simultaneously requested by more than one master port, arbitration logic selects the higher priority master and grants it ownership of the slave port. All other masters requesting that slave port are stalled until the higher priority master completes its transactions. Requesting masters are treated with equal priority and are granted access to a slave port in round-robin fashion, based upon the ID of the last master to be granted access. The crossbar provides the following features:

- 5 master ports
  - CPU instruction bus
  - CPU data bus
  - eDMA
  - FlexRay
  - External Bus Interface

providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource cannot preempt each other.

The INTC provides the following features:

- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can assigned a specific priority by software
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

1.5.5 Memory protection unit (MPU)

The Memory Protection Unit (MPU) provides hardware access control for all memory references generated in a device. Using preprogrammed region descriptors, which define memory spaces and their associated access rights, the MPU concurrently monitors all system bus transactions and evaluates the appropriateness of each transfer. Memory references with sufficient access control rights are allowed to complete; references that are not mapped to any region descriptor or have insufficient rights are terminated with a protection error response.

The MPU has these major features:

- Support for 16 memory region descriptors, each 128 bits in size
  - Specification of start and end addresses provide granularity for region sizes from 32 bytes to 4 GB
  - MPU is invalid at reset, thus no access restrictions are enforced
  - Two types of access control definitions: processor core bus master supports the traditional {read, write, execute} permissions with independent definitions for supervisor and user mode accesses; the remaining non-core bus masters (eDMA, FlexRay, and EBI[1]) support {read, write} attributes
  - Automatic hardware maintenance of the region descriptor valid bit removes issues associated with maintaining a coherent image of the descriptor
  - Alternate memory view of the access control word for each descriptor provides an efficient mechanism to dynamically alter the access rights of a descriptor only[(a)]
  - For overlapping region descriptors, priority is given to permission granting over access denying as this approach provides more flexibility to system software
- Support for two XBAR slave port connections (SRAM and PBRIDGE)
  - For each connected XBAR slave port (SRAM and PBRIDGE), MPU hardware monitors every port access using the pre-programmed memory region descriptors

  - Saturated or non-saturated modes
  - Programmable Rounding (Convergent; Two's Complement; Truncated)
  - Prefill mode to precondition the filter before the sample window opens
  - Supports Multiple Cascading Decimation Filters to implement more complex filter designs
  - Optional Absolute Integrators on the output of Decimation Filters
- Full duplex synchronous serial interface to an external device
  - Free-running clock for use by an external device
  - Supports a 26-bit message length
- Priority based queues
  - Supports six queues with fixed priority. When commands of distinct queues are bound for the same ADC, the higher priority queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Supports software and hardware trigger modes to arm a particular queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter

1.5.14 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the SPC564A80 MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that implements the Microsecond Bus protocol. There are three identical DSPI blocks on the SPC564A80 MCU. The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.

DSPI module features include:

- Selectable LVDS pads working at 40 MHZ for SOUT and SCK pins for DSPI_B and DSPI_C
- 3 sources of serialized data: eTPU_A, eMIOS output channels and memory-mapped register in the DSPI
- 4 destinations for deserialized data: eTPU_A and eMIOS input channels, SIU external Interrupt input request, memory-mapped register in the DSPI
- 32-bit DSI and TSB modes require 32 PCR registers, 32 GPO and GPI registers in the SIU to select either GPIO, eTPU or eMIOS bits for serialization
- The DSPI Module can generate and check parity in a serial frame

1.5.15 eSCI

Three enhanced serial communications interface (eSCI) modules provide asynchronous serial communications with peripheral devices and other MCUs, and include support to interface to Local Interconnect Network (LIN) slave devices. Each eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit, data format
- Programmable 12-bit or 13-bit data format for Timed Serial Bus (TSB) configuration to support the Microsecond bus standard
- Automatic parity generation
- LIN support
  - Autonomous transmission of entire frames
  - Configurable to support all revisions of the LIN standard
  - Automatic parity bit generation
  - Double stop bit after bit error
  - 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- 2 receiver wake-up methods:
  - Idle line wake-up
  - Address mark wake-up
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  - Global error bit stored with receive data in system RAM to allow post processing of errors

1.5.16 FlexCAN

The SPC564A80 MCU includes three controller area network (FlexCAN) blocks. The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and required bandwidth. Each FlexCAN module contains 64 message buffers.

Table 7. Power/ground segmentation

Power Segment	Voltage	I/O Pins Powered by Segment
VDDE2	1.8 V - 3.3 V	CS0, CS1, CS2, CS3,RD_WR, BDIP, WE0, WE1, OE, TS, TA
VDDE3	1.8 V - 3.3 V	ADDR12, ADDR13, ADDR14, ADDR15
VDDE5	1.8 V - 3.3 V	DATA0, DATA1, DATA2, DATA3, DATA4, DATA5, DATA6, DATA7, DATA8, DATA9, DATA10, DATA11, DATA12, DATA13, DATA14, DATA15, CLKOUT, ENGCLK
VDDE12	1.8 V - 3.3 V	CAL_CS0, CAL_CS2, CAL_CS3 CAL_ADDR12, CAL_ADDR13, CAL_ADDR14, CAL_ADDR15, CAL_ADDR16, CAL_ADDR17, CAL_ADDR18, CAL_ADDR19, CAL_ADDR20, CAL_ADDR21, CAL_ADDR22, CAL_ADDR23, CAL_ADDR24, CAL_ADDR25, CAL_ADDR26, CAL_ADDR27, CAL_ADDR28, CAL_ADDR29, CAL_ADDR30, CAL_DATA0, CAL_DATA1, CAL_DATA2, CAL_DATA3, CAL_DATA4, CAL_DATA5, CAL_DATA6, CAL_DATA7, CAL_DATA8, CAL_DATA9, CAL_DATA10, CAL_DATA11, CAL_DATA12, CAL_DATA13, CAL_DATA14, CAL_DATA15, CAL_RD_WR, CAL_WE0, CAL_WE1, CAL_OE, CAL_TS
VDDE-EH	3.0 V - 5 V	ADDR16, ADDR17, ADDR18, ADDR19, ADDR20, ADDR21, ADDR22, ADDR23, ADDR24, ADDR25, ADDR26, ADDR27, ADDR28, ADDR29, ADDR30, ADDR31
VDDEH1	3.3 V - 5.0 V	ETPUA10, ETPUA11, ETPUA12, ETPUA13, ETPUA14, ETPUA15, ETPUA16, ETPUA17, ETPUA18, ETPUA19, ETPUA20, ETPUA21, ETPUA22, ETPUA23, ETPUA24, ETPUA25, ETPUA26, ETPUA27, ETPUA28, ETPUA29, ETPUA30, ETPUA31
VDDEH4	3.3 V - 5.0 V	EMIOS0, EMIOS1, EMIOS2, EMIOS3, EMIOS4, EMIOS5, EMIOS6, EMIOS7, EMIOS8, EMIOS9, EMIOS10, EMIOS11, EMIOS12, EMIOS13, EMIOS14, EMIOS15, EMIOS16, EMIOS17, EMIOS18, EMIOS19, EMIOS20, EMIOS21, EMIOS22, EMIOS23, TCRCLKA, ETPUA0, ETPUA1, ETPUA2, ETPUA3, ETPUA4, ETPUA5, ETPUA6, ETPUA7, ETPUA8, ETPUA9, ETPUA0
VDDEH6	3.3 V - 5.0 V	$\overline{\text{RESET}}$, $\overline{\text{RSTOUT}}$, PLLREF, PLLCFG1, RSTCFG, BOOTCFG0, BOOTCFG1, WKPCFG, CAN_A_TX, CAN_A_RX, CAN_B_TX, CAN_B_RX, CAN_C_TX, CAN_C_RX, SCI_A_TX, SCI_A_RX, SCI_B_TX, SCI_C_RX, DSPI_B_SCK, DSPI_B_SIN, DSPI_B_SOUT, DSPI_B_PCS[0], DSPI_B_PCS[1], DSPI_B_PCS[2], DSPI_B_PCS[3], DSPI_B_PCS[4], DSPI_B_PCS[5], SCI_B_RX, SCI_C_TX, EXTAL, XTAL
VDDEH7	3.3 V - 5.0 V	EMIOS14, EMIOS 15, GPIO98, GPIO99, GPIO203, GPIO204, GPIO206, GPIO207, GPIO219, EVTI, EVTO, MDO4, MDO5, MDO6, MDO7, MDO8, MDO9, MDO10, MDO11, MSEO0, MSEO1, RDY, TCK, TDI, TDO, TMS, JCOMP, DSPI_A_SCK, DSPI_A_SIN, DSPI_A_SOUT, DSPI_A_PCS[0], DSPI_A_PCS[1], DSPI_A_PCS[4], DSPI_A_PCS[5], AN12-SDS, AN13-SDO, AN14-SDI, AN15-FCK
VDDA	5 V	AN0, AN1, AN2, AN3, AN4, AN5, AN6, AN7, AN8, AN9, AN10, AN11, AN16, AN17, AN18, AN19, AN20, AN21, AN22, AN23, AN24, AN25, AN26, AN27, AN28, AN29, AN30, AN31, AN32, AN33, AN34, AN35, AN36, AN37, AN38, AN39, VRH, VRL, REFBYBC
VRC33[(1)]	3.3 V	MCKO, MDO0, MDO1, MDO2, MDO3

Table 7. Power/ground segmentation (continued)

Power Segment	Voltage	I/O Pins Powered by Segment
Other Power Segments		
VDDREG	5 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.95–1.2 V (unregulated mode)	—
	2.0–5.5 V (regulated mode)	—
VSS	—	—

1. Do not use VRC33 to drive external circuits.

3.6.2 Recommended power transistors

The following NPN transistors are recommended for use with the on-chip voltage regulator controller: ON Semiconductor™ BCP68T1 or NJD2873 as well as Philips Semiconductor™ BCP68. The collector of the external transistor is preferably connected to the same voltage supply source as the output stage of the regulator.

Table 18. Recommended operating characteristics

Symbol	Parameter	Value	Unit
h_{FE} (β)	DC current gain (Beta)	60 – 550	—
P_D	Absolute minimum power dissipation	>1.0 (1.5 preferred)	W
I_{CMaxDC}	Minimum peak collector current	1.0	A
VCE_{SAT}	Collector-to-emitter saturation voltage	200 – 600(1)	mV
V_{BE}	Base-to-emitter voltage	0.4 – 1.0	V

1. Adjust resistor at bipolar transistor collector for 3.3 V/5.0 V to avoid VCE < VCE_{SAT}.

3.7 Power up/down sequencing

There is no power sequencing required among power sources during power up and power down, in order to operate within specification.

Although there are no power up/down sequencing requirements to prevent issues such as latch-up or excessive current spikes the state of the I/O pins during power up/down varies according to *Table 19* for all pins with fast pads, and *Table 20* for all pins with medium, slow, and multi-voltage pads.

Table 19. Power sequence pin states (fast pads)

V_{DDE}	V_{RC33}	V_{DD}	Pad State
LOW	X	X	LOW
V_{DDE}	LOW	X	HIGH
V_{DDE}	V_{RC33}	LOW	HIGH IMPEDANCE
V_{DDE}	V_{RC33}	V_{DD}	FUNCTIONAL

Table 20. Power sequence pin states (medium, slow, and multi-voltage pads)

V_{DDEH}	V_{DD}	Pad State
LOW	X	LOW
V_{DDEH}	LOW	HIGH IMPEDANCE
V_{DDEH}	V_{DD}	FUNCTIONAL

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
$I_{ACT\_MV\_PD}$	CC	C	Multivoltage pad weak pulldown current	V_{DDE}= 3.0–3.6 V[5], MultiV pad, high swing mode only	10	—	60	µA
		P		4.75 V – 5.25 V	25	—	200	
I_{INACT_D}	CC	P	I/O input leakage current[16]	—	–2.5	—	2.5	µA
I_{IC}	SR	T	DC injection current (per pin)	—	–1.0	—	1.0	mA
I_{INACT_A}	SR	P	Analog input current, channel off, AN[0:7][17]	—	–250	—	250	nA
		P	Analog input current, channel off, all other analog pins[17]	—	–150	—	150	
C_L	CC	D	Load capacitance (fast I/O)[18]	DSC(PCR[8:9]) = 0b00	—		10	pF
		D		DSC(PCR[8:9]) = 0b01	—		20	
		D		DSC(PCR[8:9]) = 0b10	—		30	
		D		DSC(PCR[8:9]) = 0b11	—		50	
C_{IN}	CC	D	Input capacitance (digital pins)	—	—		7	pF
C_{IN_A}	CC	D	Input capacitance (analog pins)	—	—		10	pF
C_{IN_M}	CC	D	Input capacitance (digital and analog pins[19])	—	—		12	pF
$R_{PUPD200K}$	SR	P	Weak Pull-Up/Down Resistance[20], 200 kΩ Option	—	130	—	280	kΩ
$R_{PUPD100K}$	SR	P	Weak Pull-Up/Down Resistance[20], 100 kΩ Option	—	65	—	140	kΩ

Table 24. V_{RC33} pad average DC current(1)

Pad Type	Symbol		C	Period (ns)	Load (2) (pF)	V_{RC33} (V)	V_{DDE} (V)	Drive Select	I_{DD33} Avg (µA)	I_{DD33} RMS (µA)
Fast	I_{DRV_FC}	CC	D	10	50	3.6	3.6	11	2.35	6.12
		CC	D	10	30	3.6	3.6	10	1.75	4.3
		CC	D	10	20	3.6	3.6	01	1.41	3.43
		CC	D	10	10	3.6	3.6	00	1.06	2.9
		CC	D	10	50	3.6	1.98	11	1.75	4.56
		CC	D	10	30	3.6	1.98	10	1.32	3.44
		CC	D	10	20	3.6	1.98	01	1.14	2.95
		CC	D	10	10	3.6	1.98	00	0.95	2.62

1. These are typical values that are estimated from simulation and not tested. Currents apply to output pins only.
2. All loads are lumped.

3.9.2 LVDS pad specifications

LVDS pads are implemented to support the MSC (Microsecond Channel) protocol which is an enhanced feature of the DSPI module. The LVDS pads are compliant with LVDS specifications and support data rates up to 50 MHz.

Table 25. DSPI LVDS pad specification

#	Characteristic	Symbol	C		Condition	Min. Value	Typ. Value	Max. Value	Unit
Data Rate									
4	Data Frequency	$f_{LVDSCLK}$	CC	D	—		50		MHz
Driver Specs									
5	Differential output voltage	V_{OD}	CC	P	SRC=0b00 or 0b11	150		400	mV
			CC	P	SRC=0b01	90		320	
			CC	P	SRC=0b10	160		480	
6	Common mode voltage (LVDS), VOS	V_{OD}	CC	P		1.06	1.2	1.39	V
7	Rise/Fall time	T_R/T_F	CC	D	—		2		ns
8	Propagation delay (Low to High)	T_{PLH}	CC	D			4		ns
9	Propagation delay (High to Low)	T_{PHL}	CC	D	—		4		ns

Table 25. DSPI LVDS pad specification (continued)

#	Characteristic	Symbol		C	Condition	Min. Value	Typ. Value	Max. Value	Unit
10	Delay (H/L), sync Mode	t_{PDSYNC}	CC	D			4		ns
11	Delay, Z to Normal (High/Low)	T_{DZ}	CC	D	—		500		ns
12	Diff Skew Itphla-tplhbl or Itplhb-tphlal	T_{SKEW}	CC	D	—			0.5	ns
Termination									
13	Trans. Line (differential Zo)		CC	D	—	95	100	105	Ω
14	Temperature		CC	D		–40		150	°C

3.10 Oscillator and PLLMRFM electrical characteristics

Table 26. PLLMRFM electrical specifications

(V_{DDPLL} = 1.08 V to 3.6 V, V_{SS} = V_{SSPLL} = 0 V, T_A = T_L to T_H)

Symbol		C	Parameter	Conditions	Value		Unit
					min	max	
$f_{ref\_crystal}$ f_{ref_ext}	CC	D	PLL reference frequency range[1]	Crystal reference	4	40	MHz
		C		External reference	4	80	
f_{pll_in}	CC	P	Phase detector input frequency range (after pre-divider)	—	4	16	MHz
f_{vco}	CC	P	VCO frequency range	—	256	512	MHz
f_{sys}	CC	C	On-chip PLL frequency[2]	—	16	150	MHz
f_{sys}	CC	T	System frequency in bypass mode[2]	Crystal reference	4	40	MHz
		P		External reference	0	80	
t_{CYC}	CC	D	System clock period	—	—	1 / f_{sys}	ns
f_{LORL} f_{LORH}	CC	D	Loss of reference frequency window[3]	Lower limit	1.6	3.7	MHz
		D		Upper limit	24	56	
f_{SCM}	CC	P	Self-clocked mode frequency [4],[5]	—	1.2	72.25	MHz

3.13 Configuring SRAM wait states

Use the SWSC field in the ECSM_MUDCR register to specify an additional wait state for the device SRAM. By default, no wait state is added.

Table 31. Cutoff frequency for additional SRAM wait state

(1)	SWSC Value
98	0
153	1

1. Max frequencies including 2% PLL FM.

Please see the device reference manual for details.

3.14 Platform flash controller electrical characteristics

Table 32. APC, RWSC, WWSC settings vs. frequency of operation(1),(2)

Max. Flash Operating Frequency (MHz)(3)	APC(4)	RWSC(4)	WWSC
20 MHz	0b000	0b000	0b11
61 MHz	0b001	0b001	0b11
90 MHz	0b010	0b010	0b11
123 MHz	0b011	0b011	0b11
153 MHz	0b100	0b100	0b11

1. APC, RWSC and WWSC are fields in the flash memory BIUCR register used to specify wait states for address pipelining and read/write accesses. Illegal combinations exist—all entries must be taken from the same row.
2. TBD: To Be Defined.
3. Max frequencies including 2% PLL FM.
4. APC must be equal to RWSC.

3.15 Flash memory electrical characteristics

Table 33. Flash program and erase specifications(1)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
1	$T_{dwprogram}$	CC	P	Double Word (64 bits) Program Time	—	45	—	500	µs
2	$T_{pprogram}$	CC	P	Page Program Time	—	55	160(4)	500	µs
3	$T_{16kpperase}$	CC	P	16 KB Block Pre-program and Erase Time	—	300	1000	5000	ms

Table 33. Flash program and erase specifications(1) (continued)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	3000	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5300	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.
4. Page size is 128 bits (4 words).
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

1. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

3.17 AC timing

3.17.1 Reset and configuration pin timing

Table 37. Reset and Configuration Pin Timing(1)

#	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width(2)	t_{RPW}	10	—	t_{cyc}
2	$\overline{\text{RESET}}$ Glitch Detect Pulse Width	t_{GPW}	2	—	t_{cyc}
3	PLLREF, BOOTCFG, WKPCFG Setup Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCSU}	10	—	t_{cyc}
4	PLLREF, BOOTCFG, WKPCFG Hold Time to $\overline{\text{RSTOUT}}$ Valid	t_{RCH}	0	—	t_{cyc}

1. Reset timing specified at: V_{DDEH} = 3.0 V to 5.25 V, V_{DD} = 1.14 V to 1.32 V, $T_A = T_L$ to T_H.
2. $\overline{\text{RESET}}$ pulse width is measured from 50% of the falling edge to 50% of the rising edge.

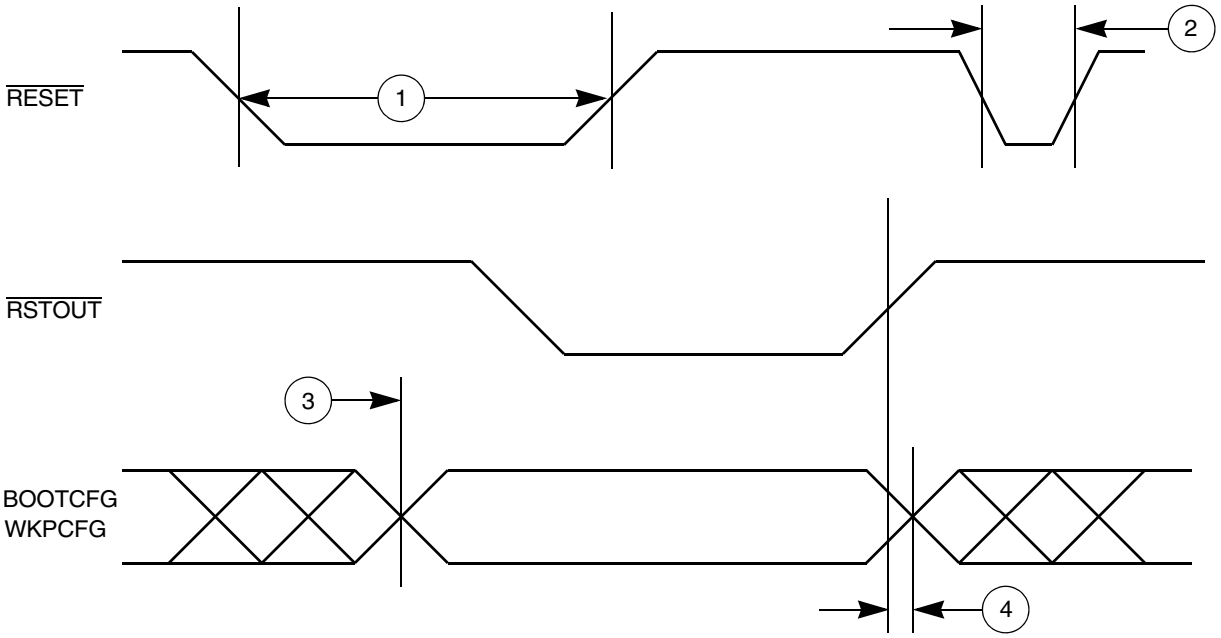


Figure 10. Reset and Configuration Pin Timing

next Nexus/JTAG command. Expect the affect of EVTI and RDY to be delayed by edges of TCK. Note: RDY is not available in all packages of all devices.

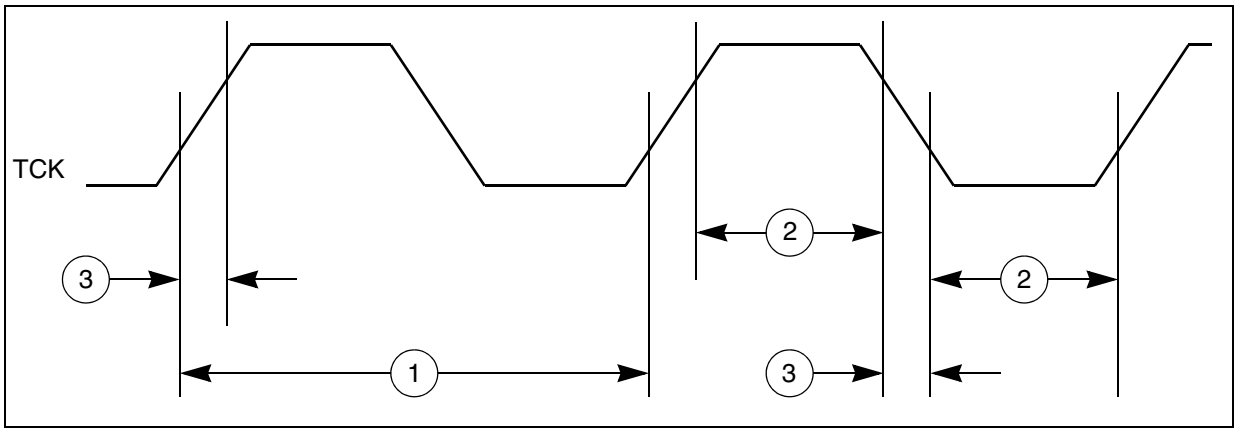


Figure 11. JTAG test clock input timing

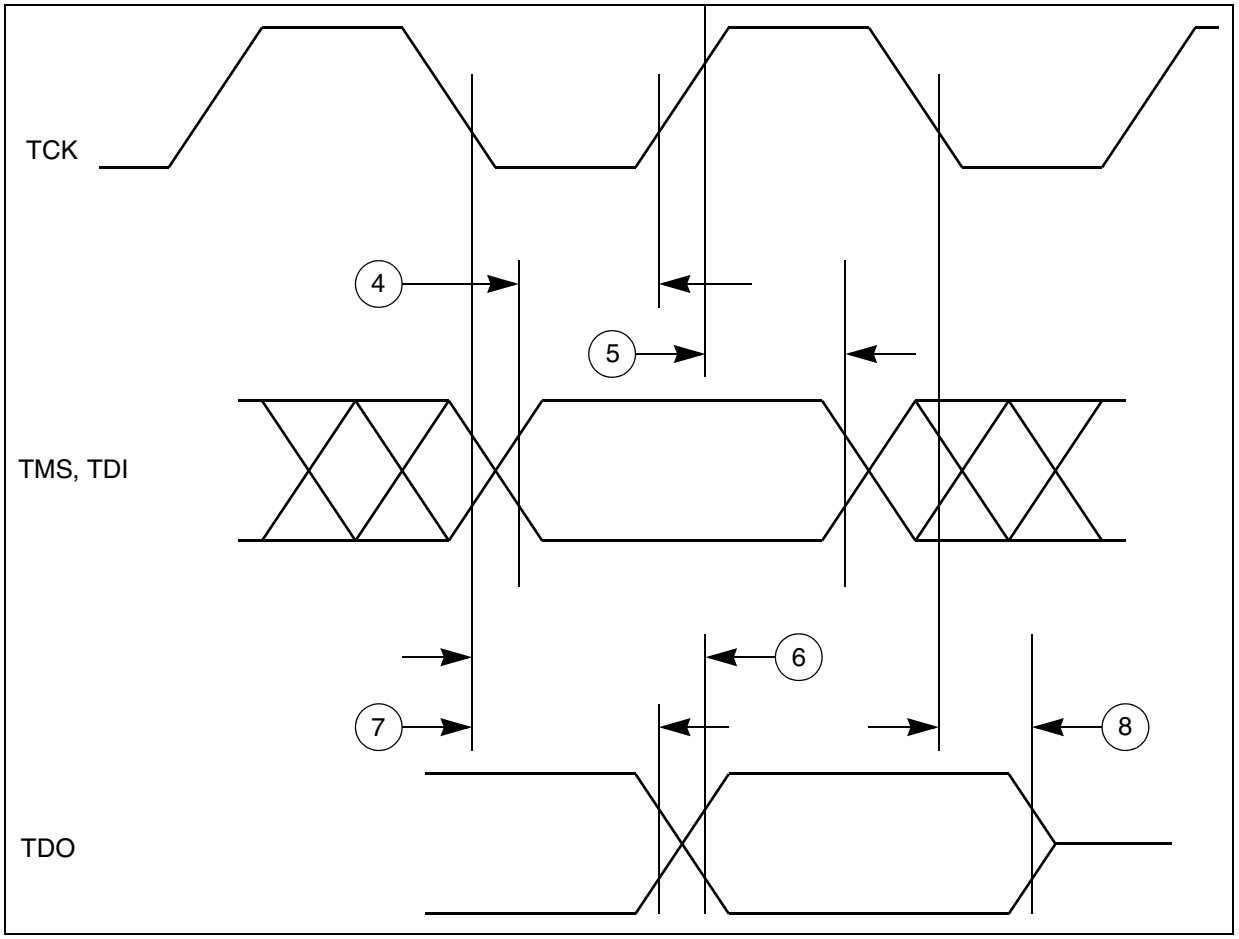
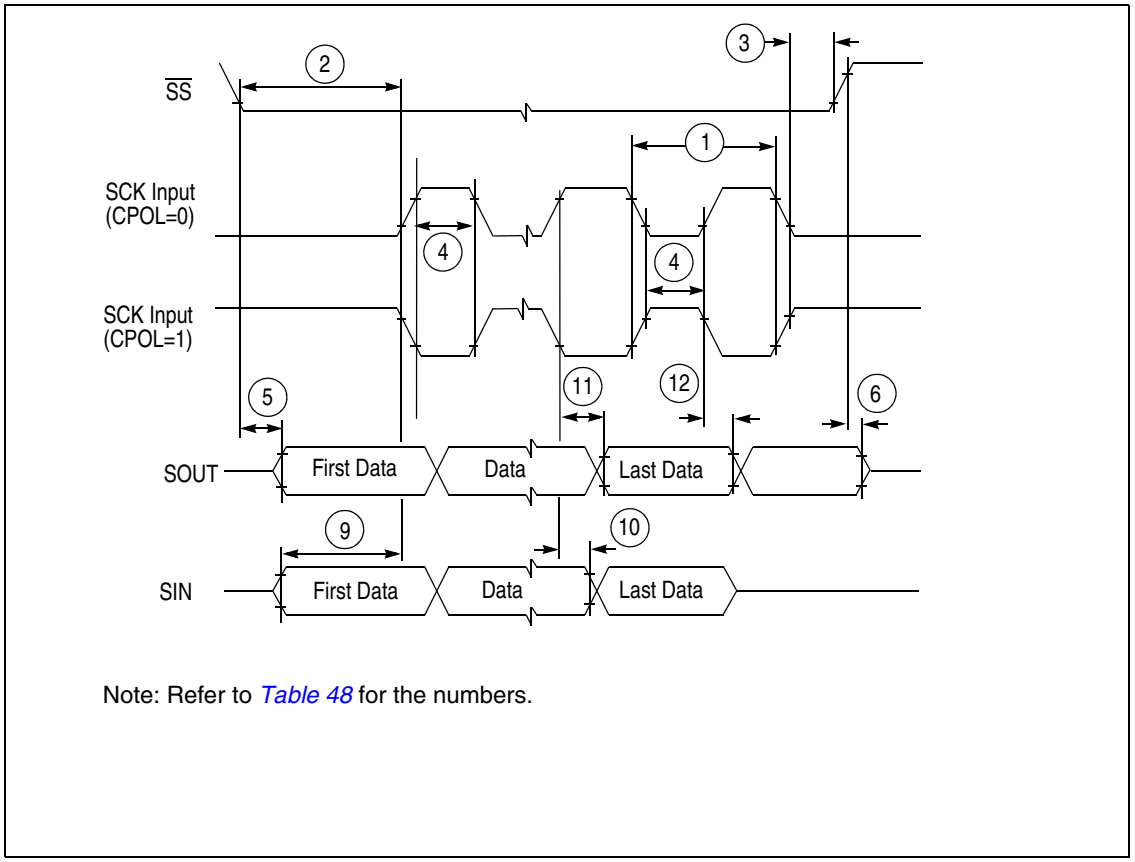


Figure 12. JTAG test access port timing



Note: Refer to *Table 48* for the numbers.

Figure 29. DSPI modified transfer format timing — slave, CPHA =0

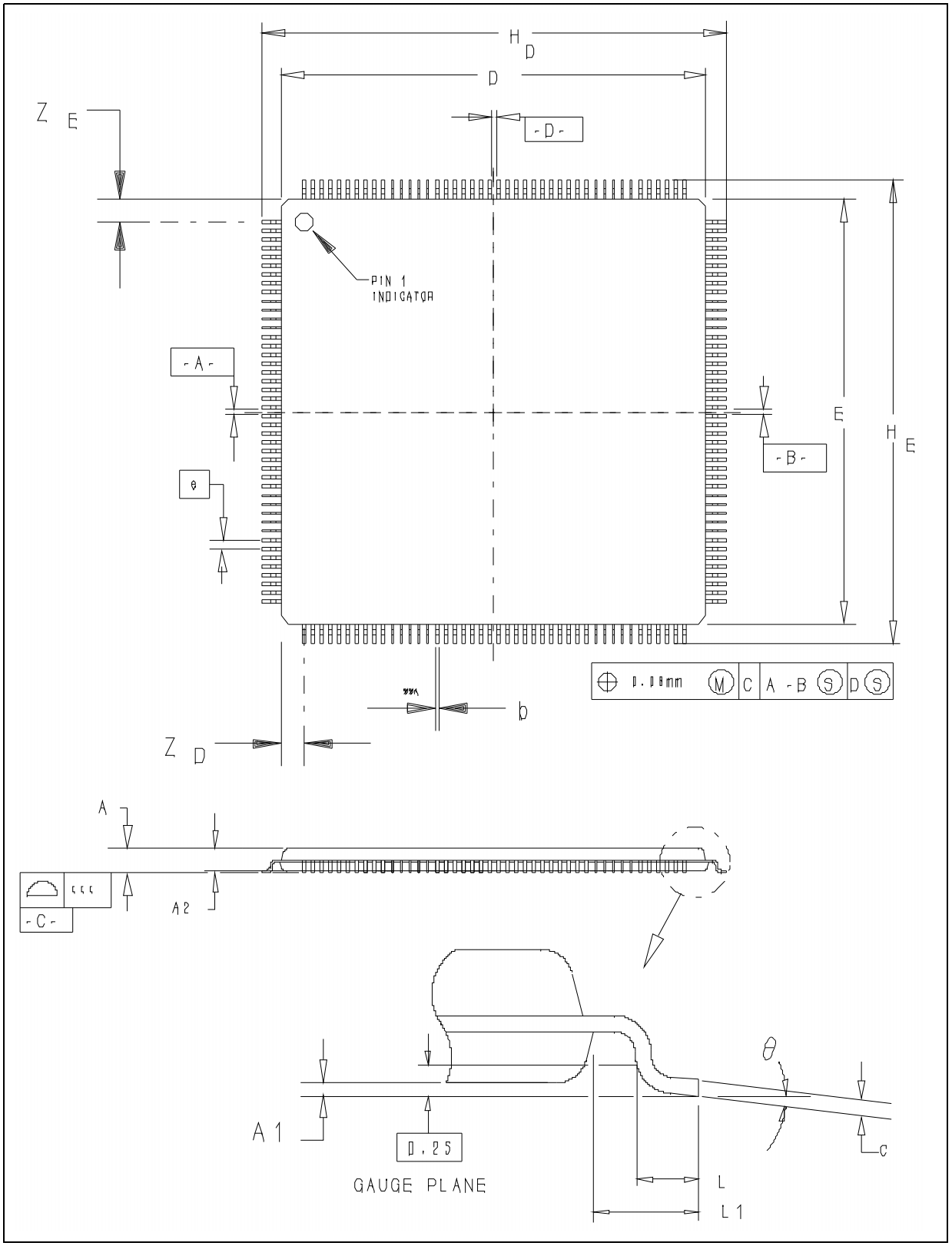


Figure 33. LQFP176 package mechanical drawing

Table 54. PBGA324 package mechanical data

Symbol	mm			inches		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A(1),(2),(3)		1.720		1.620	1.720	1.820
A1	0.270			0.350	0.400	0.450
A2		1.320			1.320	
b	0.550	0.6000	0.650	0.550	0.600	0.650
D	22.80	23.00	23.200	22.900	23.000	23.100
D1		21.00			21.000	
E	22.800	23.000	23.200	22.900	23.000	23.100
E1		21.000			21.000	
e	0.950	1.000	1.050	0.950	1.000	1.050
f	0.875	1.000	1.125	0.875	1.000	1.125
ddd			0.200			0.200

1. Max mounted height is 1.77mm.Based on 0.35mm ball pad diameter. Solder paste is 0.15mm thickness and 0.35mm diameter.
2. PBGA stands for Plastic Ball Grid Array.
3. The terminal A1 corner must be identified on the top surface by using a corner chamfer, ink or metallized markings, or other feature of package body or integral heatslug. A distinguishing feature is allowable on the bottom surface of the package to identify the terminal A1corner. Exact shape of each corner is optional.

Table 56. Revision history (continued)

Date	Revision	Changes
03-Feb-2012 (cont)	6 (cont)	– Added *Table 17: SPC564A80 External network specification*. – Updated *Figure 8: Core voltage regulator controller external components preferred configuration*. – Changed External Network Parameter Ce min value to “3*2.35µF+5µF” from “2*2.35µF+5µF” in *Table 17: SPC564A80 External network specification*. – Changed Trans. Line (differential Zo) unit to Ω from W in *Table 25: DSPI LVDS pad specification*.
07-Mar-2012	7	– Update table footnotes in *Table 21: DC electrical specifications*.
21-Mar-2012	8	– Minor editorial changes. – In *Section 1.4, “SPC564A80 feature list*, moved “24 unified channels” after “1 x eMIOS”. – In *Table 4,“SPC564A80 signal properties”*/Column “Name” updated the following rows: DSPI_D_SCK /GPIO [98] -Changed “-” to CS[2] DSPI_D_SIN /GPIO[99] -Changed “-” to CS[3]. – In *Table 12,“Thermal characteristics for 324-pin PBGA”*/ Column “Value” added conditional text. – In *Table 21,“DC electrical specifications”* made the following changes: -For the value “V_{OL_S}” parameter changed from “Slow/ medium/multi-voltage pad I/O output low voltage” to “Slow/medium pad I/O output low voltage”. -Added a new row for “$I_{DDSTBY27}$”. -For row “I_{DDSTBY}(operating current 0.95 -1.2V)” added max value “100” and changed typ value from “125” to “35”. -For row “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “110” and changed typ value from “135” to “45”. -For symbol “$I_{DDSTBY\ 150}$(operating current 0.95 -1.2V)” added max value “2000”, changed typ value from “1050” to “790”,C cell changed from “T” to “P” and for symbol “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “2000”, changed typ value from “1050” to “760”, C cell changed from “T” to “P”. -Removed note 9 and note 10 (Characterization based capability) from symbol “V_{OL_HS}”. – Splitted *Table 28,“eQADC conversion specifications (operating)”*into *Table 29,“eQADC single ended conversion specifications (operating)”* and *Table 30,“eQADC differential ended conversion specifications (operating)”*. – In *Table 30 ,“eQADC differential ended conversion specifications (operating)”*made the following changes: -Added the note of $DIFF_{cmv}$ on all of the DIFF specs. -Min value changed from (VRH-VRL)/2-5% to (VRH+VRL)/2-5 % and max value changed from (VRH-VRL)/2+5 % to (VRH+VRL)/2+5 %for DIFFcmv. – In *Table 31 ,“Cutoff frequency for additional SRAM wait state”*made the following changes: -Added note “Max frequencies including 2% PLL FM”. -Max operating frequency changed from “96” to “98” and “150” to “153”. – In *Section 3.13, “Configuring SRAM wait states*, changed text from “SPC564A80 4M Microcontroller Reference Manual “ to “device reference manual”.

Table 56. Revision history (continued)

Date	Revision	Changes
21-Mar-2012	8 (cont.)	– In *Table 32,"APC, RWSC, WWSC settings vs. frequency of operation"* - Added note for "Max Flash Operating Frequency(MHz). - Changed values from 30, 60,120, 150 to 20,61,123, 153 respectively in Max Flash Operating Frequency (MHz). – In *Table 33*,a,*"Flash program and erase specifications"*dded two parameter "T_{psrt}" and "T_{esrt}". – In *Table 41,"External Bus Interface maximum operating frequency"*, replacedthe <= symbol in notes with ≤ – Added note "Refer to table DSPI timing for the numbers" in all the figures under *Section 3.17.8, "DSPI timing* . In *Table 55*, changed LBGA208 to MAPBGA and changed all packages to 123XXXX format. – Added *Table 17,"SPC564A80 External network specification"*. – Updated *Figure 8*. – Changed External Network Parameter Ce min value to "3*2.35µF+5µF" from "2*2.35µF+5µF" in *Table 17,"SPC564A80 External network specification"*. Changed Trans. Line (differential Zo) unit to Ω from W in *Table 25,"DSPI LVDS pad specification"*.
18-Sep-2013	9	– Updated Disclaimer.