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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z4
Core Size	32-Bit Single-Core
Speed	120MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	118
Program Memory Size	4MB (4M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc564a80l7coby

Contents

Table 2. SPC564A80, SPC563M64 and SPC564A70 comparison (continued)

Feature		SPC564A80	SPC563M64	SPC564A70
	Micro Second Channel (MSC) bus downlink	Yes		
	DSPI_A	No		
	DSPI_B	Yes (with LVDS)		
	DSPI_C	Yes (with LVDS)		
	DSPI_D	Yes	No	Yes
FlexRay		Yes	No	Yes
System timers		5 PIT channels 4 STM channels 1 Software Watchdog		
eMIOS		24 ch.	16 ch.	24 ch.
eTPU		32 ch. eTPU2		
	Code memory	14 KB		
	Data memory	3 KB		
Interrupt controller		486 ch.(1)	307 ch.	486 ch.(1)
ADC		40 ch.	34 ch.	40 ch.
	ADC_A	Yes		
	ADC_B	Yes		
	Temp sensor	Yes		
	Variable gain amp.	Yes		
	Decimation filter	2	1	2
	Sensor diagnostics	Yes		
CRC		Yes	No	Yes
FMPLL		Yes		
VRC		Yes		
Supplies		5 V, 3.3 V(2)	5 V, 3.3 V(3)	5 V, 3.3 V(2)
Low-power modes		Stop Mode Slow Mode		
Packages		LQFP176(4) LBGA208(4) PBGA Known Good Die (KGD) 496-pin CSP(5)	LQFP100 LQFP144 LQFP176 LBGA208 496-pin CSP(5)	LQFP176(4) LBGA208(4) PBGAKnown Good Die (KGD) 496-pin CSP(5)

1. 199 interrupt vectors are reserved.
2. 5 V single supply only for LQFP176.
3. 5 V single supply only for LQFP144 and LQFP100.
4. Pinout compatible with STMicroelectronics' SPC563M64 devices.
5. For ST calibration tool only.

1.4 SPC564A80 feature list

- 150 MHz e200z4 Power Architecture core
  - Variable length instruction encoding (VLE)
  - Superscalar architecture with 2 execution units
  - Up to 2 integer or floating point instructions per cycle
  - Up to 4 multiply and accumulate operations per cycle
- Memory organization
  - 4 MB on-chip flash memory with ECC and Read While Write (RWW)
  - 192 KB on-chip SRAM with standby functionality (32 KB) and ECC
  - 8 KB instruction cache (with line locking), configurable as 2- or 4-way
  - 14 + 3 KB eTPU code and data RAM
  - 5 × 4 crossbar switch (XBAR)
  - 24-entry MMU
  - External Bus Interface (EBI) with slave and master port
- Fail Safe Protection
  - 16-entry Memory Protection Unit (MPU)
  - CRC unit with 3 sub-modules
  - Junction temperature sensor
- Interrupts
  - Configurable interrupt controller (with NMI)
  - 64-channel DMA
- Serial channels
  - 3 × eSCI
  - 3 × DSPI (2 of which support downstream Micro Second Channel [MSC])
  - 3 × FlexCAN with 64 messages each
  - 1 × FlexRay module (V2.1) up to 10 Mbit/s with dual or single channel and 128 message objects and ECC
- 1 × eMIOS: 24 unified channels
- 1 × eTPU2 (second generation eTPU)
  - 32 standard channels
  - 1 × reaction module (6 channels with three outputs per channel)
- 2 enhanced queued analog-to-digital converters (eQADCs)
  - Forty 12-bit input channels (multiplexed on 2 ADCs); expandable to 56 channels with external multiplexers
  - 6 command queues
  - Trigger and DMA support
  - 688 ns minimum conversion time
- On-chip CAN/SCI/FlexRay Bootstrap loader with Boot Assist Module (BAM)
- Nexus
  - Class 3+ for the e200z4 core
  - Class 1 for the eTPU
- JTAG (5-pin)

- An access protection error is detected if a memory reference does not hit in any memory region or the reference is flagged as illegal in all memory regions where it does hit. In the event of an access error, the XBAR reference is terminated with an error response and the MPU inhibits the bus cycle being sent to the targeted slave device
- 64-bit error registers, one for each XBAR slave port, capture the last faulting address, attributes, and detail information

1.5.6 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable. The PLL has the following major features:

- Input clock frequency from 4 MHz to 40 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without forcing the PLL to relock
- Three modes of operation
  - Bypass mode with PLL off
  - Bypass mode with PLL running (default mode out of reset)
  - PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation
  - Modulation enabled/disabled through software
  - Triangle wave modulation up to 100 kHz modulation frequency
  - Programmable modulation depth (0% to 2% modulation depth)
  - Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Clock Quality Module
  - Detects the quality of the crystal clock and causes interrupt request or system reset if error is detected
  - Detects the quality of the PLL output clock; if error detected, causes system reset or switches system clock to crystal clock and causes interrupt request
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation

1.5.7 SIU

The SPC564A80 SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The

a. EBI not available on all packages and is not available, as a master, for customer.

- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.

The eTPU2 includes these distinctive features:

- 32 channels; each channel associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators.
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host
- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands.
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, that is, one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel

The FlexCAN modules provide the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1088 bytes of embedded memory for message buffer storage
- Includes 256-byte memory for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi-master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

The Error Correction Status Module supports a number of miscellaneous control functions for the platform. The ECSM includes these features:

- Registers for capturing information on platform memory errors if error-correcting codes (ECC) are implemented
- For test purposes, optional registers to specify the generation of double-bit memory errors are enabled on the SPC564A80.

The sources of the ECC errors are:

- Flash
- SRAM
- Peripheral RAM (FlexRay, CAN, eTPU2 Parameter RAM)

1.5.22 External bus interface (EBI)

The SPC564A80 device features an external bus interface that is available in PBGA324 and calibration packages.

The EBI supports operation at frequencies of system clock /1, /2 and /4, with a maximum frequency support of 80 MHz. Customers running the device at 120 MHz or 132 MHz will use the /2 divider, giving an EBI frequency of 60 MHz or 66 MHz. Customers running the device at 80 MHz will be able to use the /1 divider to have the EBI run at the full 80 MHz frequency.

Features include:

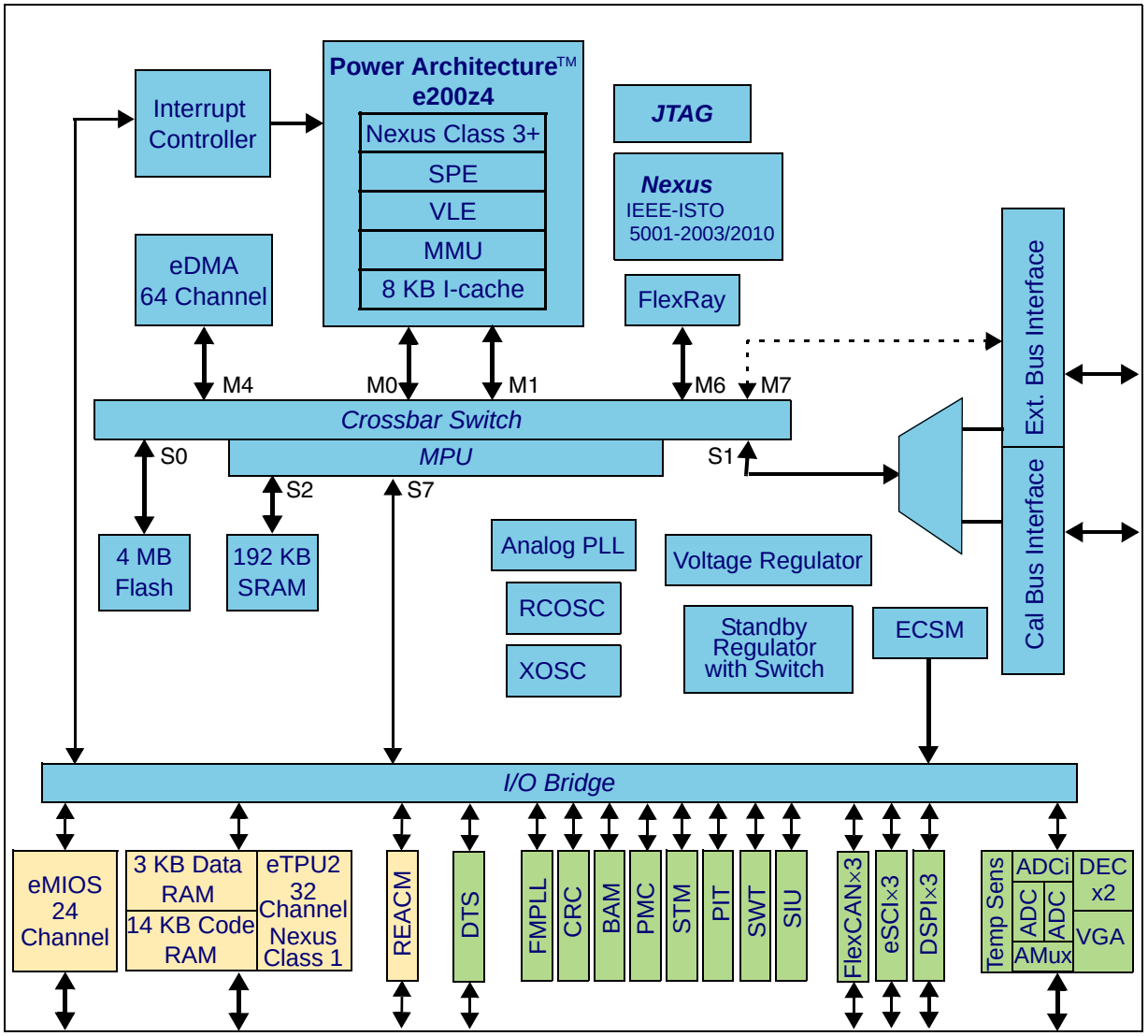
- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller with support for various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing included to support 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states

1.5.23 Calibration EBI

The Calibration EBI controls data transfer across the crossbar switch to/from memories or peripherals attached to the calibration tool connector in the calibration address space. The Calibration EBI is only available in the calibration tool.

Features include:

- 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
- Memory controller supports various memory types
- 16-bit data bus, up to 22-bit address bus
- Pin muxing supports 32-bit muxed bus
- Selectable drive strength
- Configurable bus speed modes
- Bus monitor
- Configurable wait states



LEGEND

ADC – Analog to Digital Converter
ADCi – ADC interface
AMux – Analog Multiplexer
BAM – Boot Assist Module
CRC – Cyclic Redundancy Check unit
DEC – Decimation Filter
DTS – Development Trigger Semaphore
DSPI – Deserial/Serial Peripheral Interface
EBI – External Bus Interface
ECSM – Error Correction Status Module
eDMA – Enhanced Direct Memory Access
eMIOS – Enhanced Modular Input Output System
eSCI – Enhanced Serial Communications Interface
eTPU2 – Second gen. Enhanced Time Processing Unit
FlexCAN – Controller Area Network (FlexCAN)
FMPLL – Frequency-Modulated Phase Locked Loop
JTAG – IEEE 1149.1 test controller
MMU – Memory Management Unit
MPU – Memory Protection Unit
PMC – Power Management Controller
PIT – Periodic Interrupt Timer
RCOSC – low-speed RC oscillator
REACM – Reaction module
SIU – System Integration Unit
SPE – Signal Processing Extension
SRAM – Static RAM
STM – System Timer Module
SWT – Software Watchdog Timer
VGA – Variable Gain Amplifier
VLE – Variable Length (instruction) Encoding
XOSC – XTAL Oscillator

Figure 1. SPC564A80 series block diagram

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VRH	Voltage Reference High	P	—	—	I	VDDA —	I / —	VRH	163	A8	A10
VRL	Voltage Reference Low	P	—	—	I	VDDA —	I / —	VRL	162	A9	A11
REFBYBC	Reference Bypass Capacitor Input	P	—	—	I	VDDA Analog	I / —	REFBYPC	164	B7	B10
eTPU2											
TCRCLKA IRQ[7] GPIO[113]	eTPU A TCR clock External interrupt request GPIO	P A1 G	01 10 00	113	I I I/O	VDDEH4 Slow	— / Up	— / Up	—	L4	M2
ETPUA0 ETPUA12_O[8] ETPUA19_O[8] GPIO[114]	eTPU A channel eTPU A channel (output only) eTPU A channel (output only) GPIO	P A1 A2 G	001 010 100 000	114	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	61	N3	L3
ETPUA1 ETPUA13_O[8] GPIO[115]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	115	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	60	M3	L4
ETPUA2 ETPUA14_O[8] GPIO[116]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	116	I/O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	59	P2	K3
ETPUA3 ETPUA15_O[8] GPIO[117]	eTPU A channel eTPU A channel (output only) GPIO	P A1 G	01 10 00	117	I/O O I/O	VDDEH4 Slow	— / WKPCFG	GPIO / WKPCFG	58	P1	L2
ETPUA4 ETPUA16_O[8] FR_B_TX GPIO[118]	eTPU A channel eTPU A channel (output only) Flexray TX data channel B GPIO	P A1 A3 G	0001 0010 1000 0000	118	I/O O O I/O	VDDEH4 Slow	— / WKPCFG	— / WKPCFG	56	N2	L1

Table 4. SPC564A80 signal properties (continued)

Name	Function[1]	PAG[2]	PCR PA Field[3]	PCR[4]	I/O Type	Voltage[5] / Pad Type[6]	Status[7]		Package pin #		
							During Reset	After Reset	176	208	324
VDD	Core supply for input or decoupling	—		—	I	1.2 V	I / —	VDD	33, 45, 62, 103, 132, 149, 176	B1, B16, C2, D3, E4, N5, P4, P13, R3, R14, T2, T15	A2, A20, B3, C4, C22, D5, V19, W5, W20, Y4, Y21, AA3, AA22, AB2
VDDE12	External supply input for calibration bus interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE12	—	—	—
VDDE2[23]	External supply input for EBI interfaces	—		—	I	1.8 V - 3.3 V	I / —	VDDE2[24]	—	—	M9, M10, N11, P11, W6, W8, Y5, AA4, AA6, AA10, AB3
VDDE5	External supply input for ENGCLK, CLKOUT and EBI signals DATA[0:15]	—		—	I	1.8 V - 3.3 V	I / —	VDDE5	—	T13	W17, Y18, AA19, AB20
VDDE-EH	External supply for EBI interfaces	—		—	I	3.0 V - 5 V	I / —	VDDE-EH	—	—	R3, W2
VDDEH1A[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1A[25]	31	—	—
VDDEH1B[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1B[25]	41	—	—
VDDEH1AB[25]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH1AB[25]	—	K4	H4
VDDEH4[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4[26]	—	—	—
VDDEH4A[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4A[26]	55	—	—
VDDEH4B[26]	I/O Supply Input	—		—	I	3.3 V - 5.0 V	I / —	VDDEH4B[26]	74	—	—

Table 7. Power/ground segmentation (continued)

Power Segment	Voltage	I/O Pins Powered by Segment
Other Power Segments		
VDDREG	5 V	—
VRCCTL	—	—
VDDPLL	1.2 V	—
VSTBY	0.95–1.2 V (unregulated mode)	—
	2.0–5.5 V (regulated mode)	—
VSS	—	—

1. Do not use VRC33 to drive external circuits.

Table 21. DC electrical specifications (continued)

Symbol		C	Parameter	Conditions	Value			Unit
					min	typ	max	
V_{IL_F}	CC	C	Fast pad I/O input low voltage	Hysteresis enabled	V_{SS}-0.3	—	0.35*V_{DDE}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.40*V_{DDE}	
V_{IL_LS}	CC	C	Multi-voltage I/O pad input low voltage in Low-swing-mode[5],[6],[7],[8]	Hysteresis enabled	V_{SS}-0.3	—	0.8	V
		P		Hysteresis disabled	V_{SS}-0.3	—	1.1	
V_{IL_HS}	CC	C	Multi-voltage pad I/O input low voltage in high-swing-mode	Hysteresis enabled	V_{SS}-0.3	—	0.35 V_{DDEH}	V
		P		Hysteresis disabled	V_{SS}-0.3	—	0.4 V_{DDEH}	
V_{IH_S}	CC	C	Slow/medium pad I/O input high voltage[9]	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{IH_F}	CC	C	Fast I/O input high voltage	Hysteresis enabled	0.65 V_{DDE}	—	V_{DDE}+0.3	V
		P		Hysteresis disabled	0.58 V_{DDE}	—	V_{DDE}+0.3	
V_{IH_LS}	CC	C	Multi-voltage pad I/O input high voltage in low-swing-mode[5],[6],[7],[8]	Hysteresis enabled	2.5	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	2.2	—	V_{DDEH}+0.3	
V_{IH_HS}	CC	C	Multi-voltage I/O input high voltage in high-swing-mode	Hysteresis enabled	0.65 V_{DDEH}	—	V_{DDEH}+0.3	V
		P		Hysteresis disabled	0.55 V_{DDEH}	—	V_{DDEH}+0.3	
V_{OL_S}	CC	P	Slow/medium pad I/O output low voltage[9]		—	—	0.2*V_{DDEH}	V
V_{OL_F}	CC	P	Fast I/O output low voltage[9]		—	—	0.2*V_{DDE}	V
V_{OL_LS}	CC	P	Multi-voltage pad I/O output low voltage in low-swing mode[5],[6],[7],[8],[9]		—	—	0.6	V

Table 33. Flash program and erase specifications(1) (continued)

#	Symbol		C	Parameter	Min. Value	Typical Value	Initial Max(2)	Max(3)	Unit
5	$T_{64kpperase}$	CC	P	64 KB Block Pre-program and Erase Time	—	800	1800	5000	ms
6	$T_{128kpperase}$	CC	P	128 KB Block Pre-program and Erase Time	—	1500	3000	7500	ms
7	$T_{256kpperase}$	CC	P	256 KB Block Pre-program and Erase Time	—	3000	5300	15000	ms
8	T_{psrt}	SR	—	Program suspend request rate(5)	100	—	—	—	µs
9	T_{esrt}	SR	—	Erase suspend request rate (6)	10				ms

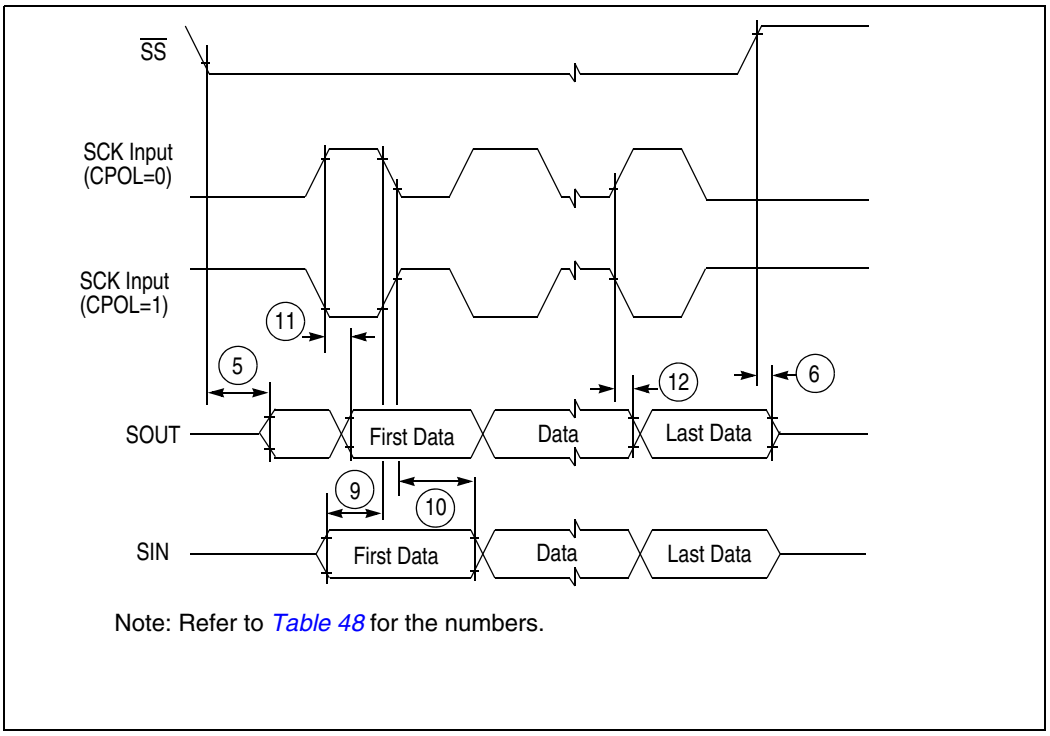
1. Typical program and erase times assume nominal supply values and operation at 25 °C. All times are subject to change pending device characterization.
2. Initial factory condition: ≤ 100 program/erase cycles, 25 °C, typical supply voltage, 80 MHz minimum system frequency.
3. The maximum erase time occurs after the specified number of program/erase cycles. This maximum value is characterized but not guaranteed.
4. Page size is 128 bits (4 words).
5. Time between program suspend resume and the next program suspend request.
6. Time between erase suspend resume and the next erase suspend request.

Table 34. Flash module life

Symbol		C	Parameter	Conditions	Value		Unit
					min	typ	
P/E	CC	C	Number of program/erase cycles per block for 16 KB, 48 KB, and 64 Kbyte blocks over the operating temperature range (T_J)	—	100,000	—	P/E cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte and 256 Kbyte blocks over the operating temperature range (T_J)	—	1,000	100,000	P/E cycles
Data Retention	CC	C	Minimum data retention at 85 °C average ambient temperature(1)	Blocks with 0 – 1,000 P/E cycles	20	—	years
				Blocks with 1,001 – 10,000 P/E cycles	10	—	years
				Blocks with 10,001 – 100,000 P/E cycles	5	—	years

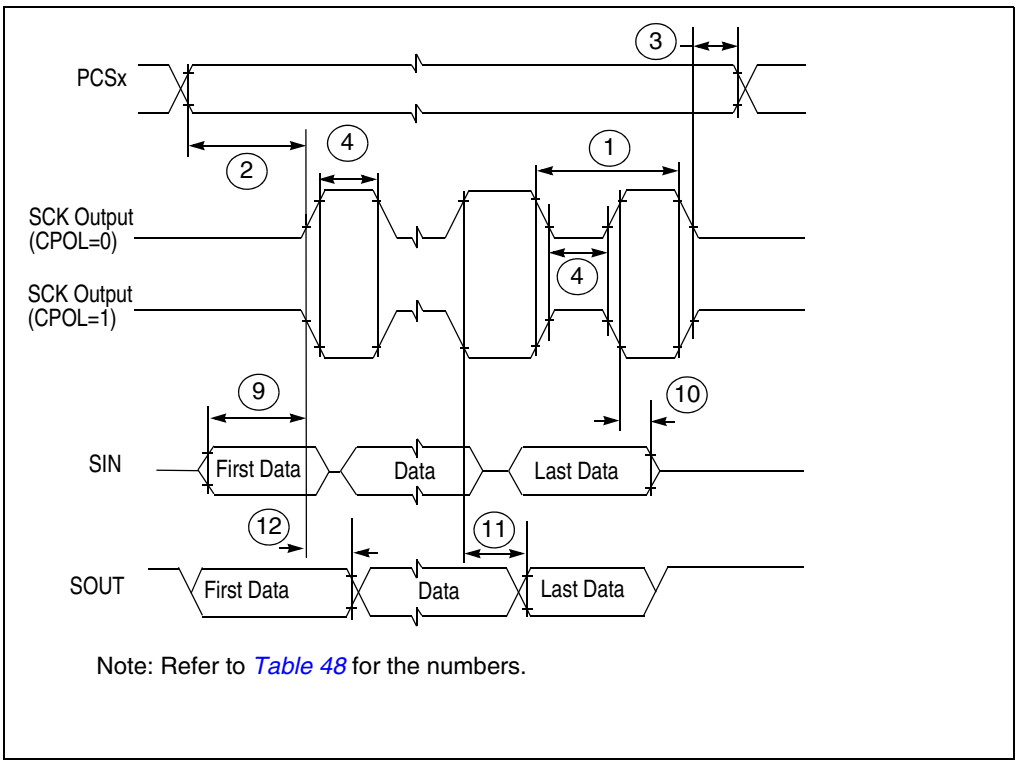
1. Ambient temperature averaged over duration of application, not to exceed product operating temperature range.

Figure 25. DSPI classic SPI timing — slave, CPHA = 0



Note: Refer to *Table 48* for the numbers.

Figure 26. DSPI classic SPI timing — slave, CPHA = 1



Note: Refer to *Table 48* for the numbers.

Figure 27. DSPI modified transfer format timing — master, CPHA = 0

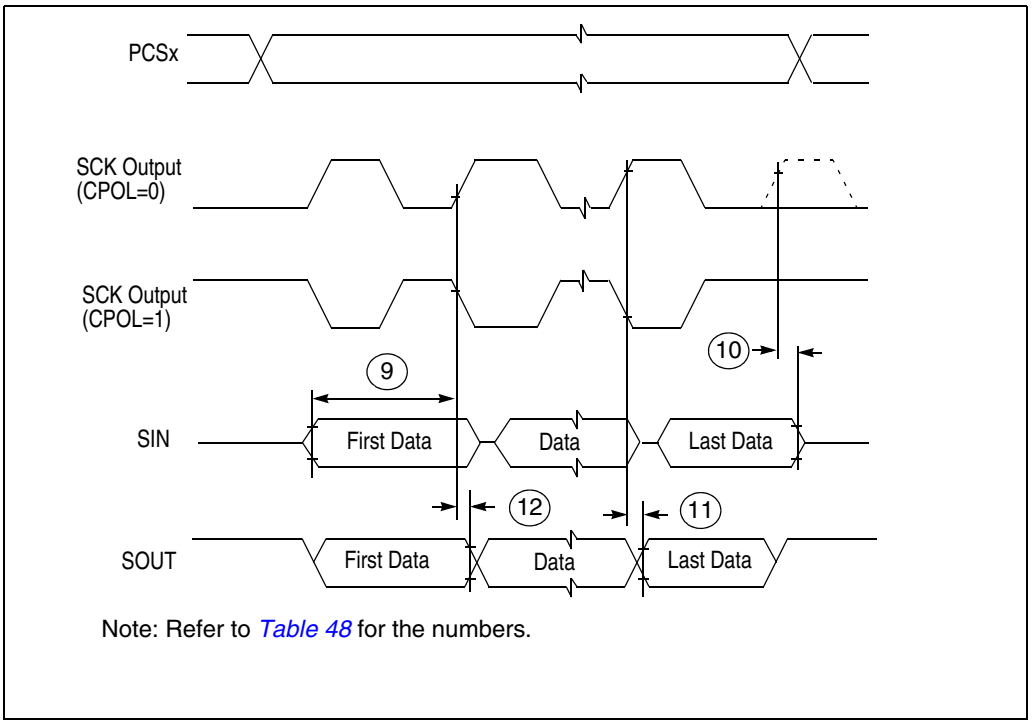


Figure 28. DSPI modified transfer format timing — master, CPHA = 1

Table 56. Revision history (continued)

Date	Revision	Changes
02-Apr-2010	3	Internal release. Changes to Signal Properties table (changes apply to Revision 2 and later devices: EBI changes: – WE_BE[2] (A2) and CAL_WE_BE[2] (A3) signals added to CS[2] (PCR 2) – WE_BE[3] (A2) and CAL_WE_BE[3] (A3) signals added to CS[3] (PCR 3) Calibration bus changes: – CAL_WE[2]/BE[2] (A2) signal added to CAL_CS[2] (PCR 338) – CAL_WE[3]/BE[3] (A2) signal added to CAL_CS[3] (PCR 339) – CAL_ALE (A1) added to CAL_ADDR[15] (PCR 340) eQADC changes: – AN[8] and AN[38] pins swapped. AN[8] Is now on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball). AN[8] was on C5 (324-ball) on previous devices. AN[38] Is now on C5 (324-ball). AN[38] was on pins 9 (176-pin), B3 (208-ball) and D6 (324-ball) on previous devices. – ANZ function added to AN11 pin Reaction channels added to eTPU2: – RCH0_A (A3) added to ETPU_A[14] (PCR 128) – RCH0_B (A2) added to ETPU_A[20] (PCR 134) – RCH0_C (A2) added to ETPU_A[21] (PCR 135) – RCH1_A (A2) added to ETPU_A[15] (PCR 129) – RCH1_B (A2) added to ETPU_A[9] (PCR 123) – RCH1_C (A2) added to ETPU_A[10] (PCR 124) – RCH2_A (A2) added to ETPU_A[16] (PCR 130) – RCH3_A (A2) added to ETPU_A[17] (PCR 131 – RCH4_A (A2) added to ETPU_A[18] (PCR 132)) – RCH4_B (A2) added to ETPU_A[11] (PCR 125) – RCH4_C (A2) added to ETPU_A[12] (PCR 126) – RCH5_A (A2) added to ETPU_A[19] (PCR 133) – RCH5_B (A2) added to ETPU_A[28] (PCR 142) – RCH5_C (A2) added to ETPU_A[29] (PCR 143) Reaction channels added to eMIOS: – RCH2_B (A2) added to EMIOS[2] (PCR 181) – RCH2_C (A2) added to EMIOS[4] (PCR 183) – RCH3_B (A2) added to EMIOS[10] (PCR 189) – RCH3_C (A2) added to EMIOS[11] (PCR 190) Pad changes: – ETPUA16 (PCR 130) has Medium (was Slow) pad – ETPUA17 (PCR 131) has Medium (was Slow) pad – ETPUA18 (PCR 132) has Medium (was Slow) pad – ETPUA19 (PCR 133) has Medium (was Slow) pad – ETPUA25 (PCR 139) has Slow+LVDS (was Medium+LVDS) pads

Table 56. Revision history (continued)

Date	Revision	Changes
03-Feb-2012	6	– Minor editorial changes. – In *Section 1.4: SPC564A80 feature list*, moved “24 unified channels” after “1 x eMIOS”. – In *Table 4* updated the following rows: DSPI_D_SCK /GPIO [98] -Changed “-” to CS[2] DSPI_D_SIN /GPIO[99] -Changed “-” to CS[3]. – In *Table 12* Column “Value” added conditional text. – In *Table 21* made the following changes: -For the value “VOL_S” parameter changed from “Slow/ medium/multi-voltage pad I/O output low voltage” to “Slow/medium pad I/O output low voltage”. -Added a new row for “IDDSTBY27”. -For row “IDDSTBY(operating current 0.95 -1.2V)” added max value “100” and changed typ value from “125” to “35”. -For row “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “110” and changed typ value from “135” to “45”. -For symbol “$I_{DDSTBY\ 150}$(operating current 0.95 -1.2V)” added max value “2000”, changed typ value from “1050” to “790”,C cell changed from “T” to “P” and for symbol “I_{DDSTBY} (operating current 2 - 5.5V)” added max value “2000”, changed typ value from “1050” to “760”, C cell changed from “T” to “P”. -Removed note 9 and note 10 (Characterization based capability) from symbol “V_{OL_HS}”. – Splitted *Table 28: eQADC conversion specifications (operating)* into *Table 29: eQADC single ended conversion specifications (operating)* and *Table 30: eQADC differential ended conversion specifications (operating)* – In *Table 30: eQADC differential ended conversion specifications (operating)* made the following changes: -Added the note of $DIFF_{cmv}$ on all of the DIFF specs. -Min value changed from (VRH-VRL)/2-5% to (VRH+VRL)/2-5 % and max value changed from (VRH-VRL)/2+5% to (VRH+VRL)/2+5%for DIFFcmv. – In *Table 31: Cutoff frequency for additional SRAM wait state* made the following changes: -Added note “Max frequencies including 2% PLL FM”. -Max operating frequency changed from “96” to “98” and “150” to “153”. – In *Section 3.13: Configuring SRAM wait states*, changed text from “SPC564A80 4M Microcontroller Reference Manual “ to “device reference manual”. – In *Table 32: APC, RWSC, WWSC settings vs. frequency of operation* - Added note for “Max Flash Operating Frequency(MHz). - Changed values from 30, 60,120, 150 to 20,61,123, 153 respectively in Max Flash Operating Frequency (MHz). – In *Table 33: Flash program and erase specifications*, added two parameter “T_{psrt}” and “T_{esrt}”. – In *Table 41: External Bus Interface maximum operating frequency*, replacedthe <= symbol in notes with ≤ – Added note “Refer to table DSPI timing for the numbers” in all the figures under *Section 3.17.8: DSPI timing* .

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