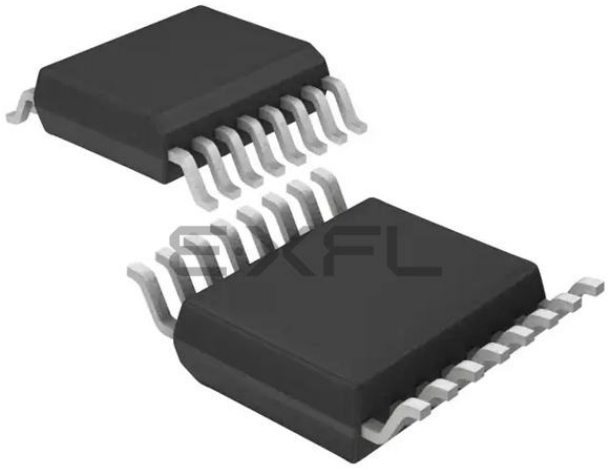

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	LINbus
Peripherals	LVD, POR, PWM
Number of I/O	13
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 6x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mc908ql4mdte

- System protection features:
  - Computer operating properly (COP) watchdog
  - Low-voltage detection with reset
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Power-on reset
- Memory mapped I/O registers
- Power saving stop and wait modes
- Available packages:
  - 16-pin small outline integrated circuit (SOIC) package
  - 16-pin thin shrink small outline package (TSSOP)

Features of the CPU08 include the following:

- Enhanced HC05 programming model
- Extensive loop control functions
- 16 addressing modes (eight more than the HC05)
- 16-bit index register and stack pointer
- Memory-to-memory data transfers
- Fast 8 × 8 multiply instruction
- Fast 16/8 divide instruction
- Binary-coded decimal (BCD) instructions
- Optimization for controller applications
- Efficient C language support

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68HC908QL4.

1.4 Pin Functions

Table 1-1 provides a description of the pin functions.

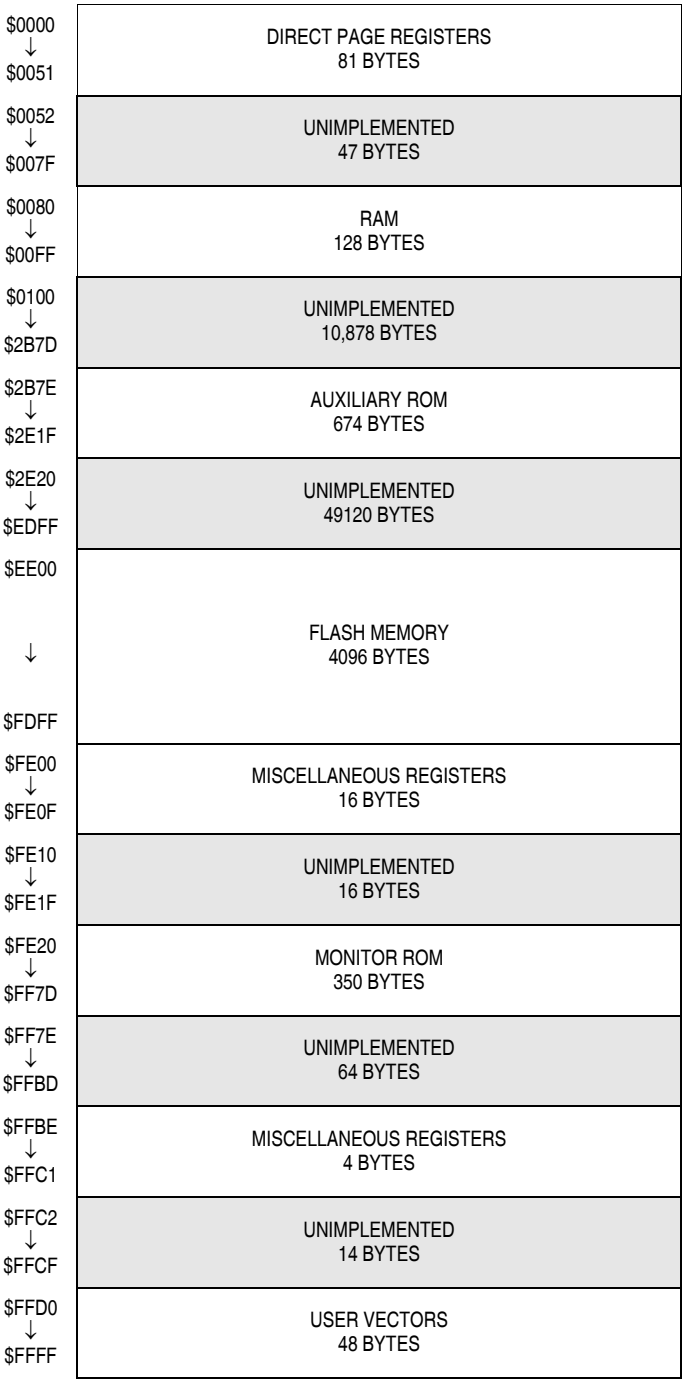


Figure 2-1. Memory Map

charging. If externally available, connect the V_{REFL} pin to the same potential as V_{SSA} at the single point ground location.

3.7.5 ADC10 Channel Pins (ADn)

The ADC10 has multiple input channels. Empirical data shows that capacitors on the analog inputs improve performance in the presence of noise or when the source impedance is high. 0.01 μF capacitors with good high-frequency characteristics are sufficient. These capacitors are not necessary in all cases, but when used they must be placed as close as possible to the package pins and be referenced to V_{SSA}.

3.8 Registers

These registers control and monitor operation of the ADC10:

- ADC10 status and control register, ADCSC
- ADC10 data registers, ADRH and ADRL
- ADC10 clock register, ADCLK

3.8.1 ADC10 Status and Control Register

This section describes the function of the ADC10 status and control register (ADCSC). Writing ADCSC aborts the current conversion and initiates a new conversion (if the ADCH[4:0] bits are equal to a value other than all 1s).

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
Write:								
Reset:	0	0	0	1	1	1	1	1

= Unimplemented

Figure 3-3. ADC10 Status and Control Register (ADCSC)

COCO — Conversion Complete Bit

COCO is a read-only bit which is set each time a conversion is completed. This bit is cleared whenever the status and control register is written or whenever the data register (low) is read.

1 = Conversion completed
0 = Conversion not completed

AIEN — ADC10 Interrupt Enable Bit

When this bit is set, an interrupt is generated at the end of a conversion. The interrupt signal is cleared when the data register is read or the status/control register is written.

1 = ADC10 interrupt enabled
0 = ADC10 interrupt disabled

ADCO — ADC10 Continuous Conversion Bit

When this bit is set, the ADC10 will begin to convert samples continuously (continuous conversion mode) and update the result registers at the end of each conversion, provided the ADCH[4:0] bits do not decode to all 1s. The ADC10 will continue to convert until the MCU enters reset, the MCU enters stop mode (if ACLKEN is clear), ADCLK is written, or until ADCSC is written again. If stop is entered

Chapter 7
Central Processor Unit (CPU)

7.1 Introduction

The M68HC08 CPU (central processor unit) is an enhanced and fully object-code-compatible version of the M68HC05 CPU. The *CPU08 Reference Manual* (document order number CPU08RM/AD) contains a description of the CPU instruction set, addressing modes, and architecture.

7.2 Features

Features of the CPU include:

- Object code fully upward-compatible with M68HC05 Family
- 16-bit stack pointer with stack manipulation instructions
- 16-bit index register with x-register manipulation instructions
- 8-MHz CPU internal bus frequency
- 64-Kbyte program/data memory space
- 16 addressing modes
- Memory-to-memory data moves without using accumulator
- Fast 8-bit by 8-bit multiply and 16-bit by 8-bit divide instructions
- Enhanced binary-coded decimal (BCD) data handling
- Modular architecture with expandable internal bus definition for extension of addressing range beyond 64 Kbytes
- Low-power stop and wait modes

7.3 CPU Registers

Figure 7-1 shows the five CPU registers. CPU registers are not part of the memory map.

The LVI module contains a bandgap reference circuit and comparator. When the LVITRIP bit is cleared, the default state at power-on reset, V_{TRIPF} is configured for the lower V_{DD} operating range. The actual trip points are specified in 17.5 5-V DC Electrical Characteristics and 17.8 3.3-V DC Electrical Characteristics.

Because the default LVI trip point after power-on reset is configured for low voltage operation, a system requiring high voltage LVI operation must set the LVITRIP bit during system initialization. V_{DD} must be above the LVI trip rising voltage, V_{TRIPR}, for the high voltage operating range or the MCU will immediately go into LVI reset.

After an LVI reset occurs, the MCU remains in reset until V_{DD} rises above V_{TRIPR}. See Chapter 13 System Integration Module (SIM) for the reset recovery sequence.

The output of the comparator controls the state of the LVIOUT flag in the LVI status register (LVISR) and can be used for polling LVI operation when the LVI reset is disabled.

The LVI is enabled out of reset. The following bits located in the configuration register can alter the default conditions.

- Setting the LVI power disable bit, LVIPWRD, disables the LVI.
- Setting the LVI reset disable bit, LVIRSTD, prevents the LVI module from generating a reset.
- Setting the LVI enable in stop mode bit, LVISTOP, enables the LVI to operate in stop mode.
- Setting the LVI trip point bit, LVITRIP, configures the trip point voltage (V_{TRIPF}) for the higher V_{DD} operating range.

10.3.1 Polled LVI Operation

In applications that can operate at V_{DD} levels below the V_{TRIPF} level, software can monitor V_{DD} by polling the LVIOUT bit. In the configuration register, LVIPWRD must be cleared to enable the LVI module, and LVIRSTD must be set to disable LVI resets.

10.3.2 Forced Reset Operation

In applications that require V_{DD} to remain above the V_{TRIPF} level, enabling LVI resets allows the LVI module to reset the MCU when V_{DD} falls below the V_{TRIPF} level. In the configuration register, LVIPWRD and LVIRSTD must be cleared to enable the LVI module and to enable LVI resets.

10.3.3 LVI Hysteresis

The LVI has hysteresis to maintain a stable operating condition. After the LVI has triggered (by having V_{DD} fall below V_{TRIPF}), the MCU will remain in reset until V_{DD} rises above the rising trip point voltage, V_{TRIPR}. This prevents a condition in which the MCU is continually entering and exiting reset if V_{DD} is approximately equal to V_{TRIPF}. V_{TRIPR} is greater than V_{TRIPF} by the typical hysteresis voltage, V_{HYS}.

10.3.4 LVI Trip Selection

LVITRIP in the configuration register selects the LVI protection range. The default setting out of reset is for the low voltage range. Because LVITRIP is in a write-once configuration register, the protection range cannot be changed after initialization.

NOTE

The MCU is guaranteed to operate at a minimum supply voltage. The trip point (V_{TRIPF}) may be lower than this. See Chapter 17 Electrical Specifications for the actual trip point voltages.

11.8 Registers

The oscillator module contains two registers:

- Oscillator status and control register (OSCSC)
- Oscillator trim register (OSCTRIM)

11.8.1 Oscillator Status and Control Register

The oscillator status and control register (OSCSC) contains the bits for switching between internal and external clock sources. If the application uses an external crystal, bits in this register are used to select the crystal oscillator amplifier necessary for the desired crystal. While running off the internal clock source, the user can use bits in this register to select the internal clock source frequency.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	OSCOPT1	OSCOPT0	ICFS1	ICFS0	ECFS1	ECFS0	ECGON	ECGST
Write:								
Reset:	0	0	1	0	0	0	0	0

= Unimplemented

Figure 11-4. Oscillator Status and Control Register (OSCSC)

OSCOPT1:OSCOPT0 — OSC Option Bits

These read/write bits allow the user to change the clock source for the MCU. The default reset condition has the bus clock being derived from the internal oscillator. See 11.3.2.2 Internal to External Clock Switching for information on changing clock sources.

OSCOPT1	OSCOPT0	Oscillator Modes
0	0	Internal oscillator (frequency selected using ICFSx bits)
0	1	External oscillator clock
1	0	External RC
1	1	External crystal (range selected using ECFSx bits)

ICFS1:ICFS0 — Internal Clock Frequency Select Bits

These read/write bits enable the frequency to be increased for applications requiring a faster bus clock when running off the internal oscillator. The WAIT instruction has no effect on the oscillator logic. BUSCLKX2 and BUSCLKX4 continue to drive to the SIM module.

ICFS1	ICFS0	Internal Clock Frequency
0	0	4.0 MHz
0	1	8.0 MHz
1	0	12.8 MHz — default reset condition
1	1	25.6 MHz

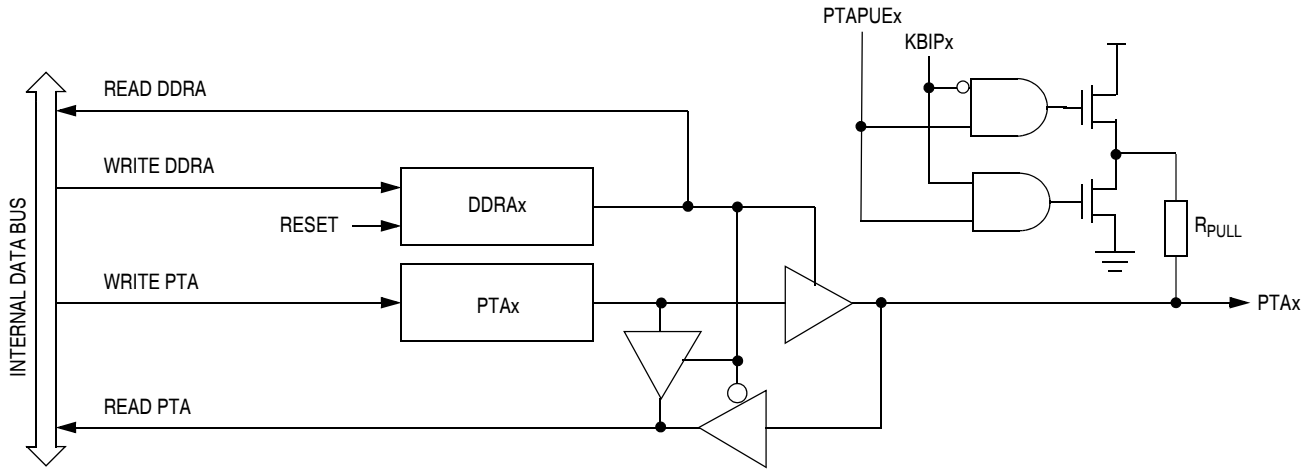


Figure 12-3. Port A I/O Circuit

NOTE

Figure 12-3 does not apply to PTA2

When DDRAx is a 1, reading PTA reads the PTAx data latch. When DDRAx is a 0, reading PTA reads the logic level on the PTAx pin. The data latch can always be written, regardless of the state of its data direction bit.

12.3.3 Port A Input Pullup/Down Enable Register

The port A input pullup/down enable register (PTAPUE) contains a software configurable pullup/down device for each of the port A pins. Each bit is individually configurable and requires the corresponding data direction register, DDRAx, to be configured as input. Each pullup/down device is automatically and dynamically disabled when its corresponding DDRAx bit is configured as output. The pull device polarity is defined by the KBIPR register, see 9.8.3 Keyboard Interrupt Polarity Register (KBIPR).

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	OSC2EN		PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-4. Port A Input Pullup/Down Enable Register (PTAPUE)

OSC2EN — Enable PTA4 on OSC2 Pin

This read/write bit configures the OSC2 pin function when internal oscillator or RC oscillator option is selected. This bit has no effect for the XTAL or external oscillator options.

1 = OSC2 pin outputs the internal or RC oscillator clock (BUSCLKX4)

0 = OSC2 pin configured for PTA4 I/O, having all the interrupt and pullup/down functions

13.4 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{RST}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE–FFFF ($FEFE–FEFF in monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see 13.5 SIM Counter), but an external reset does not. Each of the resets sets a corresponding bit in the SIM reset status register (SRSR). See 13.8 SIM Registers.

13.4.1 External Pin Reset

The $\overline{RST}$ pin circuits include an internal pullup device. Pulling the asynchronous $\overline{RST}$ pin low halts all processing. The PIN bit of the SIM reset status register (SRSR) is set as long as $\overline{RST}$ is held low for at least the minimum t_{RL} time. Figure 13-3 shows the relative timing. The $\overline{RST}$ pin function is only available if the RSTEN bit is set in the CONFIG2 register.

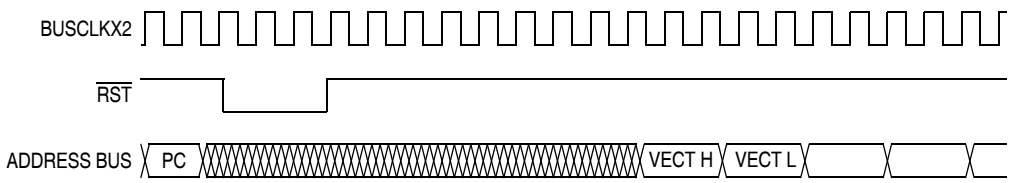


Figure 13-3. External Reset Timing

13.4.2 Active Resets from Internal Sources

The $\overline{RST}$ pin is initially setup as a general-purpose input after a POR. Setting the RSTEN bit in the CONFIG2 register enables the pin for the reset function. This section assumes the RSTEN bit is set when describing activity on the $\overline{RST}$ pin.

NOTE

For POR and LVI resets, the SIM cycles through 4096 BUSCLKX4 cycles. The internal reset signal then follows the sequence from the falling edge of $\overline{RST}$ shown in Figure 13-4.

The COP reset is asynchronous to the bus clock.

The active reset feature allows the part to issue a reset to peripherals and other chips within a system built around the MCU.

All internal reset sources actively pull the $\overline{RST}$ pin low for 32 BUSCLKX4 cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (see Figure 13-4). An internal reset can be caused by an illegal address, illegal opcode, COP time out, LVI, or POR (see Figure 13-5).

13.8 SIM Registers

The SIM has two memory mapped registers.

13.8.1 SIM Reset Status Register

This register contains seven flags that show the source of the last reset. Clear the SIM reset status register by reading it. A power-on reset sets the POR bit and clears all other bits in the register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	POR	PIN	COP	ILOP	ILAD	MODRST	LVI	0
Write:								
POR:	1	0	0	0	0	0	0	0

= Unimplemented

Figure 13-19. SIM Reset Status Register (SRSR)

POR — Power-On Reset Bit

1 = Last reset caused by POR circuit
0 = Read of SRSR

PIN — External Reset Bit

1 = Last reset caused by external reset pin ($\overline{RST}$)
0 = POR or read of SRSR

COP — Computer Operating Properly Reset Bit

1 = Last reset caused by COP counter
0 = POR or read of SRSR

ILOP — Illegal Opcode Reset Bit

1 = Last reset caused by an illegal opcode
0 = POR or read of SRSR

ILAD — Illegal Address Reset Bit (illegal attempt to fetch an opcode from an unimplemented address)

1 = Last reset caused by an opcode fetch from an illegal address
0 = POR or read of SRSR

MODRST — Monitor Mode Entry Module Reset bit

1 = Last reset caused by monitor mode entry when vector locations $FFFE and $FFFF are $FF after POR while IRQB = V_{DD}
0 = POR or read of SRSR

LVI — Low Voltage Inhibit Reset bit

1 = Last reset caused by LVI circuit
0 = POR or read of SRSR

14.8.8 SLIC Identifier and Data Registers

The SLIC identifier (SLCID) and eight data registers (SLCD7–SLCD0) comprise the transmit and receive buffer and are used to read/write the identifier and message buffer 8 data bytes. In BTM mode (BTM = 1), only SLCID is used to send and receive bytes, as only one byte is handled at any one time. The number of bytes to be read from or written to these registers is determined by the user software and written to SLCDLC. To obtain proper data, reads and writes to these registers must be made based on the proper length corresponding to a particular message. It is the responsibility of the user software to keep track of this value to prevent data corruption. For example, it is possible to read data from locations in the message buffer which contain erroneous or old data if the user software reads more data registers than were updated by the incoming message, as indicated in SLCDLC.

NOTE

An incorrect length value written to SLCDLC can result in the user software misreading or miswriting data in the message buffer. An incorrect length value might also result in SLIC error messages. For example, if a 4-byte message is to be received, but the user software incorrectly reports a 3-byte length to the DLC, the SLIC will assume the 4th data byte is actually a checksum value and attempt to validate it as such. If this value doesn't match the calculated value, an incorrect checksum error will occur. If it does happen to match the expected value, then the message would be received as a 3-byte message with valid checksum. Either case is incorrect behavior for the application and can be avoided by ensuring that the correct length code is used for each identifier.

The first data byte received after the LIN identifier in a LIN message frame will be loaded into SLCD0. The next byte (if applicable) will be loaded into SLCD1, and so forth.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-12. SLIC Identifier Register (SLCID)

The SLIC identifier register is used to capture the incoming LIN identifier and when the SLCSV value indicates that the identifier has been received successfully, this register contains the received identifier value. If the incoming identifier contained a parity error, this register value will not contain valid data.

In byte transfer mode (BTM = 1), this register is used for sending and receiving each byte of data. When transmitting bytes, the data is loaded into this register, then TXGO in SLCDLC is set to initiate the transmission. When receiving bytes, they are read from this register only.

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	R7	R6	R5	R4	R3	R2	R1	R0
Write:	T7	T6	T5	T4	T3	T2	T1	T0
Reset:	0	0	0	0	0	0	0	0

Figure 14-13. SLIC Data Register x (SLCD7–SLCD0)

R — Read SLC Receive Data

T — Write SLC Transmit Data

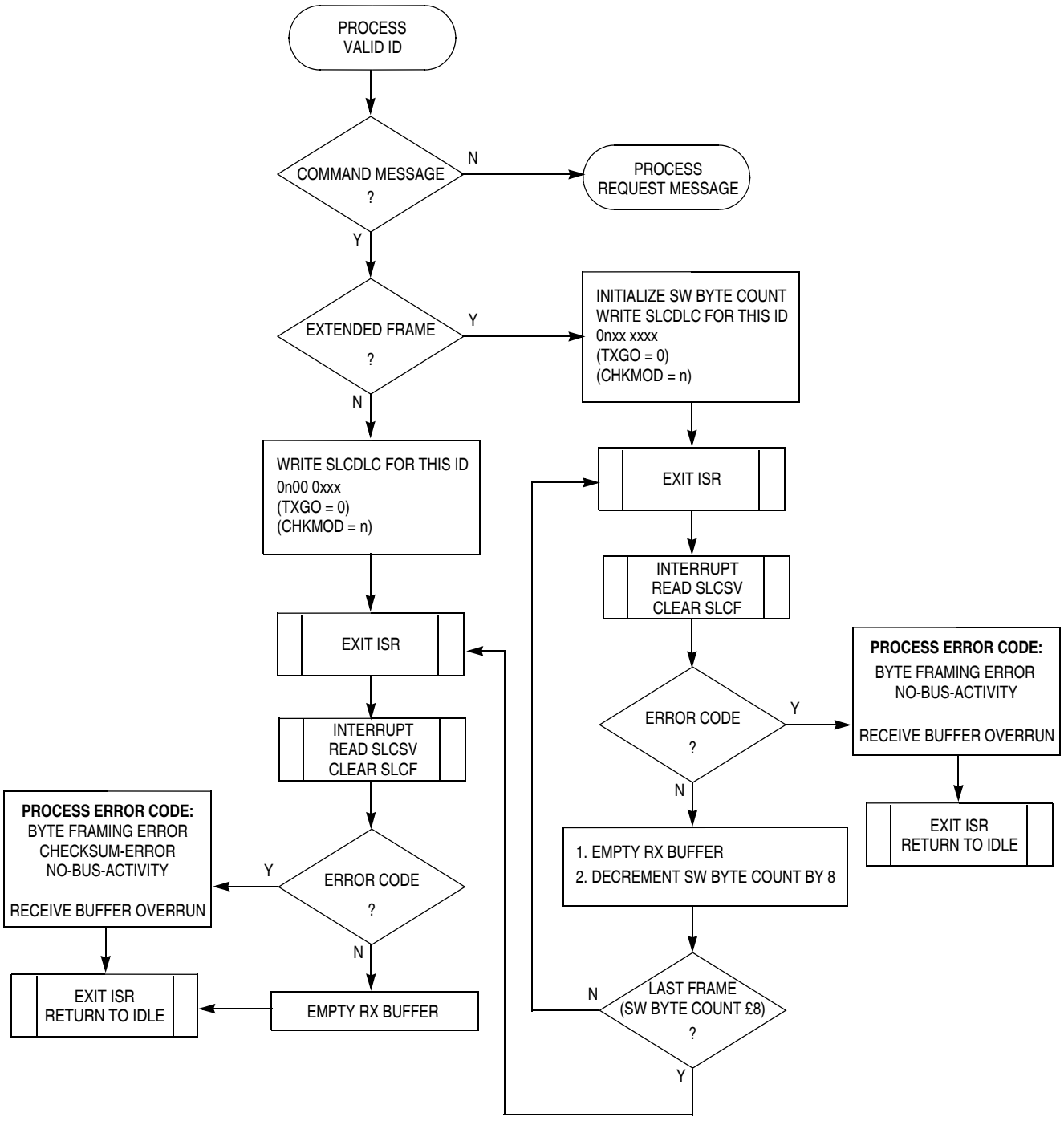


Figure 14-16. Handling Command Messages (Data Receive)

The SLIC transmit go (TXGO) bit should be 0 for command frames, indicating to the SLIC that data is coming from the master. The checksum mode control (CHKMOD) bit allows the user to select which method of checksum calculation is desired for this message frame. The LIN 1.3 checksum does not include the identifier byte in the calculation, while the SAE version does include this byte. Because the identifier is already received by the SLIC by this time, the default is to include it in the calculation. If a LIN 1.3 checksum is desired, a 1 in CHKMOD will reset the checksum circuitry to begin calculating the

14.9.14 High-Speed LIN Operation

High-speed LIN operation does not necessarily require any reconfiguration of the SLIC module, depending upon what maximum LIN bit rate is desired. Several factors affect the performance of the SLIC module at LIN speeds higher than 20 kbps, all of which are functions of the speed of the SLIC clock and the prescaler of the digital filter. The tightest constraint comes from the need to maintain ±1.5% accuracy with the master node timing. This requires that the SLIC module be able to sample the incoming data stream accurately enough to guarantee that accuracy. Table 14-5 shows the maximum LIN bit rates allowable to maintain this accuracy.

Table 14-5. Maximum LIN Bit Rates for High-Speed Operation

SLIC Clock (MHz)	Maximum LIN Bit Rate for ±1% SLIC Accuracy (Bits / Second)	Maximum LIN Bit Rate for ±1.5% SLIC Accuracy (Bits / Second)
8	80,000	120,000
6.4	64,000	96,000
4.8	48,000	72,000
4	40,000	60,000
3.2	32,000	48,000
2.4	24,000	36,000
2	20,000	30,000

The above numbers assume a perfect input waveforms into the SLCRX pin, where 1 and 0 bits are of equal length and are exactly the correct length for the appropriate speed. Factors such as physical layer wave shaping and ground shift can affect the symmetry of these waveforms, causing bits to appear shortened or lengthened as seen by the SLIC module. The user must take these factors into account and base the maximum speed upon the shortest possible bit time that the SLIC module may observe, factoring in all physical layer effects. On some LIN physical layer devices it is possible to turn off wave shaping circuitry for high-speed operation, removing this portion of the physical layer error.

The digital receive filter can also affect high speed operation if it is set too low and begins to filter out valid message traffic. Under ideal conditions, this will not happen, as the digital filter maximum speeds allowable are higher than the speeds allowed for ±1.5% accuracy. If the digital receive filter prescaler is set to divide- by-4; however, the filter delay is very close to the ±1.5% accuracy maximum bit time.

For example, with a SLIC clock of 4 MHz, the SLIC module is capable of maintaining ±1.5% accuracy up to 60,000 bps. If the digital receive filter prescaler is set to divide-by-4, this means that the filter will only pass message traffic which is 62,500 bps or slower under ideal circumstances. This is only a difference of 2,500 bps (4.17% of the nominal valid message traffic speed). In this case, the user must ensure that with all errors accounted for, no bit will appear shorter than 16 μs
(1 bit at 62,500 bps) or the filter will block that bit. This is far too narrow a margin for safe design practices. The better solution would be to reduce the filter prescaler, increasing the gap between the filter cut-off point and the nominal speed of valid message traffic. Changing the prescaler to divide by 2 in this example gives a filter cut-off of 125,000 bps, which is 60,000 bps faster than the nominal speed of the LIN bus and much less likely to interfere with valid message traffic.

To ensure that all valid messages pass the filter stage in high-speed operation, it is best to ensure that the filter cut-off point is at least 2 times the nominal speed of the fastest message traffic to appear on the bus. Refer to Table 14-6 for a more complete list of the digital receive filter delays as they relate to the maximum LIN bus frequency. Table 14-7 repeats much of the data found in Table 14-6; however, the filter

Chapter 16
Development Support

16.1 Introduction

This section describes the break module, the monitor module, and the monitor mode entry methods.

16.2 Break Module (BRK)

The break module can generate a break interrupt that stops normal program flow at a defined address to enter a background program.

Features include:

- Accessible input/output (I/O) registers during the break Interrupt
- Central processor unit (CPU) generated break interrupts
- Software-generated break interrupts
- Computer operating properly (COP) disabling during break interrupts

16.2.1 Functional Description

When the internal address bus matches the value written in the break address registers, the break module issues a breakpoint signal ($\overline{\text{BKPT}}$) to the system integration module (SIM). The SIM then causes the CPU to load the instruction register with a software interrupt instruction (SWI). The program counter vectors to $FFFC and $FFFD ($FEFC and $FEFD in monitor mode).

The following events can cause a break interrupt to occur:

- A CPU generated address (the address in the program counter) matches the contents of the break address registers.
- Software writes a 1 to the BRKA bit in the break status and control register.

When a CPU generated address matches the contents of the break address registers, the break interrupt is generated. A return-from-interrupt instruction (RTI) in the break routine ends the break interrupt and returns the microcontroller unit (MCU) to normal operation.

Figure 16-2 shows the structure of the break module.

16.3.2 Security

A security feature discourages unauthorized reading of FLASH locations while in monitor mode. The host can bypass the security feature at monitor mode entry by sending eight security bytes that match the bytes at locations $FFF6–$FFFD. Locations $FFF6–$FFFD contain user-defined data.

NOTE

Do not leave locations $FFF6–$FFFD blank. For security reasons, program locations $FFF6–$FFFD even if they are not used for vectors.

During monitor mode entry, the MCU waits after the power-on reset for the host to send the eight security bytes on pin PTA0. If the received bytes match those at locations $FFF6–$FFFD, the host bypasses the security feature and can read all FLASH locations and execute code from FLASH. Security remains bypassed until a power-on reset occurs. If the reset was not a power-on reset, security remains bypassed and security code entry is not required. See Figure 16-18.

Upon power-on reset, if the received bytes of the security code do not match the data at locations $FFF6–$FFFD, the host fails to bypass the security feature. The MCU remains in monitor mode, but reading a FLASH location returns an invalid value and trying to execute code from FLASH causes an illegal address reset. After receiving the eight security bytes from the host, the MCU transmits a break character, signifying that it is ready to receive a command.

NOTE

The MCU does not transmit a break character until after the host sends the eight security bytes.

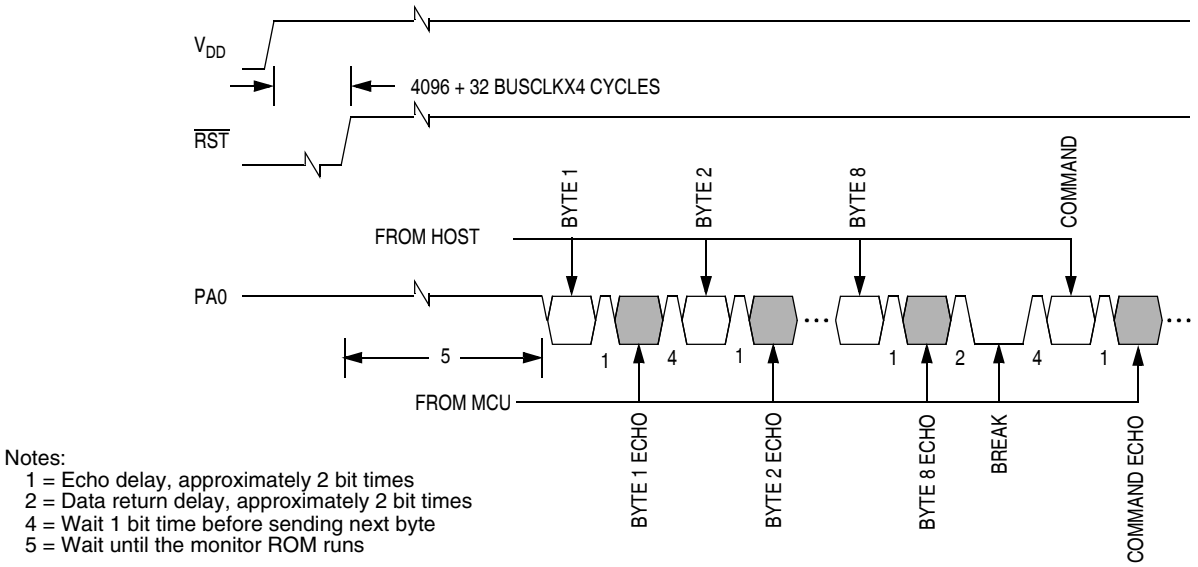


Figure 16-18. Monitor Mode Entry Timing

To determine whether the security code entered is correct, check to see if bit 6 of RAM address $80 is set. If it is, then the correct security code has been entered and FLASH can be accessed.

If the security sequence fails, the device should be reset by a power-on reset and brought up in monitor mode to attempt another entry. After failing the security sequence, the FLASH module can also be mass erased by executing an erase routine that was downloaded into internal RAM. The mass erase operation clears the security code locations so that all eight security bytes become $FF (blank).

17.7 5-V Control Timing

Characteristic[1]	Symbol	Min	Max	Unit
Internal operating frequency	f_{OP} (f_{BUS})	—	8	MHz
Internal clock period ($1/f_{OP}$)	t_{cyc}	125	—	ns
$\overline{RST}$ input pulse width low[2]	t_{RL}	100	—	ns
$\overline{IRQ}$ interrupt pulse width low (edge-triggered)[2]	t_{ILIH}	100	—	ns
$\overline{IRQ}$ interrupt pulse period[2]	t_{ILIL}	Note[3]	—	t_{cyc}

1. V_{DD} = 4.5 to 5.5 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H; timing shown with respect to 20% V_{DD} and 70% V_{SS}, unless otherwise noted.
2. Values are based on characterization results, not tested in production.
3. The minimum period is the number of cycles it takes to execute the interrupt service routine plus 1 t_{cyc}.

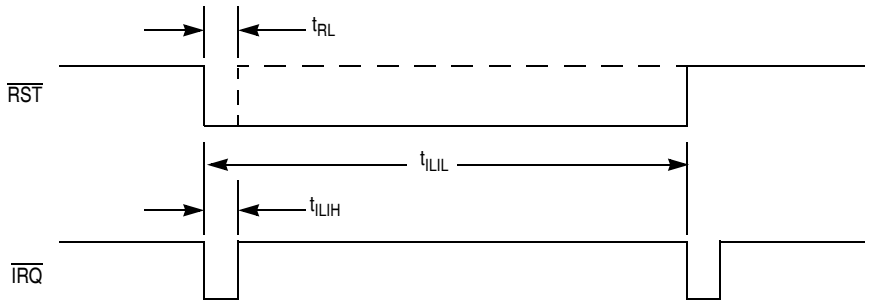


Figure 17-3. $\overline{RST}$ and $\overline{IRQ}$ Timing

17.8 3.3-V DC Electrical Characteristics

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Output high voltage I_{Load} = –0.6 mA, all I/O pins I_{Load} = –4.0 mA, all I/O pins I_{Load} = –10.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OH}	 V_{DD}–0.3 V_{DD}–1.0 V_{DD}–0.8	 — — —	 — — —	V
Maximum combined I_{OH} (all I/O pins)	I_{OHT}	—	—	50	mA
Output low voltage I_{Load} = 0.5 mA, all I/O pins I_{Load} = 6.0 mA, all I/O pins I_{Load} = 10.0 mA, PTA0, PTA1, PTA3–PTA5 only	V_{OL}	 — — —	 — — —	 0.3 1.0 0.8	V
Maximum combined I_{OL} (all I/O pins)	I_{OHL}	—	—	50	mA
Input high voltage PTA0–PTA5, PTB0–PTB7	V_{IH}	0.7 x V_{DD}	—	V_{DD}	V
Input low voltage PTA0–PTA5, PTB0–PTB7	V_{IL}	V_{SS}	—	0.3 x V_{DD}	V

— Continued on next page

Characteristic[1]	Symbol	Min	Typ[2]	Max	Unit
Input hysteresis[3]	V_{HYS}	0.06 x V_{DD}	—	—	V
DC injection current[3] [4] [5] [6] Single pin limit $V_{in} > V_{DD}$ $V_{in} < V_{SS}$ Total MCU limit, includes sum of all stressed pins $V_{in} > V_{DD}$ $V_{in} < V_{SS}$	I_{IC}	 0 0 0 0	 — — — —	 2 –0.2 25 –5	mA
Ports Hi-Z leakage current	I_{IL}	0	—	±1	µA
Capacitance Ports (as input)[3]	C_{IN}	—	—	8	pF
POR rearm voltage	V_{POR}	0.75	—	—	V
POR rise time ramp rate[3][7]	R_{POR}	0.035	—	—	V/ms
Monitor mode entry voltage [3]	V_{TST}	V_{DD} + 2.5	—	V_{DD} + 4.0	V
Pullup resistors[8] PTA0–PTA5, PTB0–PTB7	R_{PU}	16	26	36	kΩ
Pulldown resistors[9] PTA0–PTA5	R_{PD}	16	26	36	kΩ
Low-voltage inhibit reset, trip falling voltage	V_{TRIPF}	2.65	2.8	3.0	V
Low-voltage inhibit reset, trip rising voltage	V_{TRIPR}	2.75	2.9	3.10	V
Low-voltage inhibit reset/recover hysteresis	V_{HYS}	—	100	—	mV

1. V_{DD} = 3.0 to 3.6 Vdc, V_{SS} = 0 Vdc, $T_A = T_L$ to T_H, unless otherwise noted.
2. Typical values reflect average measurements at midpoint of voltage range, 25•C only.
3. This parameter is characterized and not tested on each device.
4. All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.
5. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
6. Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).
7. If minimum V_{DD} is not reached before the internal POR reset is released, the LVI will hold the part in reset until minimum V_{DD} is reached.
8. R_{PU} is measured at V_{DD} = 3.3 V. Pullup resistors only available when PTAPUEx is enabled with KBIPx = 0.
9. R_{PD} is measured at V_{DD} = 3.3 V, Pulldown resistors only available when PTAPUEx is enabled with KBIPx =1.

Characteristic	Symbol	Min	Typ	Max	Unit
External RC oscillator frequency, RCCLK (1)(2) $V_{DD} \geq 3.0$ V $V_{DD} < 3.0$ V	f_{RCCLK}	 2 2	 — —	 10 8.4	MHz
External clock reference frequencyy(1)(4)(5) $V_{DD} \geq 4.5$V $V_{DD} \geq 3.0$V $V_{DD} < 3.0$V	$f_{OSCXCLK}$	 dc dc dc	— — — —	 32 16 8.4	MHz
RC oscillator external resistor V_{DD} = 5 V V_{DD} = 3 V	R_{EXT}	See Figure 17-7 See Figure 17-8			—
Crystal frequency, XTALCLK(1)(6)(7) ECFS1:ECFS0 = 00 ($V_{DD} \geq 4.5$ V) ECFS1:ECFS0 = 00 (not allowed if $V_{DD} < 3.0$V) ECFS1:ECFS0 = 01 ECFS1:ECFS0 = 10	$f_{OSCXCLK}$	 8 8 1 30	 — — — —	 32 16 8 100	 MHz MHz MHz kHz
ECFS1:ECFS0 = 00 (8) Feedback bias resistor Crystal load capacitance(9) Crystal capacitors(9)	 R_B C_L C_1,C_2	 — — —	 1 20 (2 x C_L) – 5pF	 — — —	 MΩ pF pF
ECFS1:ECFS0 = 01(8) Crystal series damping resistor $f_{OSCXCLK}$ = 1 MHz $f_{OSCXCLK}$ = 4 MHz $f_{OSCXCLK}$ = 8 MHz Feedback bias resistor Crystal load capacitance(9) Crystal capacitors(9)	 R_S R_B C_L C_1,C_2	 — — — — — —	 20 10 0 5 18 (2 x C_L) –10 pF	 — — — — — —	 kΩ kΩ kΩ MΩ pF pF
AWU Module: Internal RC oscillator frequency	f_{INTRC}	—	32	—	kHz

1. Bus frequency, f_{OP}, is oscillator frequency divided by 4.
2. Deviation values assumes trimming @25•C and midpoint of voltage range, for example 5.0 V for 5 V ± 10%, 3.3 V for 3.3 V ± 10%.
3. Values are based on characterization results, not tested in production.
4. No more than 10% duty cycle deviation from 50%.
5. When external oscillator clock is greater than 1MHz, ECFS1:ECFS0 must be 00 or 01
6. Use fundamental mode only, do **not** use overtone crystals or overtone ceramic resonators
7. Due to variations in electrical properties of external components such as, ESR and Load Capacitance, operation above 16 MHz is not guaranteed for all crystals or ceramic resonators. Operation above 16 MHz requires that a Negative Resistance Margin (NRM) characterization and component optimization be performed by the crystal or ceramic resonator vendor for every different type of crystal or ceramic resonator which will be used. This characterization and optimization must be performed at the extremes of voltage and temperature which will be applied to the microcontroller in the application. The NRM must meet or exceed 10x the maximum ESR of the crystal or ceramic resonator for acceptable performance.
8. Do not use damping resistor when ECFS1:ECFS0 = 00, 10 or 11
9. Consult crystal vendor data sheet.

Chapter 18
Ordering Information and Mechanical Specifications

18.1 Introduction

This section provides ordering information for the MC68HC908QL4 along with the dimensions for:

- 16-pin small outline integrated circuit (SOIC) package
- 16-pin thin shrink small outline package (TSSOP)

18.2 MC Order Numbers

Table 18-1. MC Order Numbers

MC Order Number	ADC	FLASH Memory	Package
MC908QL4	Yes	4096 bytes	16-pins SOIC, and TSSOP

Temperature and package designators:
C = −40•C to +85•C
V = −40•C to +105•C
M = −40•C to +125•C
DW = Small outline integrated circuit package (SOIC)
DT = Thin shrink small outline package (TSSOP)

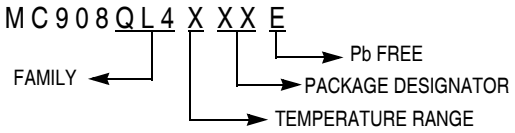
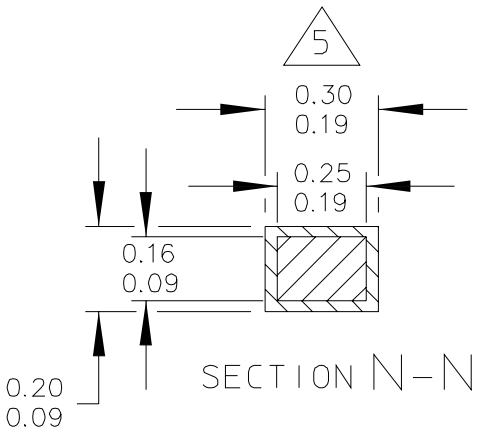
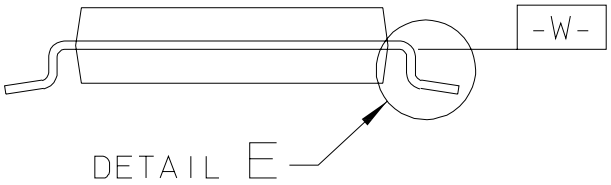


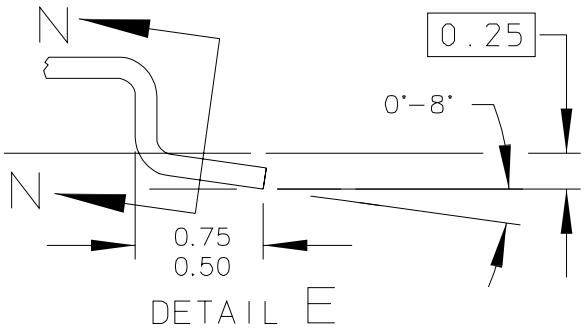
Figure 18-1. Device Numbering System

18.3 Package Dimensions

Refer to the following pages for detailed package dimensions.







MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ASH70247A	REV: B
16 LD TSSOP, PITCH 0.65MM	CASE NUMBER: 948F-01	19 MAY 2005
	STANDARD: JEDEC	