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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	83
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l433vct6tr">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l433vct6tr</a>

## 5 Power control (PWR)

### 5.1 Power supplies

The STM32L43xxx/44xxx/45xxx/46xxx devices require a 1.71 V to 3.6 V operating supply voltage ( $V_{DD}$ ). Several peripherals are supplied through independent power domains:  $V_{DDA}$ ,  $V_{DDUSB}$ ,  $V_{LCD}$ . Those supplies must not be provided without a valid operating supply on the  $V_{DD}$  pin.

- $V_{DD} = 1.71 \text{ V to } 3.6 \text{ V}$   
 $V_{DD}$  is the external power supply for the I/Os, the internal regulator and the system analog such as reset, power management and internal clocks. It is provided externally through VDD pins.
- $V_{DD12} = 1.05 \text{ V to } 1.32 \text{ V}$   
 External power supply, connected to  $V_{CORE}$ , bypassing internal regulator when connected to an external SMPS. It is provided externally through VDD12 pins and only available on packages with the external SMPS supply option.
- $V_{DDA} = 1.62 \text{ V (ADCs/COMP)} / 1.8 \text{ V (DACs/OPAMP)} / 2.4 \text{ V (VREFBUF)}$  to 3.6 V  
 $V_{DDA}$  is the external analog power supply for A/D converters, D/A converters, voltage reference buffer, operational amplifiers and comparators. The  $V_{DDA}$  voltage level is independent from the  $V_{DD}$  voltage.  $V_{DDA}$  should be preferably connected to  $V_{DD}$  when these peripherals are not used.
- $V_{DDUSB} = 3.0 \text{ V to } 3.6 \text{ V}$  (available on STM32L4x2xx and STM32L4x3xx devices only)  
 $V_{DDUSB}$  is the external independent power supply for USB transceivers. The  $V_{DDUSB}$  voltage level is independent from the  $V_{DD}$  voltage.  $V_{DDUSB}$  should be preferably connected to  $V_{DD}$  when the USB is not used.  
 On small packages,  $V_{DDUSB}$  power supply may not be present as a dedicated pin and is internally bonded to  $V_{DD}$ . For such devices,  $V_{DD}$  has to respect the  $V_{DDUSB}$  supply range when USB is used.
- $V_{LCD} = 2.5 \text{ V to } 3.6 \text{ V}$  (available on STM32L4x3xx devices only)  
 The LCD controller can be powered either externally through VLCD pin, or internally from an internal voltage generated by the embedded step-up converter. VLCD is multiplexed with PC3 which can be used as GPIO when the LCD is not used.  
 On small packages,  $V_{DDUSB}$  power supply may not be present as a dedicated pin, but is internally bonded to VDD. For such devices, VDD has to respect the VDDUSB supply range when USB is used.
- $V_{BAT} = 1.55 \text{ V to } 3.6 \text{ V}$   
 $V_{BAT}$  is the power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when  $V_{DD}$  is not present. VBAT is internally bonded to VDD for small packages without dedicated pin.  
 $V_{BAT}$  is internally bonded to  $V_{DD}$  for small packages without dedicated pin.
- $V_{REF-}$ ,  $V_{REF+}$   
 $V_{REF+}$  is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.  
 When  $V_{DDA} < 2 \text{ V}$ ,  $V_{REF+}$  must be equal to  $V_{DDA}$ .

### External crystal/ceramic resonator (HSE crystal)

The 4 to 48 MHz external oscillator has the advantage of producing a very accurate rate on the main clock.

The associated hardware configuration is shown in [Figure 14](#). Refer to the electrical characteristics section of the *datasheet* for more details.

The HSERDY flag in the [Clock control register \(RCC\\_CR\)](#) indicates if the HSE oscillator is stable or not. At startup, the clock is not released until this bit is set by hardware. An interrupt can be generated if enabled in the [Clock interrupt enable register \(RCC\\_CIER\)](#).

The HSE Crystal can be switched on and off using the HSEON bit in the [Clock control register \(RCC\\_CR\)](#).

### External source (HSE bypass)

In this mode, an external clock source must be provided. It can have a frequency of up to 48 MHz. You select this mode by setting the HSEBYP and HSEON bits in the [Clock control register \(RCC\\_CR\)](#). The external clock signal (square, sinus or triangle) with ~40-60 % duty cycle depending on the frequency (refer to the *datasheet*) has to drive the following pin (see [Figure 14](#)).

- On devices where OSC\_IN and OSC\_OUT pins are available: OSC\_IN pin must be driven while the OSC\_OUT pin can be used as a GPIO.
- Otherwise, the CK\_IN pin must be driven.

*Note:* For details on pin availability, refers to the pinout section in the corresponding device *datasheet*.

To minimize the consumption, it is recommended to use the square signal.

## 6.2.2 HSI16 clock

The HSI16 clock signal is generated from an internal 16 MHz RC Oscillator.

The HSI16 RC oscillator has the advantage of providing a clock source at low cost (no external components). It also has a faster startup time than the HSE crystal oscillator however, even with calibration the frequency is less accurate than an external crystal oscillator or ceramic resonator.

The HSI16 clock can be selected as system clock after wakeup from Stop modes (Stop 0, Stop 1 or Stop 2). Refer to [Section 6.3: Low-power modes](#). It can also be used as a backup clock source (auxiliary clock) if the HSE crystal oscillator fails. Refer to [Section 6.2.10: Clock security system \(CSS\)](#).

### Calibration

RC oscillator frequencies can vary from one chip to another due to manufacturing process variations, this is why each device is factory calibrated by ST for 1 % accuracy at  $T_A=25^{\circ}\text{C}$ .

After reset, the factory calibration value is loaded in the HSICAL[7:0] bits in the [Internal clock sources calibration register \(RCC\\_ICSCR\)](#).

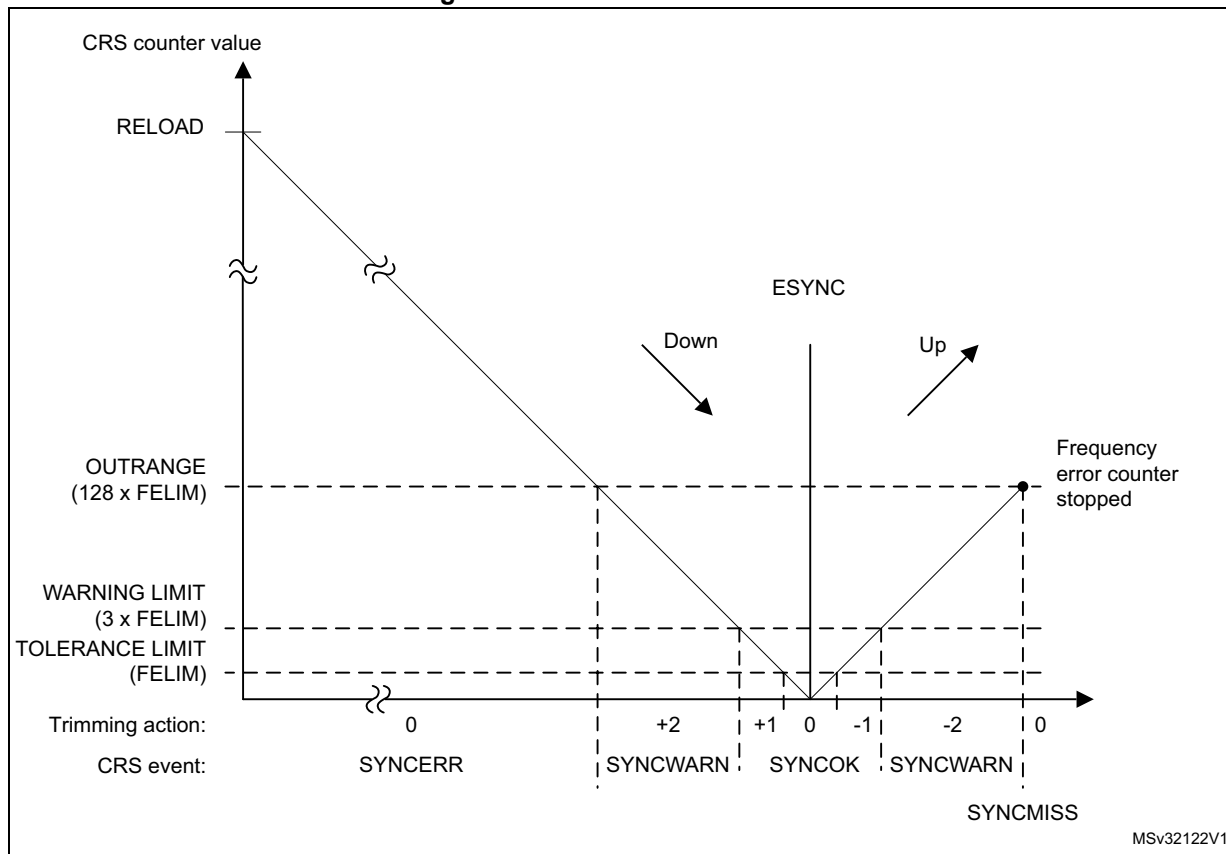
If the application is subject to voltage or temperature variations this may affect the RC oscillator speed. You can trim the HSI16 frequency in the application using the HSITRIM[4:0] bits in the [Internal clock sources calibration register \(RCC\\_ICSCR\)](#).

### 7.3.3 Frequency error measurement

The frequency error counter is a 16-bit down/up counter which is reloaded with the RELOAD value on each SYNC event. It starts counting down till it reaches the zero value, where the ESYNC (expected synchronization) event is generated. Then it starts counting up to the OUTRANGE limit where it eventually stops (if no SYNC event is received) and generates a SYNCMISS event. The OUTRANGE limit is defined as the frequency error limit (FELIM field of the CRS\_CFGR register) multiplied by 128.

When the SYNC event is detected, the actual value of the frequency error counter and its counting direction are stored in the FECAP (frequency error capture) field and in the FEDIR (frequency error direction) bit of the CRS\_ISR register. When the SYNC event is detected during the downcounting phase (before reaching the zero value), it means that the actual frequency is lower than the target (and so, that the TRIM value should be incremented), while when it is detected during the upcounting phase it means that the actual frequency is higher (and that the TRIM value should be decremented).

Figure 18. CRS counter behavior



### 7.3.4 Frequency error evaluation and automatic trimming

The measured frequency error is evaluated by comparing its value with a set of limits:

- TOLERANCE LIMIT, given directly in the FELIM field of the CRS\_CFGR register
- WARNING LIMIT, defined as 3 \* FELIM value
- OUTRANGE (error limit), defined as 128 \* FELIM value

The result of this comparison is used to generate the status indication and also to control the automatic trimming which is enabled by setting the AUTOTRIMEN bit in the CRS\_CR register:

- When the frequency error is below the tolerance limit, it means that the actual trimming value in the TRIM field is the optimal one and that then, no trimming action is necessary.
  - SYNCOK status indicated
  - TRIM value not changed in AUTOTRIM mode
- When the frequency error is below the warning limit but above or equal to the tolerance limit, it means that some trimming action is necessary but that adjustment by one trimming step is enough to reach the optimal TRIM value.
  - SYNCOK status indicated
  - TRIM value adjusted by one trimming step in AUTOTRIM mode
- When the frequency error is above or equal to the warning limit but below the error limit, it means that a stronger trimming action is necessary, and there is a risk that the optimal TRIM value will not be reached for the next period.
  - SYNCWARN status indicated
  - TRIM value adjusted by two trimming steps in AUTOTRIM mode
- When the frequency error is above or equal to the error limit, it means that the frequency is out of the trimming range. This can also happen when the SYNC input is not clean or when some SYNC pulse is missing (for example when one USB SOF is corrupted).
  - SYNCERR or SYNCMISS status indicated
  - TRIM value not changed in AUTOTRIM mode

*Note: If the actual value of the TRIM field is so close to its limits that the automatic trimming would force it to overflow or underflow, then the TRIM value is set just to the limit and the TRIMOVF status is indicated.*

*In AUTOTRIM mode (AUTOTRIMEN bit set in the CRS\_CR register), the TRIM field of CRS\_CR is adjusted by hardware and is read-only.*

### 7.3.5 CRS initialization and configuration

#### RELOAD value

The RELOAD value should be selected according to the ratio between the target frequency and the frequency of the synchronization source after prescaling. It is then decreased by one in order to reach the expected synchronization on the zero value. The formula is the following:

$$\text{RELOAD} = (f_{\text{TARGET}} / f_{\text{SYNC}}) - 1$$

The reset value of the RELOAD field corresponds to a target frequency of 48 MHz and a synchronization signal frequency of 1 kHz (SOF signal from USB).

## 11.5.2 DMA interrupt flag clear register (DMA\_IFCR)

Address offset: 0x04

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	CTEIF7	CHTIF7	CTCIF7	CGIF7	CTEIF6	CHTIF6	CTCIF6	CGIF6	CTEIF5	CHTIF5	CTCIF5	CGIF5
				w	w	w	w	w	w	w	w	w	w	w	w
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTEIF4	CHTIF4	CTCIF4	CGIF4	CTEIF3	CHTIF3	CTCIF3	CGIF3	CTEIF2	CHTIF2	CTCIF2	CGIF2	CTEIF1	CHTIF1	CTCIF1	CGIF1
w	w	w	w	w	w	w	w	w	w	w	w	w	w	w	w

Bits 31:28 Reserved, must be kept at reset value.

Bits 27, 23, 19, 15, **CTEIFx**: Channel x transfer error clear (x = 1..7)

11, 7, 3 This bit is set by software.

0: No effect

1: Clears the corresponding TEIF flag in the DMA\_ISR register

Bits 26, 22, 18, 14, **CHTIFx**: Channel x half transfer clear (x = 1..7)

10, 6, 2 This bit is set by software.

0: No effect

1: Clears the corresponding HTIF flag in the DMA\_ISR register

Bits 25, 21, 17, 13, **CTCIFx**: Channel x transfer complete clear (x = 1..7)

9, 5, 1 This bit is set by software.

0: No effect

1: Clears the corresponding TCIF flag in the DMA\_ISR register

Bits 24, 20, 16, 12, **CGIFx**: Channel x global interrupt clear (x = 1..7)

8, 4, 0 This bit is set by software.

0: No effect

1: Clears the GIF, TEIF, HTIF and TCIF flags in the DMA\_ISR register

### 11.5.7 DMA1 channel selection register (DMA1\_CSELR)

Address offset: 0xA8 (with respect to DMA1 base address)

Reset value: 0x0000 0000

This register is used to manage the mapping of DMA channels (see [Figure 26](#)).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	C7S [3:0]				C6S [3:0]				C5S [3:0]			
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C4S [3:0]				C3S [3:0]				C2S [3:0]				C1S [3:0]			
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 31:28 Reserved, must be kept at reset value.

Bits 27:24 **C7S[3:0]**: DMA channel 7 selection

0000: Reserved  
 0001: Reserved  
 0010: Channel 7 mapped on USART2\_TX  
 0011: Channel 7 mapped on I2C1\_RX  
 0100: Channel 7 mapped on TIM2\_CH2/TIM2\_CH4  
 0101: Reserved  
 0110: Reserved  
 0111: Channel 7 mapped on TIM1\_CH3

Bits 23:20 **C6S[3:0]**: DMA channel 6 selection

0000: Reserved  
 0001: Reserved  
 0010: Channel 6 mapped on USART2\_RX  
 0011: Channel 6 mapped on I2C1\_TX  
 0100: Channel 6 mapped on TIM16\_CH1/TIM16\_UP  
 0101: Channel 6 mapped on TIM3\_CH1/TIM3\_TRIG. Available on STM32L45xxx and STM32L46xxx devices only.  
 0110: Reserved  
 0111: Channel 6 mapped on TIM1\_UP  
 others: Reserved

Bits 19:16 **C5S[3:0]**: DMA channel 5 selection

0000: Reserved  
 0001: Channel 5 mapped on SPI2\_TX  
 0010: Channel 5 mapped on USART1\_RX  
 0011: Channel 5 mapped on I2C2\_RX  
 0100: Channel 5 mapped on TIM2\_CH1  
 0101: Channel 5 mapped on QUADSPI  
 0110: Reserved  
 0111: Channel 5 mapped on TIM15\_CH1/TIM15\_UP/TIM15\_TRIG/TIM15\_COM  
 others: Reserved

The QUADSPI IP is configured using the QUADSPI\_CR. The user shall configure the clock prescaler division factor and the sample shifting settings for the incoming data.

DDR mode can be set through the DDRM bit. Once enabled, the address and the alternate bytes are sent on both clock edges and the data are sent/received on both clock edges. Regardless of the DDRM bit setting, instructions are always sent in SDR mode.

The DMA requests are enabled setting the DMAEN bit. In case of interrupt usage, their respective enable bit can be also set during this phase.

FIFO level for either DMA request generation or interrupt generation is programmed in the FTHRES bits.

If timeout counter is needed, the TCEN bit can be set and the timeout value programmed in the QUADSPI\_LPTR register.

Dual-flash mode can be activated by setting DFM to 1.

### QUADSPI Flash memory configuration

The parameters related to the targeted external Flash memory are configured through the QUADSPI\_DCR register. The user shall program the Flash memory size in the FSIZE bits, the Chip Select minimum high time in the CSHT bits, and the functional mode (Mode 0 or Mode 3) in the MODE bit.

## 15.3.11 QUADSPI usage

The operating mode is selected using FMODE[1:0] (QUADSPI\_CCR[27:26]).

### Indirect mode procedure

When FMODE is programmed to 00, indirect write mode is selected and data can be sent to the Flash memory. With FMODE = 01, indirect read mode is selected where data can be read from the Flash memory.

When the QUADSPI is used in indirect mode, the frames are constructed in the following way:

1. Specify a number of data bytes to read or write in the QUADSPI\_DLR.
2. Specify the frame format, mode and instruction code in the QUADSPI\_CCR.
3. Specify optional alternate byte to be sent right after the address phase in the QUADSPI\_ABR.
4. Specify the operating mode in the QUADSPI\_CR. If FMODE = 00 (indirect write mode) and DMAEN = 1, then QUADSPI\_AR should be specified before QUADSPI\_CR, because otherwise QUADSPI\_DR might be written by the DMA before QUADSPI\_AR is updated (if the DMA controller has already been enabled)
5. Specify the targeted address in the QUADSPI\_AR.
6. Read/Write the data from/to the FIFO through the QUADSPI\_DR.



### 15.3.14 QUADSPI busy bit and abort functionality

Once the QUADSPI starts an operation with the Flash memory, the BUSY bit is automatically set in the QUADSPI\_SR.

In indirect mode, the BUSY bit is reset once the QUADSPI has completed the requested command sequence and the FIFO is empty.

In automatic-polling mode, BUSY goes low only after the last periodic access is complete, due to a match when APMS = 1, or due to an abort.

After the first access in memory-mapped mode, BUSY goes low only on a timeout event or on an abort.

Any operation can be aborted by setting the ABORT bit in the QUADSPI\_CR. Once the abort is completed, the BUSY bit and the ABORT bit are automatically reset, and the FIFO is flushed.

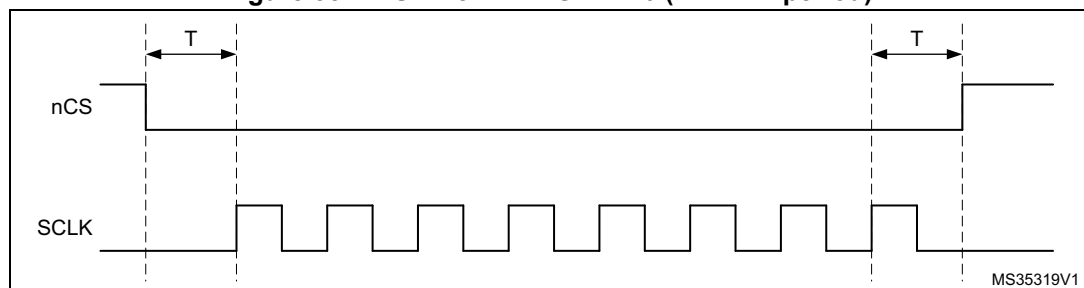
*Note:* Some Flash memories might misbehave if a write operation to a status registers is aborted.

### 15.3.15 nCS behavior

By default, nCS is high, deselecting the external Flash memory. nCS falls before an operation begins and rises as soon as it finishes.

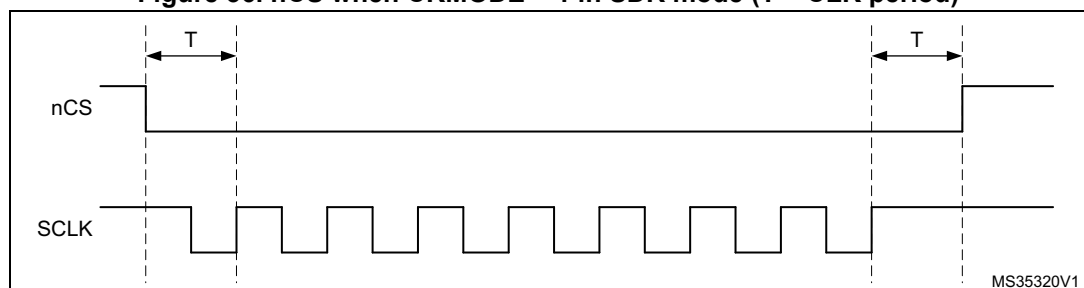
When CKMODE = 0 ("mode0", where CLK stays low when no operation is in progress) nCS falls one CLK cycle before an operation first rising CLK edge, and nCS rises one CLK cycle after the operation final rising CLK edge, as shown in [Figure 35](#).

**Figure 35. nCS when CKMODE = 0 (T = CLK period)**



When CKMODE=1 ("mode3", where CLK goes high when no operation is in progress) and DDRM=0 (SDR mode), nCS still falls one CLK cycle before an operation first rising CLK edge, and nCS rises one CLK cycle after the operation final rising CLK edge, as shown in [Figure 36](#).

**Figure 36. nCS when CKMODE = 1 in SDR mode (T = CLK period)**



### 16.6.14 ADC regular sequence register 4 (ADC\_SQR4)

Address offset: 0x3C

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	SQ16[4:0]					Res.	SQ15[4:0]				
					rw	rw	rw	rw	rw		rw	rw	rw	rw	rw

Bits 31:11 Reserved, must be kept at reset value.

Bits 10:6 **SQ16[4:0]**: 16th conversion in regular sequence

These bits are written by software with the channel number (0..18) assigned as the 16th in the regular conversion sequence.

*Note: Software is allowed to write these bits only when ADSTART=0 (which ensures that no regular conversion is ongoing).*

Bit 5 Reserved, must be kept at reset value.

Bits 4:0 **SQ15[4:0]**: 15th conversion in regular sequence

These bits are written by software with the channel number (0..18) assigned as the 15th in the regular conversion sequence.

*Note: Software is allowed to write these bits only when ADSTART=0 (which ensures that no regular conversion is ongoing).*

### 16.6.15 ADC regular Data Register (ADC\_DR)

Address offset: 0x40

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDATA[15:0]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:0 **RDATA[15:0]**: Regular Data converted

These bits are read-only. They contain the conversion result from the last converted regular channel. The data are left- or right-aligned as described in [Section 16.4.26: Data management](#).

Bits 31:29 **FORD[2:0]**: Sinc filter order

0: FastSinc filter type

1: Sinc<sup>1</sup> filter type

2: Sinc<sup>2</sup> filter type

3: Sinc<sup>3</sup> filter type

4: Sinc<sup>4</sup> filter type

5: Sinc<sup>5</sup> filter type

6-7: Reserved

Sinc<sup>x</sup> filter type transfer function:

$$H(z) = \left( \frac{1 - z^{-FOSR}}{1 - z^{-1}} \right)^x$$

FastSinc filter type transfer function: 
$$H(z) = \left( \frac{1 - z^{-FOSR}}{1 - z^{-1}} \right)^2 \cdot (1 + z^{-(2 \cdot FOSR)})$$

This bit can only be modified when DFEN=0 (DFSDM\_FLTxCR1).

Bits 28:26 Reserved, must be kept at reset value.

Bits 25:16 **FOSR[9:0]**: Sinc filter oversampling ratio (decimation rate)

0 - 1023: Defines the length of the Sinc type filter in the range 1 - 1024 ( $F_{OSR} = FOSR[9:0] + 1$ ). This number is also the decimation ratio of the output data rate from filter.

This bit can only be modified when DFEN=0 (DFSDM\_FLTxCR1)

*Note: If FOSR = 0, then the filter has no effect (filter bypass).*

Bits 15:8 Reserved, must be kept at reset value.

Bits 7:0 **IOSR[7:0]**: Integrator oversampling ratio (averaging length)

0 - 255: The length of the Integrator in the range 1 - 256 ( $IOSR + 1$ ). Defines how many samples from Sinc filter will be summed into one output data sample from the integrator. The output data rate from the integrator will be decreased by this number (additional data decimation ratio).

This bit can only be modified when DFEN=0 (DFSDM\_FLTxCR1)

*Note: If IOSR = 0, then the Integrator has no effect (Integrator bypass).*

### 21.8.7 DFSDM data register for injected group (DFSDM\_FLTxJDATAR)

Address offset:  $0x118 + 0x80 \cdot x$ ,  $x = 0 \dots 1$

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
JDATA[23:8]															
r	r	r	r	r	r	r	r	r	r	r	r	r	r	r	r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
JDATA[7:0]								Res.	Res.	Res.	Res.	Res.	Res.	JDATA[1:0]	
r	r	r	r	r	r	r	r							r	r

Table 98. DFSDM register map and reset values (continued)

Offset	Register	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0x24	DFSDM_CH1CFGR2	OFFSET[23:0]																									DTRBS[4:0]				Res	Res		
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
0x28	DFSDM_CH1AWSRDR	Res	Res	Res	Res	Res	Res	Res	Res	AWFORD[1:0]		Res	AWFOSR[4:0]				BKSCD[3:0]			Res	Res	Res	Res	SCDT[7:0]										
	reset value										0	0		0	0	0	0	0	0	0	0					0	0	0	0	0	0	0	0	0
0x2C	DFSDM_CH1WDATR	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	WDATA[15:0]																					
	reset value																	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x30	DFSDM_CH1DATINR	INDAT1[15:0]															INDAT0[15:0]																	
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x34 - 0x3C	Reserved	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
0x40	DFSDM_CH2CFGR1	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	DATPACK[1:0]		DATMPX[1:0]		Res	Res	Res	Res	CHINSEL	CHEN	CKABEN	SCDEN	SPICKSEL[1:0]		SITP[1:0]		
	reset value																	0	0	0	0					0	0	0	0	0	0	0	0	0
0x44	DFSDM_CH2CFGR2	OFFSET[23:0]																									DTRBS[4:0]				Res	Res	Res	
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				
0x48	DFSDM_CH2AWSRDR	Res	Res	Res	Res	Res	Res	Res	Res	AWFORD[1:0]		Res	AWFOSR[4:0]				BKSCD[3:0]			Res	Res	Res	Res	SCDT[7:0]										
	reset value										0	0		0	0	0	0	0	0	0						0	0	0	0	0	0	0	0	0
0x4C	DFSDM_CH2WDATR	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	WDATA[15:0]																					
	reset value																		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x50	DFSDM_CH2DATINR	INDAT1[15:0]															INDAT0[15:0]																	
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0x54 - 0x5C	Reserved	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res
0x60	DFSDM_CH3CFGR1	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	Res	DATPACK[1:0]		DATMPX[1:0]		Res	Res	Res	Res	CHINSEL	CHEN	CKABEN	SCDEN	SPICKSEL[1:0]		SITP[1:0]		
	reset value																	0	0	0	0					0	0	0	0	0	0	0	0	0
0x64	DFSDM_CH3CFGR2	OFFSET[23:0]																									DTRBS[4:0]				Res	Res	Res	
	reset value	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0				

Table 101. Remapping capability (continued)

Configuration bits		SEG x COM	Output pin	Function
DUTY	MUX_SEG			
1/3	0	44x3	COM3	not used
			COM[2:0]	COM[2:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	SEG[43:40]
			SEG[39:0]	SEG[39:0]
	1	40x3	COM3	not used
			COM[2:0]	COM[2:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	SEG[31:28]
			SEG[39:32]	SEG[39:32]
			SEG[31:28]	not used
			SEG[27:0]	SEG[27:0]
	0	28x3	COM3	not used
			COM[2:0]	COM[2:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	not used
			SEG[31:0]	SEG[31:0]
	1	32x3	COM3	not used
			COM[2:0]	COM[2:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	SEG[31:28]
			SEG[27:0]	SEG[27:0]
1/2	0	44x2	COM[3:2]	not used
			COM[1:0]	COM[1:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	SEG[43:40]
			SEG[39:0]	SEG[39:0]
	1	40x2	COM[3:2]	not used
			COM[1:0]	COM[1:0]
			SEG[43:40]/SEG[31:28]/COM[7:4]	SEG[31:28]
			SEG[39:32]	SEG[39:32]
			SEG[31:28]	not used
			SEG[27:0]	SEG[27:0]

Bit 10 **WUTF**: Wakeup timer flag

This flag is set by hardware when the wakeup auto-reload counter reaches 0.

This flag is cleared by software by writing 0.

This flag must be cleared by software at least 1.5 RTCCLK periods before WUTF is set to 1 again.

Bit 9 **ALRBF**: Alarm B flag

This flag is set by hardware when the time/date registers (RTC\_TR and RTC\_DR) match the Alarm B register (RTC\_ALRMBR).

This flag is cleared by software by writing 0.

Bit 8 **ALRAF**: Alarm A flag

This flag is set by hardware when the time/date registers (RTC\_TR and RTC\_DR) match the Alarm A register (RTC\_ALRMAR).

This flag is cleared by software by writing 0.

Bit 7 **INIT**: Initialization mode

0: Free running mode

1: Initialization mode used to program time and date register (RTC\_TR and RTC\_DR), and prescaler register (RTC\_PRER). Counters are stopped and start counting from the new value when INIT is reset.

Bit 6 **INITF**: Initialization flag

When this bit is set to 1, the RTC is in initialization state, and the time, date and prescaler registers can be updated.

0: Calendar registers update is not allowed

1: Calendar registers update is allowed

Bit 5 **RSF**: Registers synchronization flag

This bit is set by hardware each time the calendar registers are copied into the shadow registers (RTC\_SSRx, RTC\_TRx and RTC\_DRx). This bit is cleared by hardware in initialization mode, while a shift operation is pending (SHPF=1), or when in bypass shadow register mode (BYPSHAD=1). This bit can also be cleared by software.

It is cleared either by software or by hardware in initialization mode.

0: Calendar shadow registers not yet synchronized

1: Calendar shadow registers synchronized

Bit 4 **INITS**: Initialization status flag

This bit is set by hardware when the calendar year field is different from 0 (Backup domain reset state).

0: Calendar has not been initialized

1: Calendar has been initialized

Bit 3 **SHPF**: Shift operation pending

0: No shift operation is pending

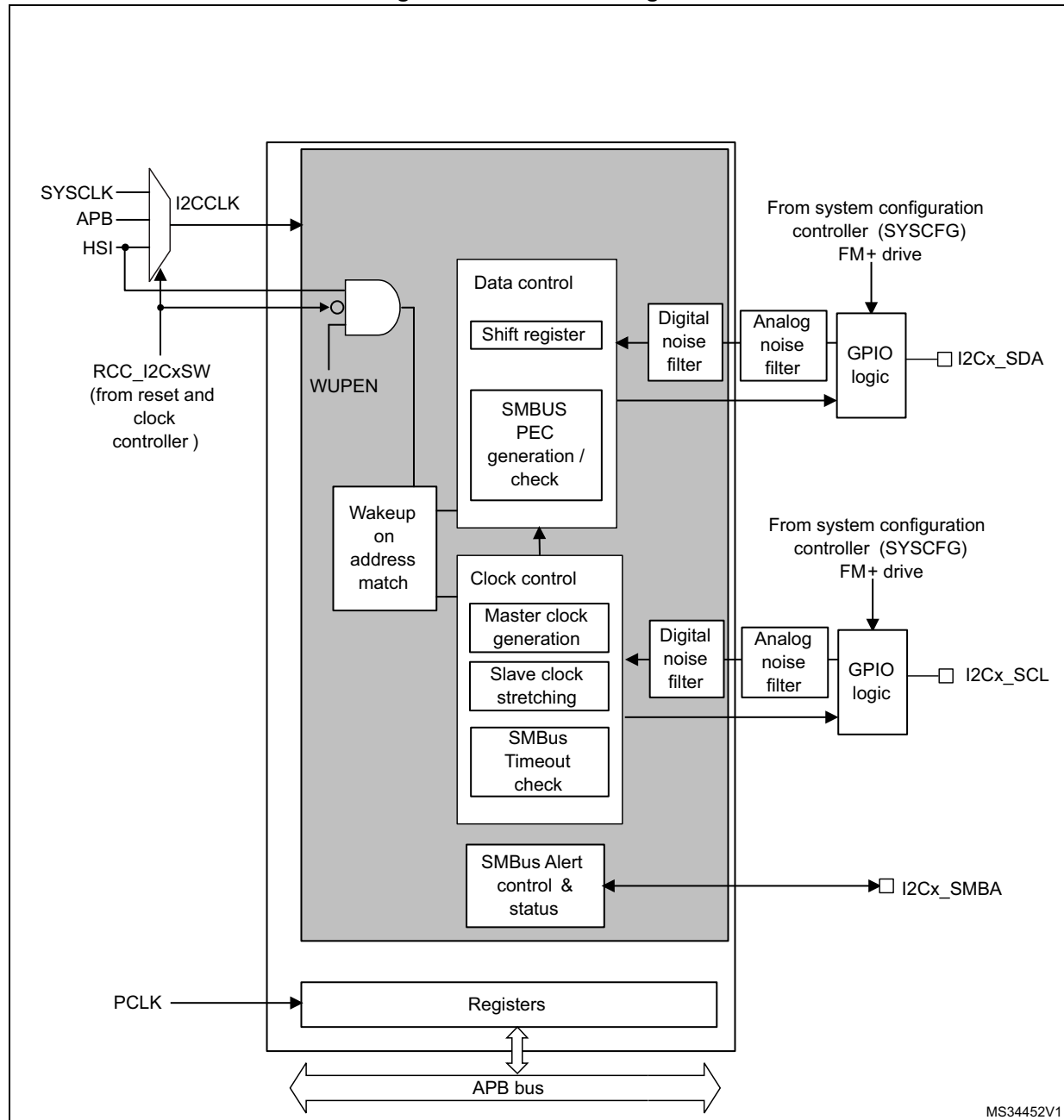
1: A shift operation is pending

This flag is set by hardware as soon as a shift operation is initiated by a write to the RTC\_SHIFTR register. It is cleared by hardware when the corresponding shift operation has been executed. Writing to the SHPF bit has no effect.

### 35.4.1 I2C block diagram

The block diagram of the I2C interface is shown in [Figure 316](#).

**Figure 316. I2C block diagram**



The I2C is clocked by an independent clock source which allows to the I2C to operate independently from the PCLK frequency.

**Note:** At every clock pulse, after SCL falling edge detection, the I2C master or slave stretches SCL low during at least  $[(SDADEL+SCLDEL+1) \times (PRESC+1) + 1] \times t_{I2CCLK}$ , in both transmission and reception modes. In transmission mode, in case the data is not yet written in I2C\_TXDR when SDADEL counter is finished, the I2C keeps on stretching SCL low until the next data is written. Then new data MSB is sent on SDA output, and SCLDEL counter starts, continuing stretching SCL low to guarantee the data setup time.

If NOSTRETCH=1 in slave mode, the SCL is not stretched. Consequently the SDADEL must be programmed in such a way to guarantee also a sufficient setup time.

**Table 150. I<sup>2</sup>C-SMBUS specification data setup and hold times**

Symbol	Parameter	Standard-mode (Sm)		Fast-mode (Fm)		Fast-mode Plus (Fm+)		SMBUS		Unit
		Min.	Max	Min.	Max	Min.	Max	Min.	Max	
$t_{HD;DAT}$	Data hold time	0	-	0	-	0	-	0.3	-	$\mu s$
$t_{VD;DAT}$	Data valid time	-	3.45	-	0.9	-	0.45	-	-	
$t_{SU;DAT}$	Data setup time	250	-	100	-	50	-	250	-	ns
$t_r$	Rise time of both SDA and SCL signals	-	1000	-	300	-	120	-	1000	
$t_f$	Fall time of both SDA and SCL signals	-	300	-	300	-	120	-	300	

Additionally, in master mode, the SCL clock high and low levels must be configured by programming the PRESC[3:0], SCLH[7:0] and SCLL[7:0] bits in the I2C\_TIMINGR register.

- When the SCL falling edge is internally detected, a delay is inserted before releasing the SCL output. This delay is  $t_{SCLL} = (SCLL+1) \times t_{PRESC}$  where  $t_{PRESC} = (PRESC+1) \times t_{I2CCLK}$ .  $t_{SCLL}$  impacts the SCL low time  $t_{LOW}$ .
- When the SCL rising edge is internally detected, a delay is inserted before forcing the SCL output to low level. This delay is  $t_{SCLH} = (SCLH+1) \times t_{PRESC}$  where  $t_{PRESC} = (PRESC+1) \times t_{I2CCLK}$ .  $t_{SCLH}$  impacts the SCL high time  $t_{HIGH}$ .

Refer to [I2C master initialization](#) for more details.

**Caution:** Changing the timing configuration is not allowed when the I2C is enabled.

The I2C slave NOSTRETCH mode must also be configured before enabling the peripheral. Refer to [I2C slave initialization](#) for more details.

**Caution:** Changing the NOSTRETCH configuration is not allowed when the I2C is enabled.



**Note:** The CK pin works in conjunction with the TX pin. Thus, the clock is provided only if the transmitter is enabled (TE=1) and data is being transmitted (the data register USART\_TDR written). This means that it is not possible to receive synchronous data without transmitting data.

The LBCL, CPOL and CPHA bits have to be selected when the USART is disabled (UE=0) to ensure that the clock pulses function correctly.

Figure 358. USART example of synchronous transmission

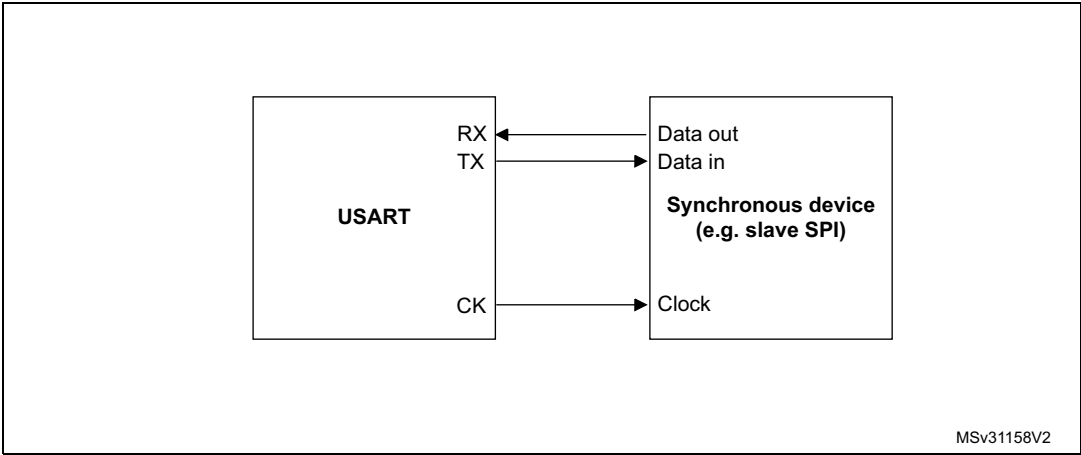
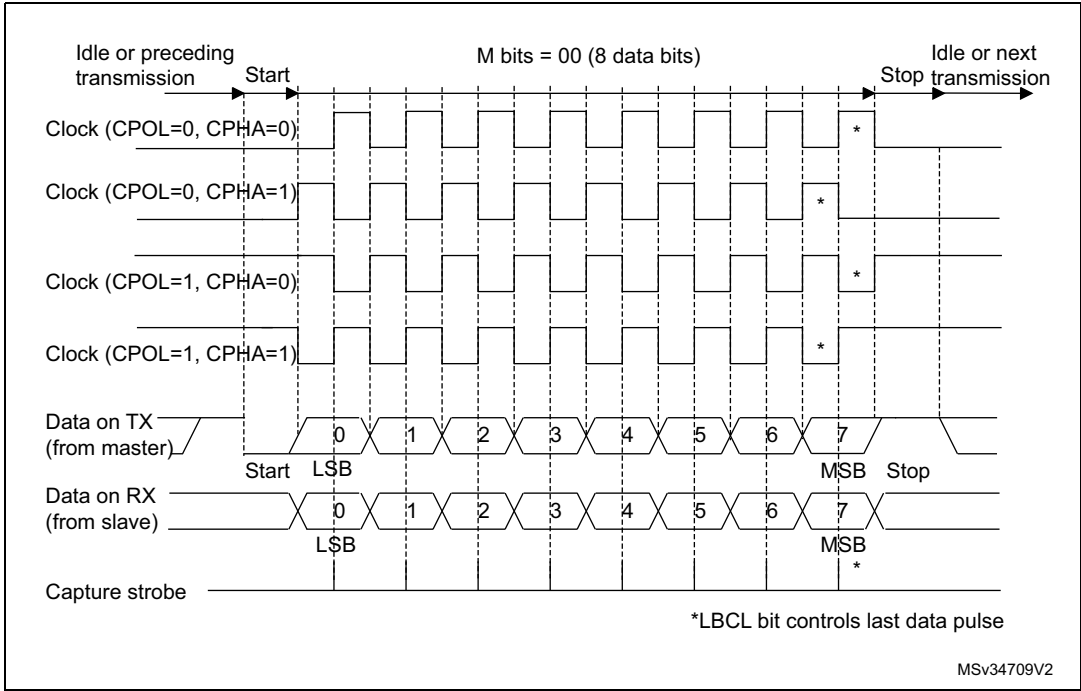


Figure 359. USART data clock timing diagram (M bits = 00)



Bits 3:2 Reserved, must be kept at reset value.

Bit 1 **TXE**: Transmit buffer empty

0: Tx buffer not empty  
1: Tx buffer empty

Bit 0 **RXNE**: Receive buffer not empty

0: Rx buffer empty  
1: Rx buffer not empty

### 38.6.4 SPI data register (SPIx\_DR)

Address offset: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DR[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 **DR[15:0]**: Data register

Data received or to be transmitted

The data register serves as an interface between the Rx and Tx FIFOs. When the data register is read, RxFIFO is accessed while the write to data register accesses Tx FIFO (See [Section 38.4.9: Data transmission and reception procedures](#)).

*Note: Data is always right-aligned. Unused bits are ignored when writing to the register, and read as zero when the register is read. The Rx threshold setting must always correspond with the read access currently used.*

### 38.6.5 SPI CRC polynomial register (SPIx\_CRCPR)

Address offset: 0x10

Reset value: 0x0007

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCPOLY[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw

Bits 15:0 **CRCPOLY[15:0]**: CRC polynomial register

This register contains the polynomial for the CRC calculation.

The CRC polynomial (0007h) is the reset value of this register. Another polynomial can be configured as required.

*Note: The polynomial value should be odd only. No even value is supported.*

Bits 31:19 Reserved, must be kept at reset value

Bits 18:16 **FLVL**: FIFO level threshold.

This bit is read only. The FIFO level threshold flag is managed only by hardware and its setting depends on SAI block configuration (transmitter or receiver mode).

If the SAI block is configured as transmitter:

000: FIFO empty

001:  $FIFO \leq \frac{1}{4}$  but not empty

010:  $\frac{1}{4} < FIFO \leq \frac{1}{2}$

011:  $\frac{1}{2} < FIFO \leq \frac{3}{4}$

100:  $\frac{3}{4} < FIFO$  but not full

101: FIFO full

If SAI block is configured as receiver:

000: FIFO empty

001:  $FIFO < \frac{1}{4}$  but not empty

010:  $\frac{1}{4} \leq FIFO < \frac{1}{2}$

011:  $\frac{1}{2} \leq FIFO < \frac{3}{4}$

100:  $\frac{3}{4} \leq FIFO$  but not full

101: FIFO full

Bits 15:7 Reserved, must be kept at reset value

Bit 6 **LFSDET**: Late frame synchronization detection.

This bit is read only.

0: No error.

1: Frame synchronization signal is not present at the right time.

This flag can be set only if the audio block is configured in slave mode.

It is not used in AC'97 or SPDIF mode.

It can generate an interrupt if LFSDETIE bit is set in the SAI\_xIM register.

This flag is cleared when the software sets bit CLFSDET in SAI\_xCLRFR register

Bit 5 **AFSDET**: Anticipated frame synchronization detection.

This bit is read only.

0: No error.

1: Frame synchronization signal is detected earlier than expected.

This flag can be set only if the audio block is configured in slave mode.

It is not used in AC'97 or SPDIF mode.

It can generate an interrupt if AFSDETIE bit is set in SAI\_xIM register.

This flag is cleared when the software sets CAFSDET bit in SAI\_xCLRFR register.

Bit 4 **CNRDY**: Codec not ready.

This bit is read only.

0: External AC'97 Codec is ready

1: External AC'97 Codec is not ready

This bit is used only when the AC'97 audio protocol is selected in the SAI\_xCR1 register and configured in receiver mode.

It can generate an interrupt if CNRDYIE bit is set in SAI\_xIM register.

This flag is cleared when the software sets CCNRDY bit in SAI\_xCLRFR register.

Table 225. R4b response (continued)

Bit position		Width (bits)	Value	Description
[39:8] Argument field	39	16	X	Card is ready
	[38:36]	3	X	Number of I/O functions
	35	1	X	Present memory
	[34:32]	3	X	Stuff bits
	[31:8]	24	X	I/O ORC
[7:1]		7	X	Reserved
0		1	1	End bit

Once an SD I/O card has received a CMD5, the I/O portion of that card is enabled to respond normally to all further commands. This I/O enable of the function within the I/O card will remain set until a reset, power cycle or CMD52 with write to I/O reset is received by the card. Note that an SD memory-only card may respond to a CMD5. The proper response for a memory-only card would be *Present memory* = 1 and *Number of I/O functions* = 0. A memory-only card built to meet the SD Memory Card specification version 1.0 would detect the CMD5 as an illegal command and not respond. The I/O aware host will send CMD5. If the card responds with response R4, the host determines the card's configuration based on the data contained within the R4 response.

#### 41.5.7 R5 (interrupt request)

Only for MultiMediaCard. Code length: 48 bits. If the response is generated by the host, the RCA field in the argument will be 0x0.

Table 226. R5 response

Bit position		Width (bits)	Value	Description
47		1	0	Start bit
46		1	0	Transmission bit
[45:40]		6	'101000'	CMD40
[39:8] Argument field	[31:16]	16	X	RCA [31:16] of winning card or of the host
	[15:0]	16	X	Not defined. May be used for IRQ data
[7:1]		7	X	CRC7
0		1	1	End bit

#### 41.5.8 R6

Only for SD I/O. The normal response to CMD3 by a memory device. It is shown in [Table 227](#).

### CAN mailbox data length control and time stamp register (CAN\_TDTxR) (x = 0..2)

All bits of this register are write protected when the mailbox is not in empty state.

Address offsets: 0x184, 0x194, 0x1A4

Reset value: 0xFFFF XXXX

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TIME[15:0]															
rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	DLC[3:0]			
												rw	rw	rw	rw

Bits 31:16 **TIME[15:0]**: Message time stamp

This field contains the 16-bit timer value captured at the SOF transmission.

Bits 15:9 Reserved, must be kept at reset value.

Bit 8 **TGT**: Transmit global time

This bit is active only when the hardware is in the Time Trigger Communication mode, TTCM bit of the CAN\_MCR register is set.

0: Time stamp TIME[15:0] is not sent.

1: Time stamp TIME[15:0] value is sent in the last two data bytes of the 8-byte message: TIME[7:0] in data byte 7 and TIME[15:8] in data byte 6, replacing the data written in CAN\_TDHxR[31:16] register (DATA6[7:0] and DATA7[7:0]). DLC must be programmed as 8 in order these two bytes to be sent over the CAN bus.

Bits 7:4 Reserved, must be kept at reset value.

Bits 3:0 **DLC[3:0]**: Data length code

This field defines the number of data bytes a data frame contains or a remote frame request. A message can contain from 0 to 8 data bytes, depending on the value in the DLC field.