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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	24MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78l052a24pl

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

1. GENERAL DESCRIPTION

The W78L052 is an 8-bit microcontroller which can accommodate a wider frequency range with low power consumption. The instruction set for the W78L052 is fully compatible with the standard 8051. The W78L052 contains an 8K bytes Flash EPROM; a 256 bytes RAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit I/O port P4; three 16-bit timer/counters; a hardware watchdog timer and a serial port. These peripherals are supported by eight sources two-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78L052 allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

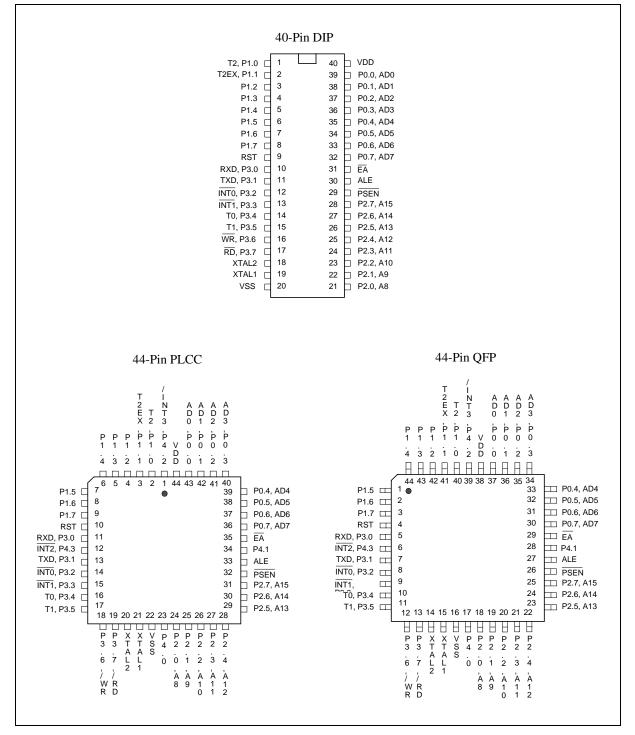
The W78L052 microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.

2. FEATURES

- Fully static design 8-bit CMOS microcontroller
- Wide supply voltage of 2.4V to 5.5V
- 256 bytes of on-chip scratchpad RAM
- 8 KB electrically erasable/programmable Flash EPROM
- 64 KB program memory address space
- 64 KB data memory address space
- Four 8-bit bi-directional ports
- One extra 4-bit bit-addressable I/O port, additional INT2 / INT3 (available on 44-pin PLCC/QFP package)
- Three 16-bit timer/counters
- One full duplex serial port(UART)
- Watchdog Timer
- Eight sources, two-level interrupt capability
- EMI reduction mode
- Built-in power management
- Code protection mechanism
- Packages:
 - Lead Free (RoHS) DIP 40: W78L052A24DL
 - Lead Free (RoHS) PLCC 44: W78L052A24PL
 - Lead Free (RoHS) PQFP 44: W78L052A24FL



3. PIN CONFIGURATIONS



Publication Release Date: November 6, 2006 Revision A6

4. PIN DESCRIPTION

SYMBOL	DESCRIPTIONS
ĒĀ	EXTERNAL ACCESS ENABLE : This pin forces the processor to execute out of external ROM. It should be kept high to access internal ROM. The ROM address and data will not be presented on the bus if \overline{EA} pin is high and the program counter is within on-chip ROM area.
PSEN	PROGRAM STORE ENABLE : PSEN enables the external ROM data onto the Port 0 address/ data bus during fetch and MOVC operations. When internal ROM access is performed, no PSEN strobe signal outputs from this pin.
ALE	ADDRESS LATCH ENABLE : ALE is used to enable the address latch that separates the address from the data on Port 0.
RST	RESET : A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	CRYSTAL1 : This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	CRYSTAL2: This is the crystal oscillator output. It is the inversion of XTAL1.
Vss	GROUND: Ground potential
Vdd	POWER SUPPLY: Supply voltage for operation.
P0.0-P0.7	PORT 0 : Port 0 is a bi-directional I/O port which also provides a multiplexed low order address/data bus during accesses to external memory. The Port 0 is also an open-drain port and external pull-ups need to be connected while in programming.
P1.0-P1.7	PORT 1 : Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture control
P2.0-P2.7	PORT 2 : Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0-P3.7	PORT 3 : Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0) : Serial Port receiver input TXD(P3.1) : Serial Port transmitter output INT0 (P3.2) : External Interrupt 0 INT1 (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input WR (P3.6) :External Data Memory Write Strobe RD (P3.7) : External Data Memory Read Strobe
P4.0-P4.3	PORT 4: Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources $(\overline{INT2}/\overline{INT3})$.

5.1 Eight-source interrupt information:

INTERRUPT SOURCE	VECTOR ADDRESS	POLLING SEQUENCE WITHIN PRIORITY LEVEL	ENABLE REQUIRED SETTINGS	INTERRUPT TYPE EDGE/LEVEL
External Interrupt 0	03H	0 (highest)	IE.0	TCON.0
Timer/Counter 0	0BH	1	IE.1	-
External Interrupt 1	13H	2	IE.2	TCON.2
Timer/Counter 1	1BH	3	IE.3	-
Serial Port	23H	4	IE.4	-
Timer/Counter 2	2BH	5	IE.5	-
External Interrupt 2	33H	6	XICON.2	XICON.0
External Interrupt 3	3BH	7 (lowest)	XICON.6	XICON.3

2. PORT4

Another bit-addressable port P4 is also available and only 4 bits (P4<3:0>) can be used. This port address is located at 0D8H with the same function as that of port P1, except the P4.3 and P4.2 are alternative function pins. It can be used as general I/O pins or external interrupt input sources ($\overline{INT2}$, $\overline{INT3}$).

Example:

P4	REG 0D8H	
MOV	P4, #0AH	; Output data "A" through P4.0–P4.3.
MOV	A, P4	; Read P4 status to Accumulator.
ORL	P4.#0000001E	5
ANL	P4.#11111110E	6

3. Reduce EMI Emission

Because of on-chip Flash EPROM, when a program is running in internal ROM space, the ALE will be unused. The transition of ALE will cause noise, so it can be turned off to reduce the EMI emission if it is useless. Turning off the ALE signal transition only requires setting the bit 0 of the AUXR SFR, which is located at 08Eh. When ALE is turned off, it will be reactivated when the program accesses external ROM/RAM data or jumps to execute an external ROM code. The ALE signal will turn off again after it has been completely accessed or the program returns to internal ROM code space. The AO bit in the AUXR register, when set, disables the ALE output. In order to reduce EMI emission from oscillation circuitry, W78L052 allows user to diminish the gain of on-chip oscillator amplifiers by using programmer to clear the B7 bit of security register. Once B7 is set to 0, a half of gain will be decreased. Care must be taken if user attempts to diminish the gain of oscillator amplifier, reducing a half of gain may affect the external crystal operating improperly at high frequency above 24MHz. The value of R and C1, C2 may need some adjustment while running at lower gain.

***AUXR - Auxiliary register (8EH)

	-	-	-	-	-	-	-	AO
--	---	---	---	---	---	---	---	----

AO: Turn off ALE output.

4. Power-off Flag

***PCON - Power control (87H)

POF GF1 GF0 PD IDL

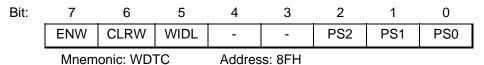
- POF: Power off flag. Bit is set by hardware when power on reset. It can be cleared by software to determine chip reset is a warm boot or cold boot.
- GF1, GF0: These two bits are general-purpose flag bits for the user.
- PD: Power down mode bit. Set it to enter power down mode.
- IDL: Idle mode bit. Set it to enter idle mode.

The power-off flag is located at PCON.4. This bit is set when VDD has been applied to the part. It can be used to determine if a reset is a warm boot or a cold boot if it is subsequently reset by software.

Watchdog Timer

The Watchdog timer is a free-running timer which can be programmed by the user to serve as a system monitor, a time-base generator or an event timer. It is basically a set of dividers that divide the system clock. The divider output is selectable and determines the time-out interval. When the time-out occurs a system reset can also be caused if it is enabled. The main use of the Watchdog timer is as a system monitor. This is important in real-time control applications. In case of power glitches or electromagnetic interference, the processor may begin to execute errant code. If this is left unchecked the entire system may crash. The watchdog time-out selection will result in different time-out values depending on the clock speed. The Watchdog timer will de disabled on reset. In general, software should restart the Watchdog timer to put it into a known state. The control bits that support the Watchdog timer are discussed below.

Watchdog Timer Control Register



ENW : Enable watch-dog if set.

CLRW : Clear watch-dog timer and prescaler if set. This flag will be cleared automatically

WIDL : If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is disabled under IDLE mode. Default is cleared.

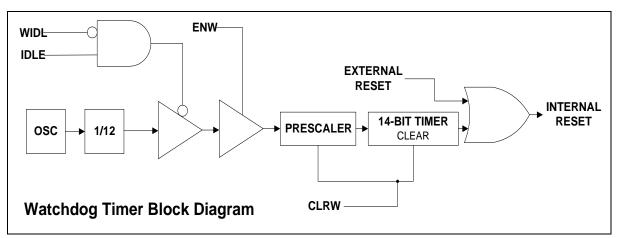
PS2, PS1, PS0: Watch-dog prescaler timer select. Prescaler is selected when set PS2–0 as follows:

PS2 PS1 PS0	PRESCALER SELECT
0 0 0	2
0 1 0	4
0 0 1	8
0 1 1	16
1 0 0	32
1 0 1	64
1 1 0	128
1 1 1	256

The time-out period is obtained using the following equation:

 $\frac{1}{OSC} \times 2^{14} \times PRESCALER \times 1000 \times 12 \text{ mS}$

Before Watchdog time-out occurs, the program must clear the 14-bit timer by writing 1 to WDTC.6 (CLRW). After 1 is written to this bit, the 14-bit timer, prescaler and this bit will be reset on the next instruction cycle. The Watchdog timer is cleared on reset.



Typical Watch-Dog time-out period when OSC = 20 MHz

PS2 PS1 PS0	WATCHDOG TIME-OUT PERIOD
0 0 0	19.66 mS
0 1 0	39.32 mS
0 0 1	78.64 mS
0 1 1	157.28 mS
1 0 0	314.57 mS
1 0 1	629.14 mS
1 1 0	1.25 S
1 1 1	2.50 S

6. ON-CHIP FLASH EPROM CHARACTERISTICS

The W78L052 has several modes to program the on-chip Flash EPROM. All these operations are configured by the pins RST, ALE, $\overrightarrow{\text{PSEN}}$, A9CTRL(P3.0), A13CTRL(P3.1), A14CTRL(P3.2), OECTRL(P3.3), $\overrightarrow{\text{CE}}$ (P3.6), $\overrightarrow{\text{OE}}$ (P3.7), A0(P1.0) and VPP($\overrightarrow{\text{EA}}$). Moreover, the A15–A0(P2.7–P2.0, P1.7–P1.0) and the D7–D0(P0.7–P0.0) serve as the address and data bus respectively for these operations.

Read Operation

This operation is supported for customer to read their code and the Security bits. The data will not be valid if the Lock bit is programmed to low.

Output Disable Condition

When the \overline{OE} is set to high, no data output appears on the D7..D0.

Program Operation

This operation is used to program the data to Flash EPROM and the security bits. Program operation is done when the VPP is reach to VCP (12.5V) level, \overline{CE} set to low, and \overline{OE} set to high.

Program Verify Operation

All the programming data must be checked after program operations. This operation should be performed after each byte is programmed; it will ensure a substantial program margin.

Erase Operation

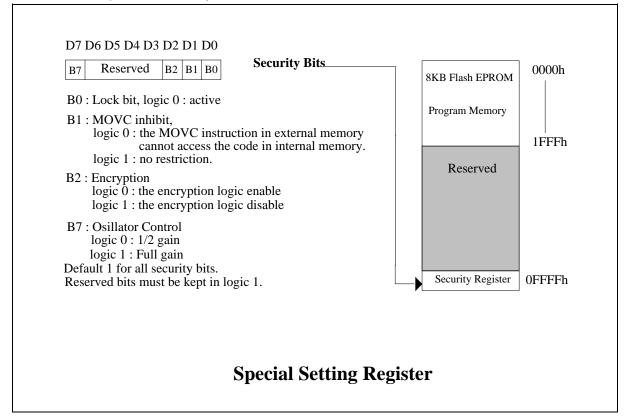
An erase operation is the only way to change data from 0 to 1. This operation will erase all the Flash EPROM cells and the security bits from 0 to 1. This erase operation is done when the VPP is reach to VEP level, \overline{CE} set to low, and \overline{OE} set to high.



7. SECURITY BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78L052 has a Special Setting Register, the Security Register, which can not be accessed in normal mode. The Security register can only be accessed from the Flash EPROM operation mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They can only be reset through erase-all operation. The Security Register is addressed in the Flash EPROM operation mode by address #0FFFFh.



Lock bit

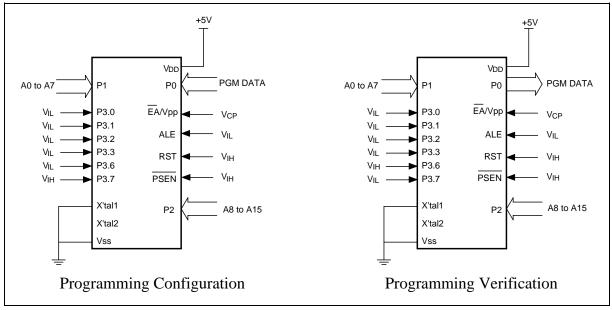
This bit is used to protect the customer's program code in the W78L052. It may be set after the programmer finishes the programming and verifies sequence. Once this bit is set to logic 0, both the Flash EPROM data and Special Setting Registers can not be accessed again.

MOVC Inhibit

This bit is used to restrict the accessible region of the MOVC instruction. It can prevent the MOVC instruction in external program memory from reading the internal program code. When this bit is set to logic 0, a MOVC instruction in external program memory space will be able to access code only in the external memory, not in the internal memory. A MOVC instruction in internal program memory space will always be able to access the ROM data in both internal and external memory. If this bit is logic 1, there are no restrictions on the MOVC instruction.

Encryption

This bit is used to enable/disable the encryption logic for code protection. Once encryption feature is enabled, the data presented on port 0 will be encoded via encryption logic. Only whole chip erase will reset this bit.



8. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN.	MAX.	UNIT
DC Power Supply	VDD-VSS	-0.3	+7.0	V
Input Voltage	Vin	Vss -0.3	Vdd +0.3	V
Operating Temperature	ТА	0	70	°C
Storage Temperature	Tst	-55	+150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

9. DC CHARACTERISTICS

Vss = 0V, TA = 25° C, unless otherwise specified.

PARAMETER	SYM.	SPEC		UNIT	TEST CONDITIONS
PARAMETER	3 T WI.	MIN.	MAX.	UNIT	TEST CONDITIONS
Operating Voltage	Vdd	2.4	5.5	V	
Operating Current		-	20	mA	No load VDD = 5.5V
Operating Current	IDD	-	3	mA	No load VDD = 2.4V
Idle Current		-	6	mA	VDD = 5.5V, FOSC = 20 MHz
Idle Current	IDLE	-	1.5	mA	VDD = 2.4V, FOSC = 12 MHz
Davisa Davis Oversant		-	50	μA	VDD = 5.5V, FOSC = 20 MHz
Power Down Current	IPWDN	-	20	μA	VDD = 2.4V, FOSC = 12 MHz
Input Current		50	. 40		VDD = 5.5V
P1, P2, P3, P4	lin1	-50	+10	μA	VIN = 0V or VDD
Input Current	luvio	10	1200		VDD = 5.5V
RST	lin2	-10	+300	μA	0 < VIN < VDD
Input Leakage Current	Ilk	-10	+10	μA	VDD = 5.5V
P0, EA		-10	+10	μΛ	0V < VIN < VDD
Logic 1 to 0 Transition Current	Itl ^[*4]	-500			VDD = 5.5V
P1, P2, P3, P4	IIL	-500	-	μA	VIN = 2.0V
Input Low Voltage	VIL1	0	0.8	V	VDD = 4.5V
P0, P1, P2, P3, P4, EA		0	0.5	V	VDD = 2.4V
Input Low Voltage	VIL2	0	0.8	V	VDD = 4.5V
RST[*1]		0	0.3	V	VDD = 2.4V
Input Low Voltage	VIL3	0	0.8	V	VDD = 4.5V
XTAL1 [*3]		0	0.6	V	VDD = 2.4V
Input High Voltage	VIH1	2.4	Vdd +0.2	V	VDD = 5.5V
P0, P1, P2, P3, P4, EA		1.4	Vdd +0.2	V	VDD = 2.4V
Input High Voltage	VIH2	3.5	Vdd +0.2	V	VDD = 5.5V
RST[*1]		1.7	Vdd +0.2	V	VDD = 2.4V
Input High Voltage	Vінз	3.5	Vdd +0.2	V	VDD = 5.5V
XTAL1 [*3]		1.6	Vdd +0.2	V	VDD = 2.4V
Output Low Voltage	VOL1	-	0.45	V	VDD = 4.5V, IOL = +2 mA
P1, P2, P3, P4		-	0.25	V	VDD = 2.4V, $IOL = +1 mA$
Output Low Voltage	VOL2	-	0.45	V	VDD = 4.5V, IOL = +4 mA
P0, ALE, PSEN [*2]		-	0.25	V	VDD = 2.4V, IOL = +2 mA

W78LE52/W78L052A **THE WINDOND SET**

DC Characteristics, continued

PARAMETER	SYM.	PECIFICATION		UNIT	TEST CONDITIONS
FARAMETER	5 T WI.	MIN.	MAX.	UNIT	TEST CONDITIONS
Sink Current	ISK1	4	12	mA	VDD = 4.5V, Vin = 0.45V
P1, P2, P3, P4		1.8	5.4	mA	VDD = 2.4V, Vin = 0.45V
Sink Current	ISK2	8	16	mA	VDD = 4.5V, Vin = 0.45V
P0, ALE, PSEN		4.0	9	mA	VDD = 2.4V, Vin = 0.45V
Output High Voltage	VOH1	2.4	-	V	$VDD = 4.5V$, IOH = -100 μ A
P1, P2, P3, P4		1.4	-	V	VDD = 2.4V, IOH = -8 μ A
Output High Voltage	Voh2	2.4	-	V	Vdd = 4.5V, Ioh = -400 μ A
P0, ALE, PSEN [*2]		1.4	-	V	VDD = 2.4V, IOH = -200 μ A
Source Current	ISR1	-100	-250	μA	VDD = 4.5V, Vin = 2.4V
P1, P2, P3, P4		-10	-30	μA	VDD = 2.4V, Vin = 1.4V
Source Current	ISR2	-8	-14	mA	VDD = 4.5V, Vin = 2.4V
P0, ALE, PSEN		-1.0	-2.4	mA	VDD = 2.4V, Vin = 1.4V

Notes:

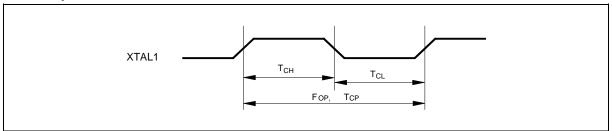
*1. RST pin is a Schmitt trigger input.*2. P0, ALE and /PSEN are tested in the external access mode.

*3. XTAL1 is a CMOS input.
*4. Pins of P1, P2, P3, P4 can source a transition current when they are being externally driven from 1 to 0.

10. AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ± 20 nS variation. The numbers below represent the performance expected from a 0.6micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	0	-	20	MHz	1
Clock Period	Тср	50	-	-	nS	2
Clock High	Тсн	25	-	-	nS	3
Clock Low	TCL	25	-	-	nS	3

Notes:

1. The clock may be stopped indefinitely in either state.

2. The TCP specification is used as a reference in other specifications.

3. There are no duty cycle requirements on the XTAL1 input.

Program Fetch Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Address Valid to ALE Low	TAAS	1 Tcp -∆	-	-	nS	4
Address Hold from ALE Low	Таан	1 TCP - Δ	-	-	nS	1, 4
ALE Low to PSEN Low	TAPL	1 TCP - Δ	-	-	nS	4
PSEN Low to Data Valid	Tpda	-	-	2 TCP	nS	2
Data Hold after PSEN High	TPDH	0	-	1 TCP	nS	3
Data Float after PSEN High	TPDZ	0	-	1 TCP	nS	
ALE Pulse Width	TALW	2 TCP - Δ	2 TCP	-	nS	4
PSEN Pulse Width	Tpsw	3 Tcp -Δ	3 Тср	-	nS	4

Notes:

1. P0.0–P0.7, P2.0–P2.7 remain stable throughout entire memory cycle.

2. Memory access time is 3 Tcp.

3. Data have been latched internally prior to PSEN going high.

4. " Δ " (due to buffer driving delay and wire loading) is 20 nS.

Program Operation

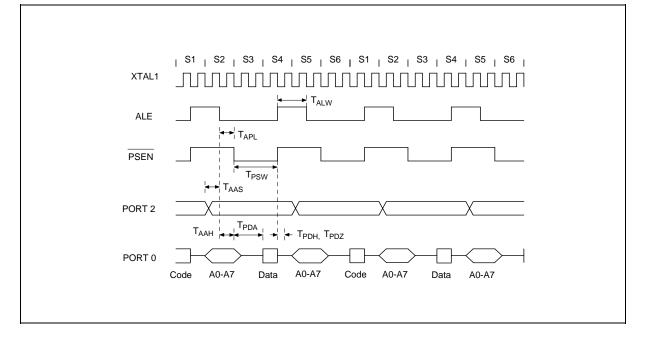
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
VPP Setup Time	TVPS	2.0	-	-	μS
Data Setup Time	TDS	2.0	-	-	μS
Data Hold Time	Трн	2.0	-	-	μS
Address Setup Time	Tas	2.0	-	-	μS
Address Hold Time	Тан	0	-	-	μS
CE Program Pulse Width for Program Operation	TPWP	290	300	310	μS
OECTRL Setup Time	Tocs	2.0	-	-	μS
OECTRL Hold Time	Тосн	2.0	-	-	μS
OE Setup Time	TOES	2.0	-	-	μS
OE High to Output Float	TDFP	0	-	130	nS
Data Valid from \overline{OE}	Τοεν	-	-	150	nS

Note: Flash data can be accessed only in flash mode. The RST pin must pull in VIH status, the ALE pin must pull in VIL status, and the PSEN pin must pull in VIH status.

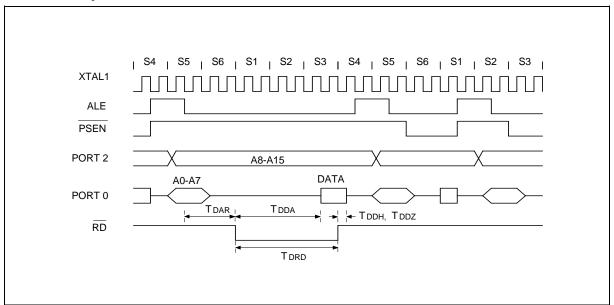


11. TIMING WAVEFORMS

Program Fetch Cycle



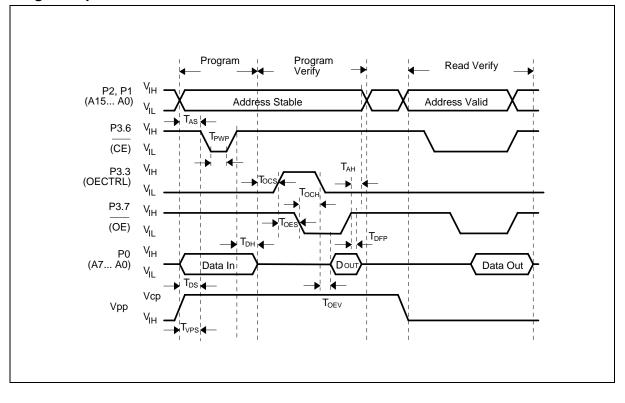
Data Read Cycle





Timing Waveforms, continued

Program Operation



12. TYPICAL APPLICATION CIRCUITS

Expanded External Program Memory and Crystal

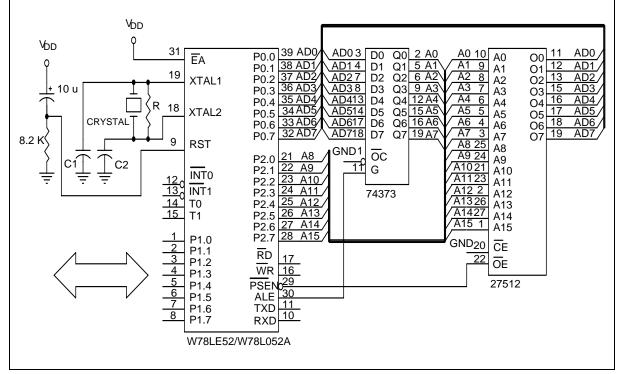


Figure A

CRYSTAL	C1	C2	R
16 MHz	30P	30P	-
20 MHz	15P	15P	-

Above table shows the reference values for crystal applications (full gain).

Note: C1, C2, R components refer to Figure A.



Typical Application Circuits, continued

Expanded External Data Memory and Oscillator

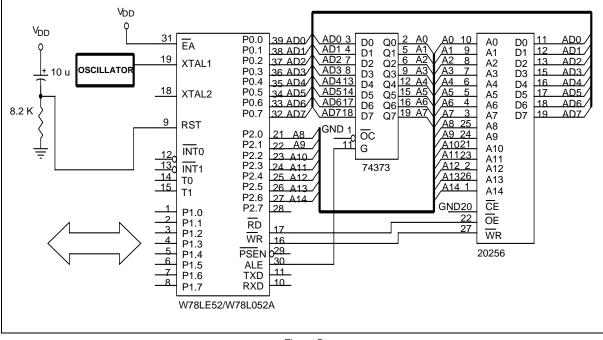
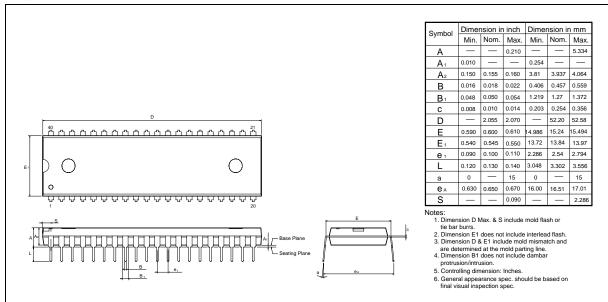


Figure B

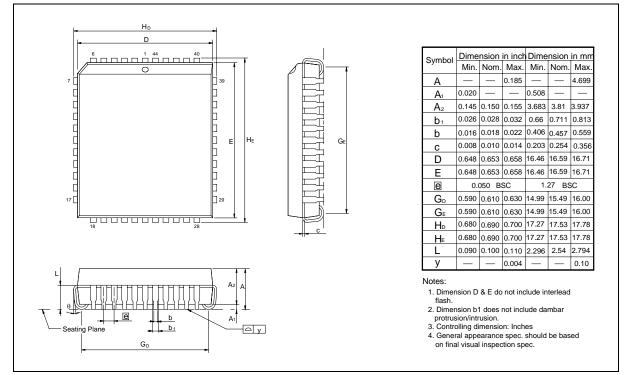


13. PACKAGE DIMENSIONS

40-pin DIP



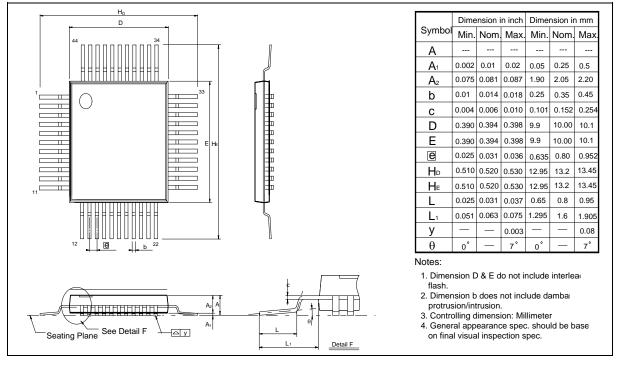
44-pin PLCC





Package Dimensions, continued

44-pin PQFP





14. REVISION HISTORY

VERSION	DATE	PAGE	REASONS FOR CHANGE
A3	December 2000		-
A4	April 19, 2005	25	Add Important Notice
A5	June 14, 2005	2	Add Lead Free (RoHS) parts
			Remove block diagram
A6	November 6, 2006	2	Remove all Leaded parts
		16	Revise Operating speed to 20MHz

Important Notice

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