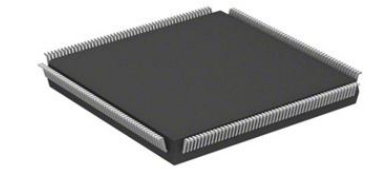
Infineon Technologies - MB91F591BHPMC-GSK5E1 Datasheet



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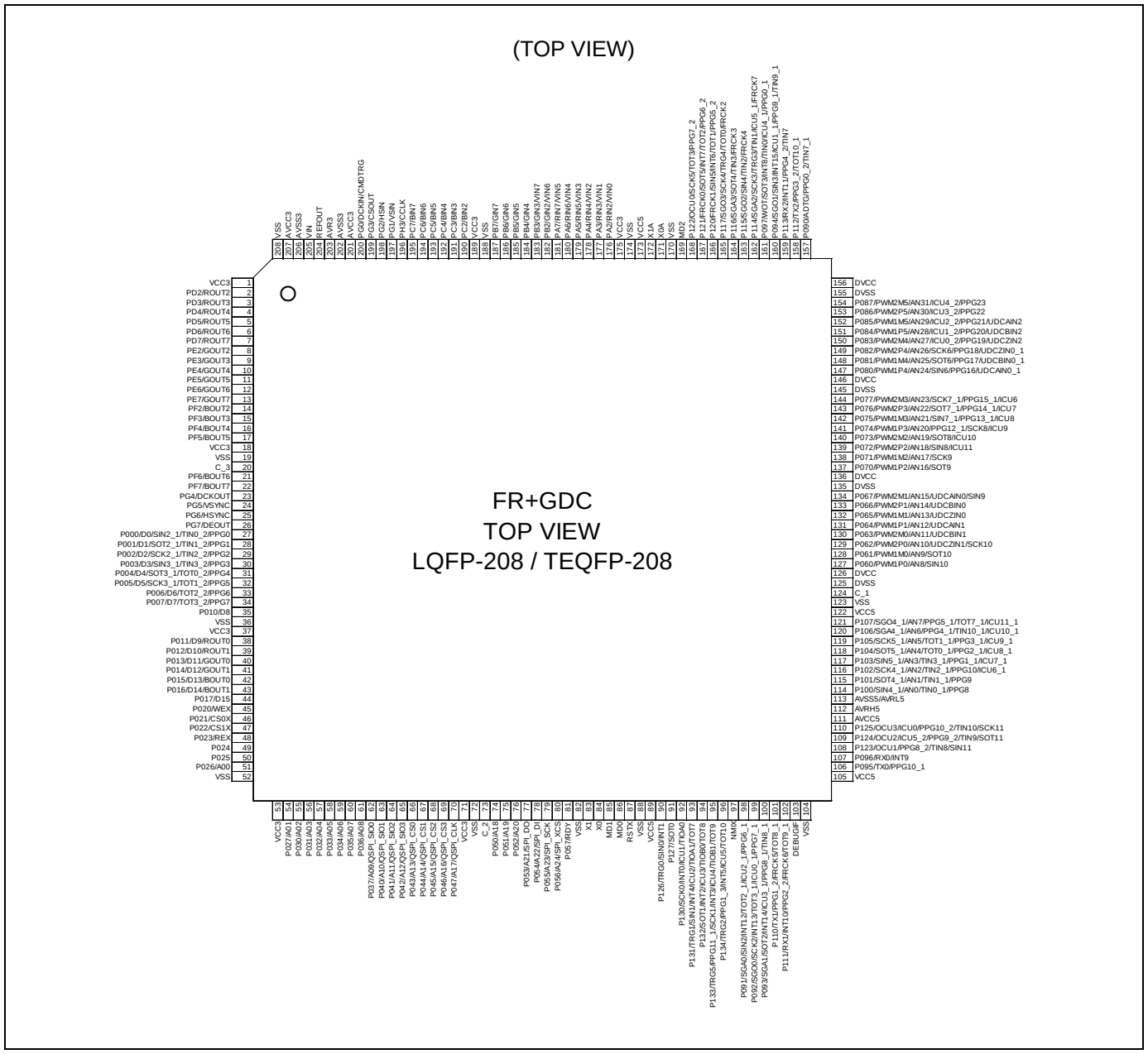
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	308K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f591bhpmc-gsk5e1

2.4 Pin Assignment (MB91F59A/B dual Clock Product)



3. Pin Description

3.1 Pin Description of LQFP-208/TEQFP-208

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
84	X0	–	L	Main clock oscillation input pin
83	X1	–	L	Main clock oscillation output pin
171 (dual clock product)	X0A	–	N	Sub clock oscillation input pin
172 (dual clock product)	X1A	–	N	Sub clock oscillation output pin
171 (single clock product)	P137	–	A	General-purpose I/O port
172 (single clock product)	P136	–	A	General-purpose I/O port
97	NMIX	N	F1	Non-masking interrupt input pin
87	RSTX	N	F1	External reset input pin
86	MD0	–	P	Mode pin 0
85	MD1	–	P	Mode pin 1
169	MD2	–	F2	Mode pin 2
27	P000	–	O	General-purpose I/O port (3V pin)
	D0	–		External bus · Data bit0 I/O pin
	SIN2_1	–		LIN-UART ch.2 serial data input pin (1)
	TIN0_2	–		Reload timer ch.0 event input pin (2)
	PPG0	–		PPG ch.0 output pin
28	P001	–	O	General-purpose I/O port (3V pin)
	D1	–		External bus · Data bit1 I/O pin
	SOT2_1	–		LIN-UART ch.2 serial data output pin (1)
	TIN1_2	–		Reload timer ch.1 event input pin (2)
	PPG1	–		PPG ch.1 output pin
29	P002	–	O	General-purpose I/O port (3V pin)
	D2	–		External bus · Data bit2 I/O pin
	SCK2_1	–		LIN-UART ch.2 clock I/O pin (1)
	TIN2_2	–		Reload timer ch.2 event input pin (2)
	PPG2	–		PPG ch.2 output pin
30	P003	–	O	General-purpose I/O port (3V pin)
	D3	–		External bus · Data bit3 I/O pin
	SIN3_1	–		LIN-UART ch.3 serial data input pin (1)
	TIN3_2	–		Reload timer ch.3 event input pin (2)
	PPG3	–		PPG ch.3 output pin
31	P004	–	O	General-purpose I/O port (3V pin)
	D4	–		External bus · Data bit4 I/O pin
	SOT3_1	–		LIN-UART ch.3 serial data output pin (1)
	TOT0_2	–		Reload timer ch.0 output pin (2)
	PPG4	–		PPG ch.4 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
121	P107	–	C	General-purpose I/O port
	SGO4_1	–		Sound generator ch.4 SGO output pin
	AN7	–		ADC Analog 7 input pin
	PPG5_1	–		PPG ch.5 output pin (1)
	TOT7_1	–		Reload timer ch.7 output pin (1) (MB91F59A/B only)
	ICU11_1	–		Input capture ch.11 input pin (1) (MB91F59A/B only)
101	P110	–	C	General-purpose I/O port
	TX1	–		CAN transmission data1 output pin
	PPG1_2	–		PPG ch.1 output pin (2)
	FRCK5	–		Free-run timer 5 clock input pin(MB91F59A/B only)
	TOT8_1	–		Reload timer ch.8 output pin (1) (MB91F59A/B only)
102	P111	–	C	General-purpose I/O port
	RX1	–		CAN reception data 1 input pin
	INT10	–		INT10 External interrupt input pin
	PPG2_2	–		PPG ch.2 output pin (2)
	FRCK6	–		Free-run timer 6 clock input pin(MB91F59A/B only)
	TOT9_1	–		Reload timer ch.9 output pin (1) (MB91F59A/B only)
158	P112	–	C	General-purpose I/O port
	TX2	–		CAN transmission data 2 output pin
	PPG3_2	–		PPG ch.3 output pin (2)
	TOT10_1	–		Reload timer ch.10 output pin (1) (MB91F59A/B only)
159	P113	–	C	General-purpose I/O port
	RX2	–		CAN reception data 2 input pin
	INT11	–		INT11 External interrupt input pin
	PPG4_2	–		PPG ch.4 output pin (2)
	TIN7	–		Reload timer ch.7 event input pin(MB91F59A/B only)
162	P114	–	C	General-purpose I/O port
	SGA2	–		Sound generator ch.2 SGA output pin
	SCK3	–		LIN-UART ch.3 clock I/O pin
	TRG3	–		PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1	–		Reload timer ch.1 event input pin
	ICU5_1	–		Input capture ch.5 input pin (1)
	FRCK7	–		Free-run timer 7 clock input pin(MB91F59A/B only)
163	P115	–	C	General-purpose I/O port
	SGO2	–		Sound generator ch.2 SGO output pin
	SIN4	–		LIN-UART ch.4 serial data input pin
	TIN2	–		Reload timer ch.2 event input pin
	FRCK4	–		Free-run timer 4 clock input pin(MB91F59A/B only)
164	P116	–	C	General-purpose I/O port
	SGA3	–		Sound generator ch.3 SGA output pin
	SOT4	–		LIN-UART ch.4 serial data output pin
	TIN3	–		Reload timer ch.3 event input pin
	FRCK3	–		Free-run timer 3 clock input pin(MB91F59A/B only)
165	P117	–	C	General-purpose I/O port
	SGO3	–		Sound generator ch.3 SGO output pin
	SCK4	–		LIN-UART ch.4 clock I/O pin
	TRG4	–		PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0	–		Reload timer ch.0 output pin
	FRCK2	–		Free-run timer 2 clock input pin(MB91F59A/B only)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
165	AN17	–	E	ADC Analog 17 input pin
	P071			General-purpose I/O port
	SCK9			Multi-function serial ch.9 clock I/O pin
	PWM1M2			SMC ch.2 output pin
166	AN14	–	E	ADC Analog 14 input pin
	P066			General-purpose I/O port
	PWM2P1			SMC ch.1 output pin
	UDCBIN0			Up/down counter ch.0 BIN input pin
167	AN11	–	E	ADC Analog 11 input pin
	P063			General-purpose I/O port
167	PWM2M0			SMC ch.0 output pin
	UDCBIN1			Up/down counter ch.1 BIN input pin
168	AN8	–	E	ADC Analog 8 input pin
	P060			General-purpose I/O port
	SIN10			Multi-function serial ch.10 serial data input pin
	PWM1P0			SMC ch.0 output pin
169	VCC5	–	–	+5.0V power supply pin
170	AN6	–	C	ADC Analog 6 input pin
	P106			General-purpose I/O port
	ICU10_1			Input capture ch.10 input pin (1)
	PPG4_1			PPG ch.4 output pin (1)
	TIN10_1			Reload timer ch.10 event input pin (1)
	SGA4_1			Sound generator ch.4 SGA output pin
171	AN3	–	C	ADC Analog 3 input pin
	P103			General-purpose I/O port
	ICU7_1			Input capture ch.7 input pin (1)
	SIN5_1			LIN-UART ch.5 serial data input pin (1)
	PPG1_1			PPG ch.1 output pin (1)
	TIN3_1			Reload timer ch.3 event input pin (1)
172	AN1	–	C	ADC Analog 1 input pin
	P101			General-purpose I/O port
	SOT4_1			LIN-UART ch.4 serial data output pin (1)
	PPG9			PPG ch.9 output pin
	TIN1_1			Reload timer ch.1 event input pin (1)
173	AN0	–	C	ADC Analog 0 input pin
	P100			General-purpose I/O port
	SIN4_1			LIN-UART ch.4 serial data input pin (1)
	PPG8			PPG ch.8 output pin
	TIN0_1			Reload timer ch.0 event input pin (1)
174	TX0	–	A	CAN transmission data0 output pin
	P095			General-purpose I/O port
	PPG10_1			PPG ch.10 output pin (1)
175	VSS	–	–	GND pin
176	P092	–	C	General-purpose I/O port
	ICU0_1			Input capture ch.0 input pin (1)
	INT13			INT13 External interrupt input pin
	SCK2			LIN-UART ch.2 clock I/O pin
	PPG7_1			PPG ch.7 output pin (1)
	TOT3_1			Reload timer ch.3 output pin (1)
	SGO0			Sound generator ch.0 SGO output pin

■Precautions when writing to registers including the status flag
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

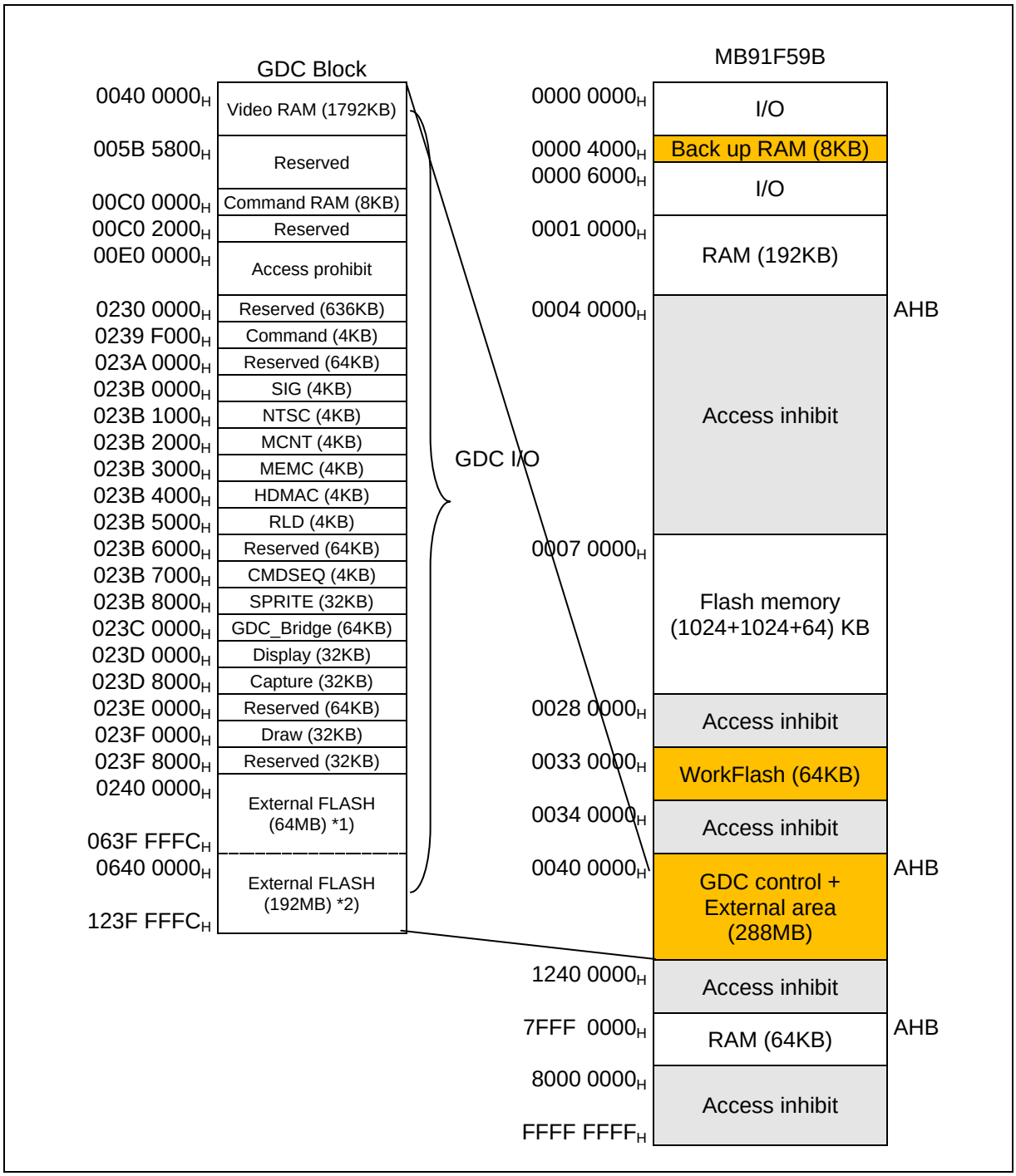
The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note:

These points can be ignored because the bit instructions to a register which supports RMW are already taken the points into consideration. Care must be taken when the bit instruction is used to a register which does not support RMW.

■GDC memory map

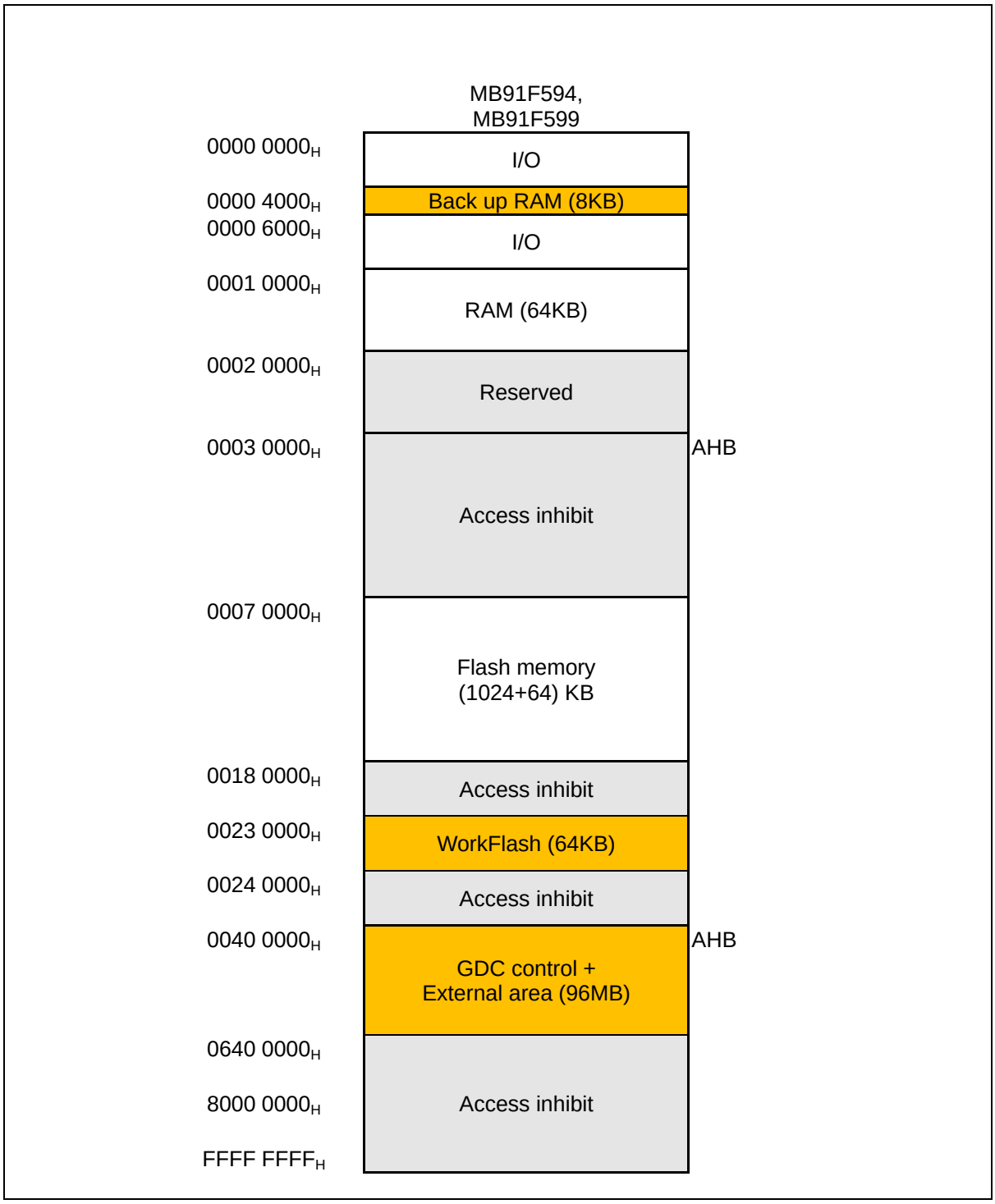


Note: The GDC area is executed mapping with the little endian.

*1) Parallel interface supports 64MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192MB of memory space from 0640_0000H to 123F_FFFFH.
(HS-SPI totally supports 256MB of memory space from 0240_0000H to 123F_FFFFH for External FLASH)

■Memory map


MB91F594,
MB91F599
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (64KB)
0002 0000H
Reserved
0003 0000H
Access inhibit
AHB
0007 0000H
Flash memory
(1024+64) KB
0018 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
GDC control +
External area (96MB)
AHB
0640 0000H
Access inhibit
8000 0000H
FFFF FFFFH

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000440_H	ICR00 [R/W] B, H, W ---11111	ICR01 [R/W] B, H, W ---11111	ICR02 [R/W] B, H, W ---11111	ICR03 [R/W] B, H, W ---11111	Interrupt controller [S]
000444_H	ICR04 [R/W] B, H, W ---11111	ICR05 [R/W] B, H, W ---11111	ICR06 [R/W] B, H, W ---11111	ICR07 [R/W] B, H, W ---11111	
000448_H	ICR08 [R/W] B, H, W ---11111	ICR09 [R/W] B, H, W ---11111	ICR10 [R/W] B, H, W ---11111	ICR11 [R/W] B, H, W ---11111	
$00044C_H$	ICR12 [R/W] B, H, W ---11111	ICR13 [R/W] B, H, W ---11111	ICR14 [R/W] B, H, W ---11111	ICR15 [R/W] B, H, W ---11111	
000450_H	ICR16 [R/W] B, H, W ---11111	ICR17 [R/W] B, H, W ---11111	ICR18 [R/W] B, H, W ---11111	ICR19 [R/W] B, H, W ---11111	
000454_H	ICR20 [R/W] B, H, W ---11111	ICR21 [R/W] B, H, W ---11111	ICR22 [R/W] B, H, W ---11111	ICR23 [R/W] B, H, W ---11111	
000458_H	ICR24 [R/W] B, H, W ---11111	ICR25 [R/W] B, H, W ---11111	ICR26 [R/W] B, H, W ---11111	ICR27 [R/W] B, H, W ---11111	
$00045C_H$	ICR28 [R/W] B, H, W ---11111	ICR29 [R/W] B, H, W ---11111	ICR30 [R/W] B, H, W ---11111	ICR31 [R/W] B, H, W ---11111	
000460_H	ICR32 [R/W] B, H, W ---11111	ICR33 [R/W] B, H, W ---11111	ICR34 [R/W] B, H, W ---11111	ICR35 [R/W] B, H, W ---11111	
000464_H	ICR36 [R/W] B, H, W ---11111	ICR37 [R/W] B, H, W ---11111	ICR38 [R/W] B, H, W ---11111	ICR39 [R/W] B, H, W ---11111	
000468_H	ICR40 [R/W] B, H, W ---11111	ICR41 [R/W] B, H, W ---11111	ICR42 [R/W] B, H, W ---11111	ICR43 [R/W] B, H, W ---11111	
$00046C_H$	ICR44 [R/W] B, H, W ---11111	ICR45 [R/W] B, H, W ---11111	ICR46 [R/W] B, H, W ---11111	ICR47 [R/W] B, H, W ---11111	
000470_H to $00047C_H$	—	—	—	—	Reserved [S]
000480_H	RSTRR [R] B, H, W XXXX--XX	RSTCR [R/W] B, H, W 111----0	STBCR [R/W] B, H, W *3 000---11	—	Reset control [S] Power consumption control [S] *3: Writing to STBCR by DMA is disabled
000484_H	—	—	—	—	Reserved [S]
000488_H	DIVR0 [R/W] B, H, W 000-----	DIVR1 [R/W] B, H, W 0001----	DIVR2 [R/W] B, H, W 0011----	—	Clock control [S]
$00048C_H$	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002100_H	CTRLR1 [R/W] B,H,W -------- 000-0001		STATR1[R/W] B,H,W -------- 00000000		CAN1 (32msg)
002104_H	ERRCNT1 [R] B,H,W 00000000 00000000		BTR1[R/W] B,H,W -0100011 00000001		
002108_H	INTR1 [R] B,H,W 00000000 00000000		TESTR1[R/W] B,H,W -------- X00000--		
$00210C_H$	BRPER1 [R/W] B,H,W -------- ----0000		—		
002110_H	IF1CREQ1 [R/W] B,H,W 0------- 00000001		IF1CMSK1 [R/W] B,H,W -------- 00000000		
002114_H	IF1MSK21 [R/W] B,H,W 11-11111 11111111		IF1MSK11 [R/W] B,H,W 11111111 11111111		
002118_H	IF1ARB21 [R/W] B,H,W 00000000 00000000		IF1ARB11 [R/W] B,H,W 00000000 00000000		
$00211C_H$	IF1MCTR1 [R/W] B,H,W 00000000 0---0000		—		
002120_H	IF1DTA11 [R/W] B,H,W 00000000 00000000		IF1DTA21 [R/W] B,H,W 00000000 00000000		
002124_H	IF1DTB11 [R/W] B,H,W 00000000 00000000		IF1DTB21 [R/W] B,H,W 00000000 00000000		
002128_H, $00212C_H$	Reserved				
002130_H, 002134_H	Reserved (IF1 data mirror)				
002138_H, $00213C_H$	Reserved				
002140_H	IF2CREQ1 [R/W] B,H,W 0------- 00000001		IF2CMSK1 [R/W] B,H,W -------- 00000000		
002144_H	IF2MSK21 [R/W] B,H,W 11-11111 11111111		IF2MSK11 [R/W] B,H,W 11111111 11111111		
002148_H	IF2ARB21 [R/W] B,H,W 00000000 00000000		IF2ARB11 [R/W] B,H,W 00000000 00000000		

10. Interrupt Vector Table

This list shows the assignments of interrupt factors and interrupt vectors/interrupt control registers.

■ Interrupt vector

Interrupt Factor	Interrupt Number		Interrupt Level	Offset	Default Address for TBR	RN[*1]
	Decimal	Hexa-Decimal				
Reset	0	00	-	$3FC_H$	$000FFFFC_H$	-
System reserved	1	01	-	$3F8_H$	$000FFFF8_H$	-
System reserved	2	02	-	$3F4_H$	$000FFFF4_H$	-
System reserved	3	03	-	$3F0_H$	$000FFFF0_H$	-
System reserved	4	04	-	$3EC_H$	$000FFFEC_H$	-
FPU exception	5	05	-	$3E8_H$	$000FFFE8_H$	-
Exception of instruction access protection violation	6	06	-	$3E4_H$	$000FFFE4_H$	-
Exception of data access protection violation	7	07	-	$3E0_H$	$000FFFE0_H$	-
Data access error interrupt	8	08	-	$3DC_H$	$000FFFDC_H$	-
INTE instruction	9	09	-	$3D8_H$	$000FFFD8_H$	-
Instruction break	10	0A	-	$3D4_H$	$000FFFD4_H$	-
System Reserved	11	0B	-	$3D0_H$	$000FFFD0_H$	-
System Reserved	12	0C	-	$3CC_H$	$000FFFCC_H$	-
System Reserved	13	0D	-	$3C8_H$	$000FFFC8_H$	-
Exception of invalid instruction	14	0E	-	$3C4_H$	$000FFFC4_H$	-
NMI request/ XBS RAM double-bit error generation/ AHB RAM double-bit error generation[**]/ Backup RAM double-bit error generation	15	0F	15 (F_H) Fixed	$3C0_H$	$000FFFC0_H$	-
External interrupt 0-7	16	10	ICR00	$3BC_H$	$000FFFBC_H$	0
External interrupt 8-15	17	11	ICR01	$3B8_H$	$000FFFB8_H$	1
Reload timer 0/1/7[**]/8[**]	18	12	ICR02	$3B4_H$	$000FFFB4_H$	2
Reload timer 2/3/9[**]/10[**]	19	13	ICR03	$3B0_H$	$000FFFB0_H$	3
Multi-function serial interface ch.0 (reception completed)/ Multi-function serial interface ch.0(status)	20	14	ICR04	$3AC_H$	$000FFFAC_H$	4*[2]
Multi-function serial interface ch.0 (transmission completed)	21	15	ICR05	$3A8_H$	$000FFFA8_H$	5
Multi-function serial interface ch.1 (reception completed)/ Multi-function serial interface ch.1(status)	22	16	ICR06	$3A4_H$	$000FFFA4_H$	6*[2]
Multi-function serial interface ch.1 (transmission completed)	23	17	ICR07	$3A0_H$	$000FFFA0_H$	7
LIN-UART2(reception completed)	24	18	ICR08	$39C_H$	$000FFF9C_H$	8
LIN-UART2(transmission completed)	25	19	ICR09	398_H	$000FFF98_H$	9
LIN-UART3(reception completed)	26	1A	ICR10	394_H	$000FFF94_H$	10
LIN-UART3(transmission completed)	27	1B	ICR11	390_H	$000FFF90_H$	11
LIN-UART4(reception completed)	28	1C	ICR12	$38C_H$	$000FFF8C_H$	12
LIN-UART4(transmission completed)	29	1D	ICR13	388_H	$000FFF88_H$	13
LIN-UART5(reception completed)	30	1E	ICR14	384_H	$000FFF84_H$	14
LIN-UART5(transmission completed)	31	1F	ICR15	380_H	$000FFF80_H$	15
LIN-UART6(reception completed)	32	20	ICR16	$37C_H$	$000FFF7C_H$	16
LIN-UART6(transmission completed)	33	21	ICR17	378_H	$000FFF78_H$	17
CAN0	34	22	ICR18	374_H	$000FFF74_H$	-
CAN1	35	23	ICR19	370_H	$000FFF70_H$	-
CAN2/UDC0[**]/1[**]	36	24	ICR20	$36C_H$	$000FFF6C_H$	-
Real time clock	37	25	ICR21	368_H	$000FFF68_H$	-

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[*1,*2]	$V_{CC}5$	Vss-0.3	Vss+6.0	V	
	$V_{CC}3$	Vss-0.3	Vss+4.0	V	Vcc3 ≤ Vcc5
	DV_{CC}	Vss-0.3	Vss+6.0	V	DVcc ≤ Vcc5
Analog power supply voltage[*1,*2]	$AV_{CC}5$	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5 ≤ Vcc5
	$AV_{CC}3$	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3 ≤ Vcc3
Analog reference voltage[*1]	AVRH5	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5
	AVR3	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3
Input voltage[*1]	V_{I1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{I2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{I3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Analog pin input voltage[*1]	$V_{IA}5$	Vss-0.3	Vcc5+0.3	V	
	$V_{IA}3$	Vss-0.3	Vcc3+0.3	V	
Output voltage[*1]	V_{O1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{O2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{O3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Maximum clamp current	I_{CLAMP}	-4	4	mA	*9
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	–	20	mA	*9
"L" level maximum output current [*3]	I_{OL1}	–	7	mA	When setting to 2mA[*6]
	I_{OL2}	–	40	mA	When setting to 30mA[*7]
	I_{OL3}	–	30	mA	When setting to 20mA[*8]
"L" level average output current [*4]	I_{OLAV1}	–	2	mA	When setting to 2mA[*6]
	I_{OLAV2}	–	30	mA	When setting to 30mA[*7]
	I_{OLAV3}	–	20	mA	When setting to 20mA[*8]
"L" level total output current [*5]	ΣI_{OL1}	–	50	mA	*6
	ΣI_{OL2}	–	250	mA	*7
	ΣI_{OL3}	–	50	mA	*8
"H" level maximum output current [*3]	I_{OH1}	–	-7	mA	When setting to 2mA[*6]
	I_{OH2}	–	-40	mA	When setting to 30mA[*7]
	I_{OH3}	–	-30	mA	When setting to 20mA[*8]
"H" level average output current [*4]	I_{OHAV1}	–	-2	mA	When setting to 2mA[*6]
	I_{OHAV2}	–	-30	mA	When setting to 30mA[*7]
	I_{OHAV3}	–	-20	mA	When setting to 20mA[*8]
"H" level total output current [*5]	ΣI_{OH1}	–	-50	mA	*6
	ΣI_{OH2}	–	-250	mA	*7
	ΣI_{OH3}	–	-50	mA	*8
Power consumption	P_D	–	1250	mW	LQFP product
		–	2500	mW	BGA product TEQFP product HQFP product
Operating temperature	T_A	-40	+105	°C	*10
Storage temperature	Tstg	-55	+150	°C	

[*1]: These parameters are based on the condition that V_{SS}=AV_{SS}=DV_{SS}=0.0V

[*2]: Caution must be taken that $AV_{CC}5$ and DV_{CC} do not exceed $V_{CC}5$.Similarly,$AV_{CC}3$ must not exceed $V_{CC}3$.

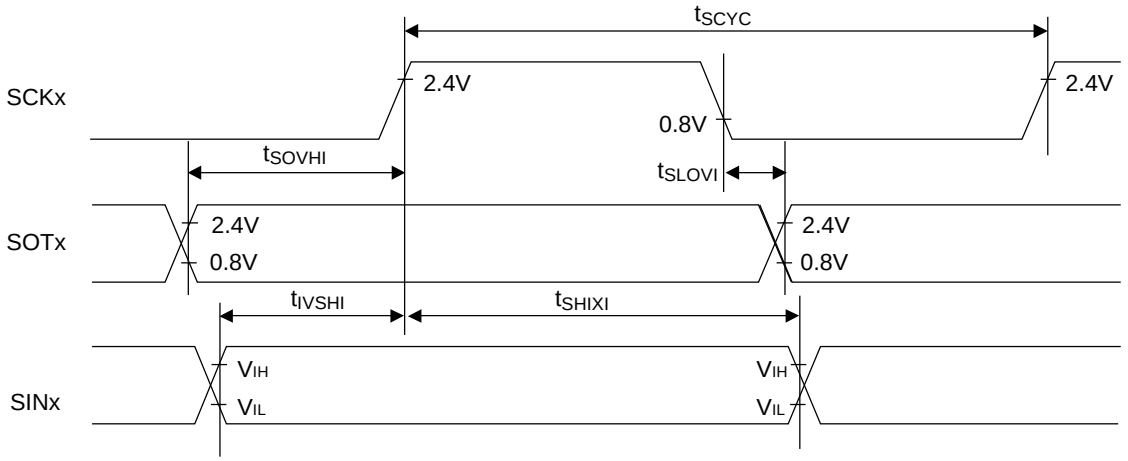
[*3]: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

[*4]: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

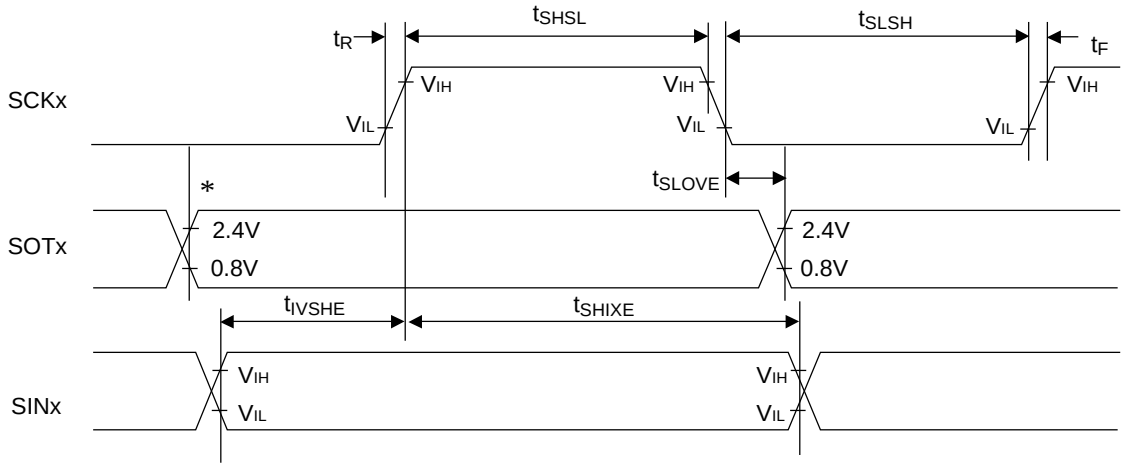
[*5]: The total output current is defined as the maximum current value flowing through all of corresponding pins.

[*6]: Outputs other than P60-P87 and 3V pin.

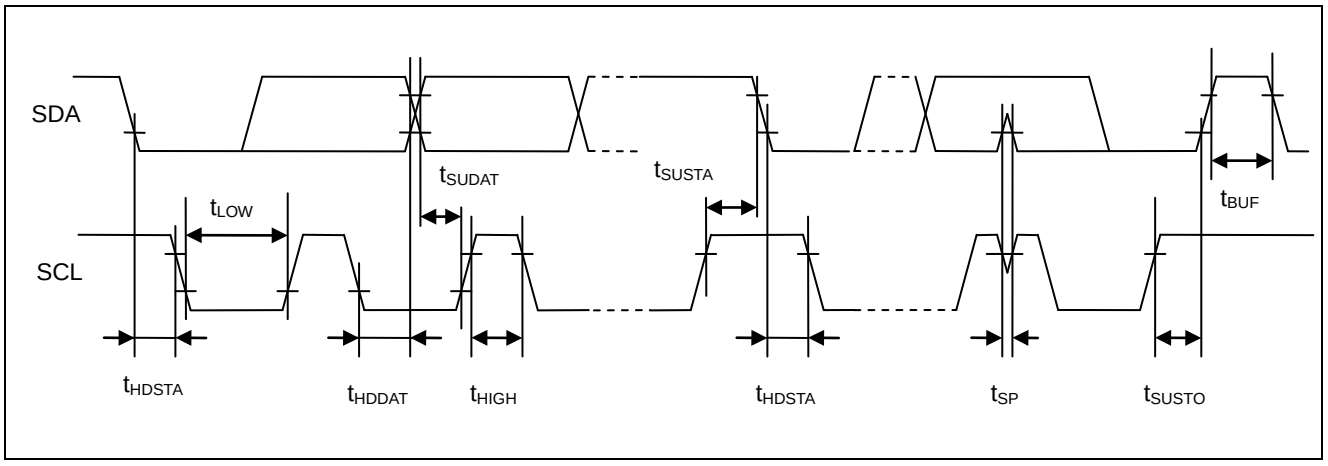
• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



***: Changes when Writing to TDR Register**


SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

11.4.1.5 LIN-UART timing

■Bit setting: ESCR: SCES=0, ECCR: SCDE=0

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF + 1 · TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
Serial clock "L" pulse width	t_{SLSH}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80pF + 1 · TTL
Serial clock "H" pulse width	t_{SHSL}			t_{CPP}+10	–	ns	
SCK ↓ → SOT delay time	t_{SLOVE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		30	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

11.4.1.10 Low voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC	–	–	–	1.3	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		–	–	–	50	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	

*: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.4.1.12 External memory interface

Memory Controller

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip Select delay time	t_{cso}	MEM_XCS0, MEM_XCS1	12pF/10mA	–	18	ns	*1
				–	14	ns	*2
Address delay time	t_{ao}	MEM_EA[24:0]		–	18	ns	*1
				–	14	ns	*2
Data output delay time	t_{do}	MEM_ED[15:0]		–	18	ns	*1
				–	17	ns	*2
Data output → HiZ time	t_{doz}			–	18	ns	*1
				–	17	ns	*2
NOR Flash data setup time	t_{dsr}			20	–	ns	*1
				11	–	ns	*2
NOR Flash data hold time	t_{dhr}			0	–	ns	*1
				0	–	ns	*2
NOR Flash page Read data setup time	t_{dsp}			20	–	ns	*1
				8.5	–	ns	*2
NOR Flash page Read data hold time	t_{dhp}			0	–	ns	*1
				0	–	ns	*2
XRD delay time	t_{rdo}	MEM_XRD		–	18	ns	*1
				–	14	ns	*2
XWR delay time	t_{wro}	MEM_XWR		–	18	ns	*1
				–	14	ns	*2

Output delay is reference clock is an internal clock. The reference clock of MEM_RDY is an internal clock.

*1: MB91F591/2/4/6/7/9

*2: MB91F59A/B

■AC Timing Parameters

This section describes parameters used for AC timing specifications. Select whether you use the DCLKO reverse edge mode, depending on the use/non-use of delay mode.

When the delay mode is not used:
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

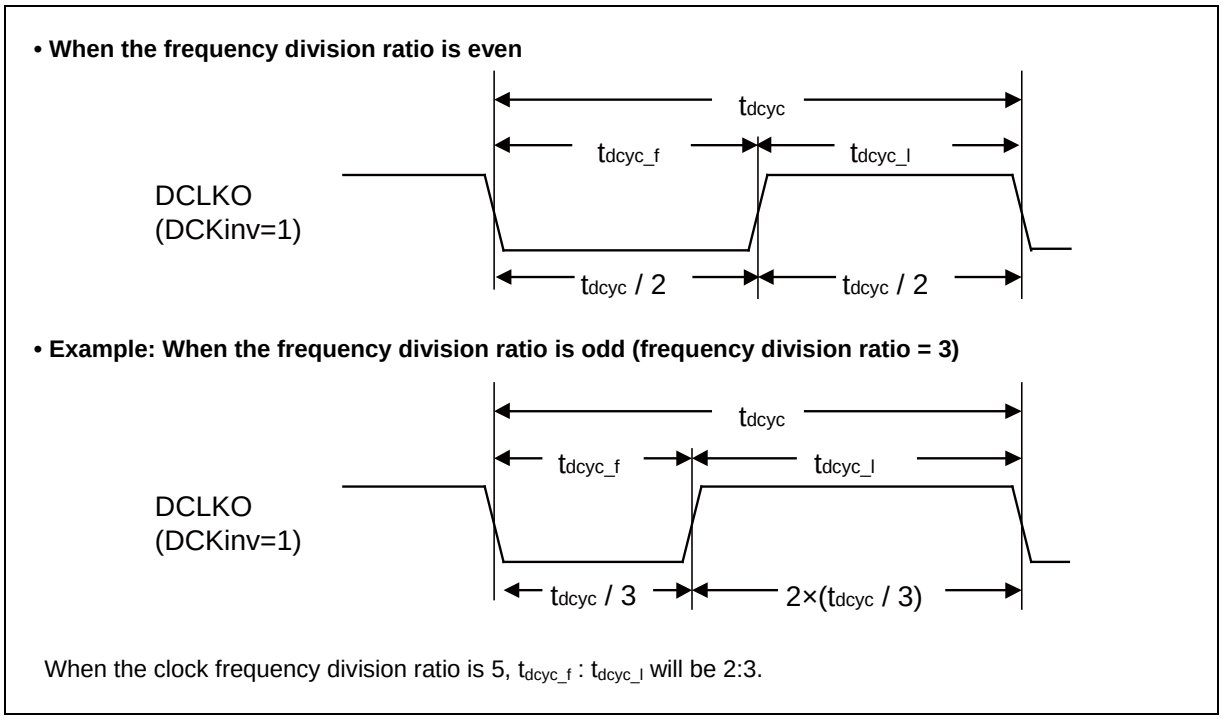
When the delay mode is used:
Use the DCLKO standard mode when the external display device (TFT) receives the signal at the rising edge of DCLKO.
Use the DCLKO reverse edge mode when the external display device (TFT) receives the signal at the falling edge of DCLKO.

Note: Clock duty ratio when the clock frequency division ratio is even or odd

AC specifications use the half-cycle of the display output clock DCLKO as a parameter. In AC specifications, the first half-cycle is indicated as t_{dcyc_f}, and the second half-cycle is indicated as t_{dcyc_l}.

Note that clock duty ratio will not be 50%:50% when the clock frequency division ratio (specified in SC field of DCM1 register) is odd. If the clock frequency division ratio is odd, the first half-cycle t_{dcyc_f} becomes different from the second half-cycle t_{dcyc_l}.

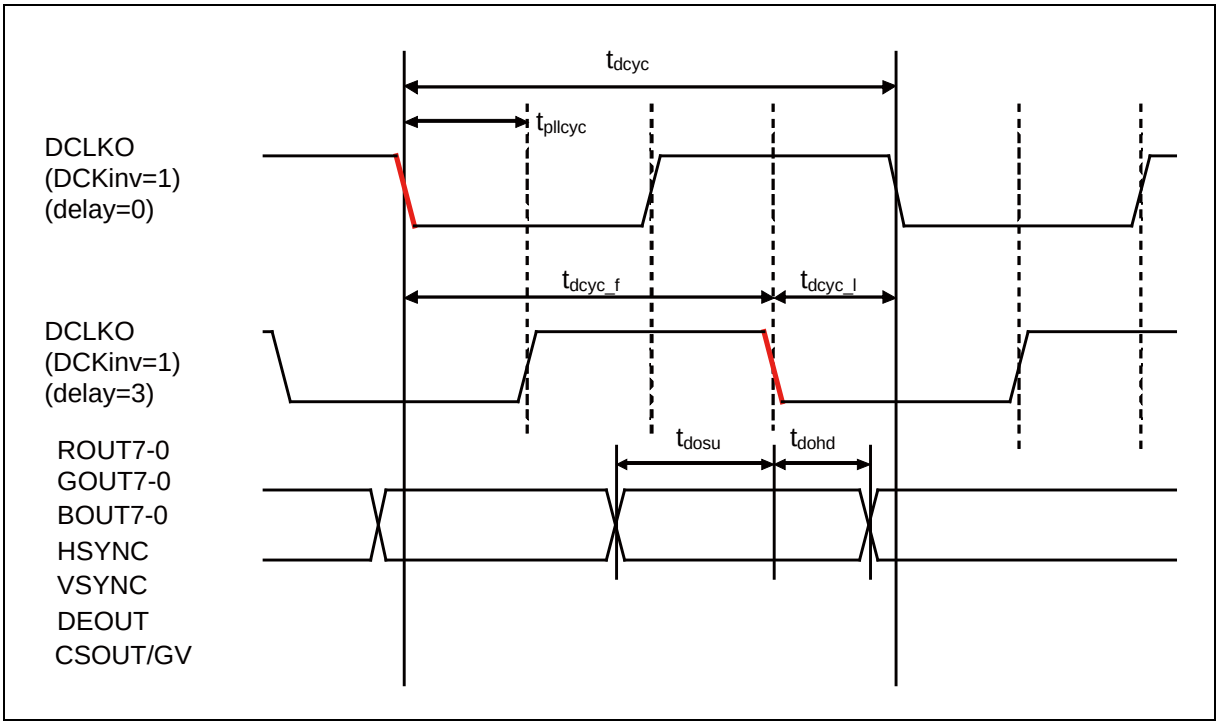
Figure 2. Clock Duty Ratio when the Clock Frequency Division Ratio is even or Odd



Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

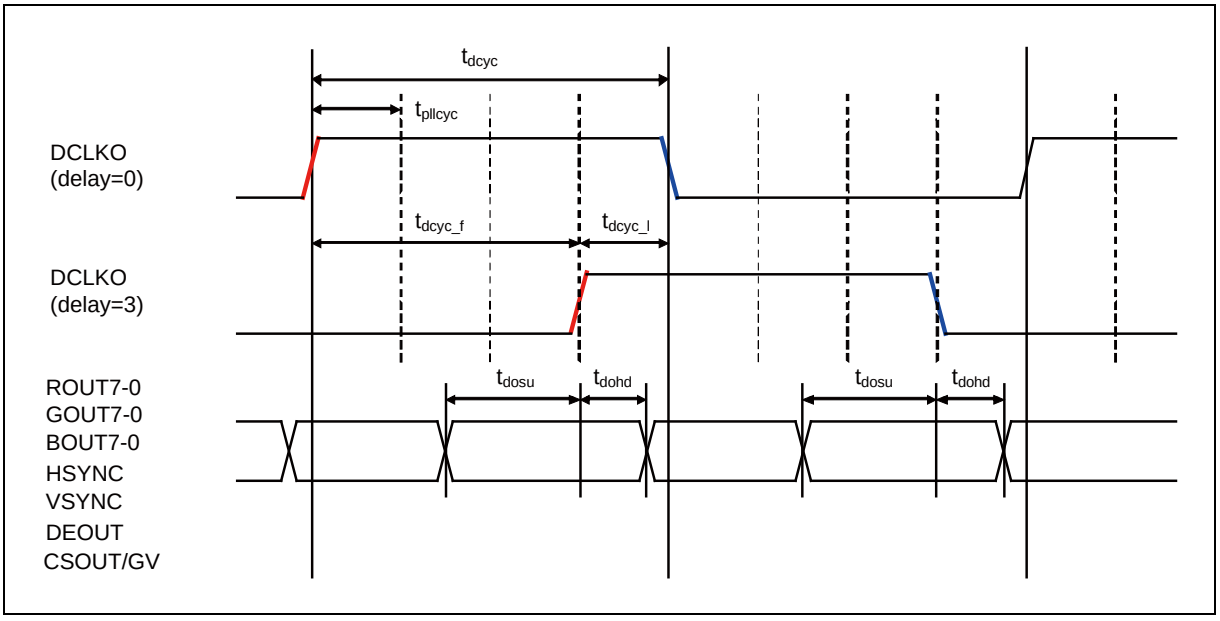
Figure 6. Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

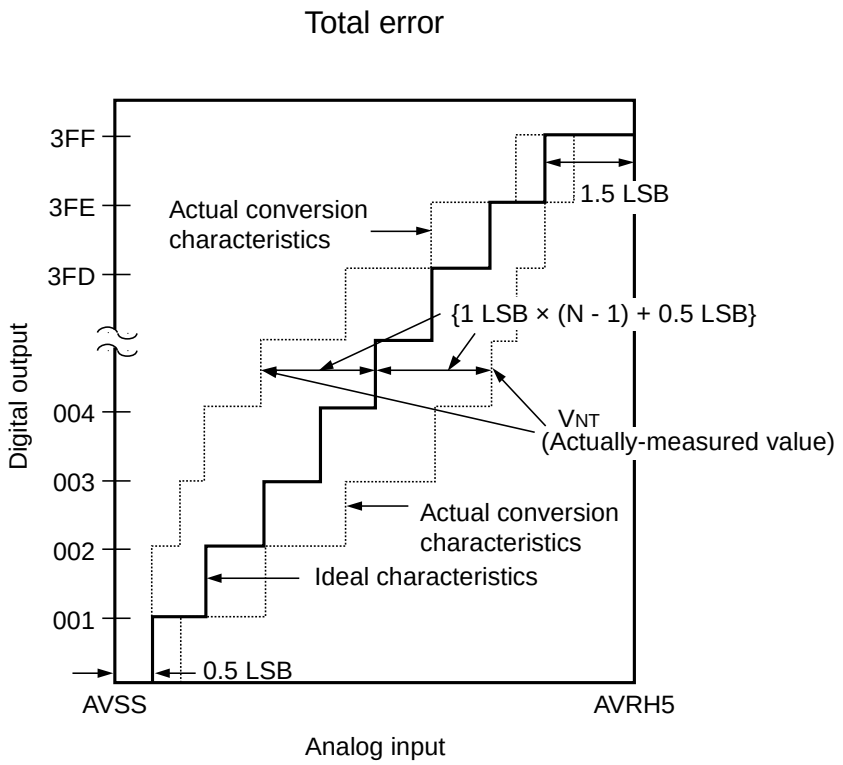
Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



11.5.2 Definition of A/D Converter Terms

Resolution	:	Analog variation that is recognized by an A/D converter.
Non linearity error	:	Deviation of the actual conversion characteristics from a straight line that connects the zero transition point ("00 0000 0000"← →"00 0000 0001") to the full-scale transition point ("111111 1110"← →"11 1111 1111").
Differential linearity error	:	Deviation of the input voltage from the ideal value that is required to change the output code by LSB.
Total error	:	Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error, and non linearity error.



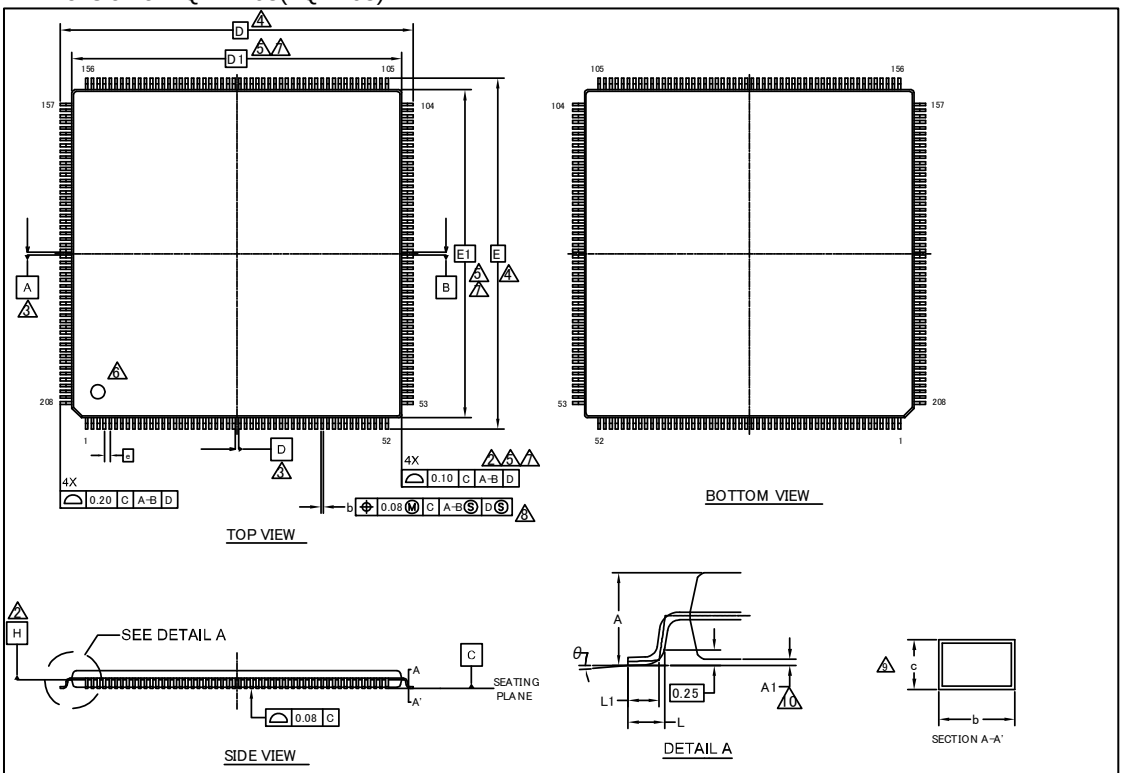
$$\text{Total error of digital output N} = \frac{V_{NT} - \{1LSB\} \times (N - 1) + 0.5LSB\}}{1LSB} \text{ [LSB]}$$

$$1LSB \text{ (Ideal value)} = \frac{AVRH5 - AVSS}{1024} \text{ [V]}$$

N: A/D converter digital output value.
V_{OT} (Ideal value) = AVSS + 0.5 LSB[V]
V_{FST} (Ideal value) = AVRH5 - 1.5 LSB[V]
V_{NT}: Voltage at which the digital output changes from (N - 1) to N.

13. Package Dimensions

■Dimension of LQFP-208(LQR208)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.00 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15151 **

PACKAGE OUTLINE, 208 LEAD LQFP
28.0X28.0X1.7 MM LQR208 REV**