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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	308K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f591bhspmc-gsk5e1

- Multi-function serial communication (built-in transmission/reception FIFO memory) :
  - 2 channels for MB91F591/2/4/6/7/9
  - 6 channels for MB91F59A/B

  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detect functions provided
  - DMA transfer support

  <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 9-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detect function is provided
  - DMA transfer support

  <LIN-UART (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - LIN protocol Revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support

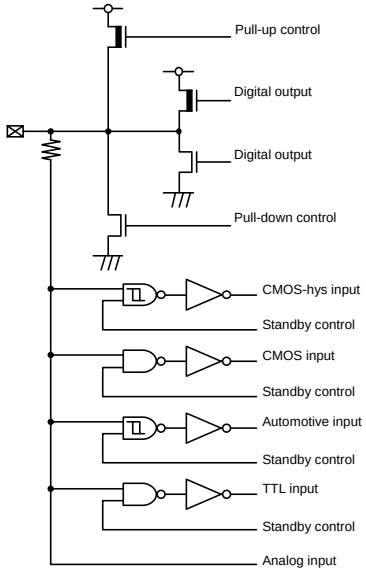
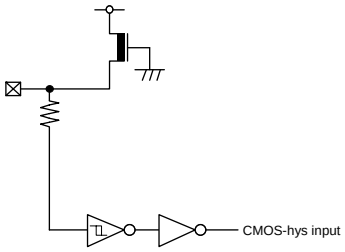
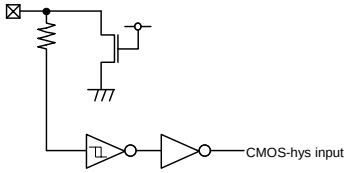
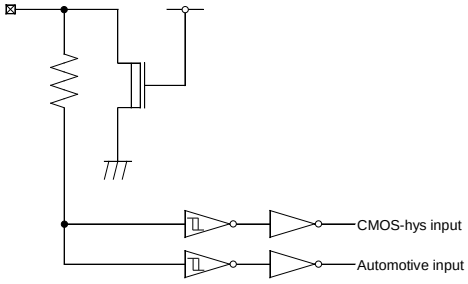
  < I^2C >
  - ch.0 and ch.1 only supported
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (C-CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 64-transmission/reception message buffering : 1 channel, 32-transmission/reception message buffering : 2 channels
- Up/down counter: 16-bit × 3 channels for MB91F59A/B
- PPG : 16-bit × 24 channels
- Reload timer :
  - 16-bit × 4 channels for MB91F591/2/4/6/7/9
  - 16-bit × 8 channels for MB91F59A/B
- Free-run timer :
  - 32-bit × 2 channels (Can select each channel for input capture, output compare) for MB91F591/2/4/6/7/9
  - 32-bit × 2 channels (LSYN (LIN synch field detection) for exclusive input capture) for MB91F591/2/4/6/7/9
  - 32-bit × 8 channels (Can select ch.0, 1, 2, and 3 for input capture, output compare) for MB91F59A/B
- Input capture :
  - 32-bit × 6 channels (linked to the free-run timer) for MB91F591/2/4/6/7/9
  - 32-bit × 2 channels (linked to the free-run timer) LSYN (LIN synch field detected) Exclusive for MB91F591/2/4/6/7/9
  - 32-bit × 12 channels (linked to the free-run timer) LSYN (LIN synch field detected) for MB91F59A/B
- Output compare : 32-bit × 4 channels (linked to the free-run timer)
- Sound generator : 5 channels
  - Frequency and amplitude sequencers provided
- Stepping motor controller : 6 channels
  - 8/10-bit PWM
  - High current output supported (4 lines × 6 channels)
  - Can refer back electromotive force using pin-shared A/D converter
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main/sub oscillation frequency can be selected for the operation clock (dual product only)
- Calibration: The hardware watchdog for CR oscillation drive and real-time clock (RTC) for sub clock drive (dual product only)
  - The CR oscillation frequency can be trimmed
  - The main clock to sub clock (dual product only) ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32kHz) (two system clock kinds) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
- Base timer : 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
126, 136, 146, 156	DVCC	–	–	SMC large current port power supply pin
125, 135, 145, 155	DVSS	–	–	SMC large current port GND pin
89, 105, 122, 173	VCC5	–	–	+5.0V power supply pin
1, 18, 37, 53, 71, 175, 189	VCC3	–	–	+3.3V power supply pin
19, 36, 52, 72, 82, 88, 104, 123, 170, 174, 188, 208	VSS	–	–	GND pin

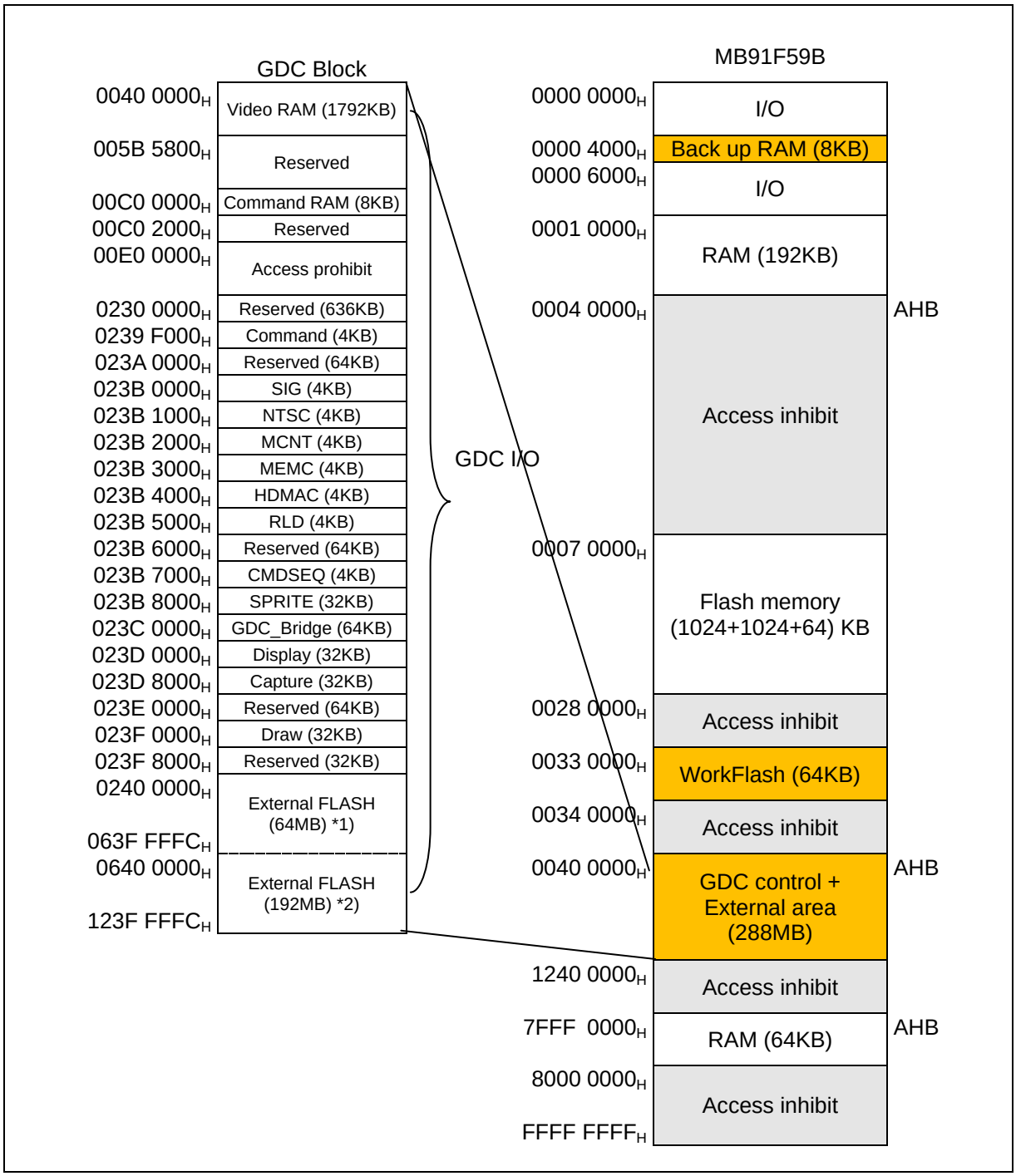
[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
177	P134	–	A	General-purpose I/O port
	ICU5			Input capture ch.5 input pin
	INT5			INT5 External interrupt input pin
	PPG1_3			PPG ch.1 output pin (3)
177	TRG2			PPG trigger 2 input pin (ch.8 to ch.11)
	TOT10			Reload timer ch.10 output pin
178	TIOB0	–	K	Base timer TIOB0 input pin
	P132			General-purpose I/O port
	ICU3			Input capture ch.3 input pin
	INT2			INT2 External interrupt input pin
	SOT1			Multi-function serial ch.1 serial data output pin / I^2C ch.1 serial data I/O pin
	TOT8			Reload timer ch.8 output pin
179	TIOA0	–	K	Base timer TIOA0 output pin
	P130			General-purpose I/O port
	ICU1			Input capture ch.1 input pin
	INT0			INT0 External interrupt input pin
	SCK0			Multi-function serial ch.0 clock I/O pin / I^2C ch.0 clock I/O pin
180	P127	–	K	General-purpose I/O port
	SOT0			Multi-function serial ch.0 serial data output pin / I^2C ch.0 serial data I/O pin
181	RSTX	N	F1	External reset input pin
182	RDY	–	O	External bus · Wait input pin
	P057			General-purpose I/O port (3V pin)
183	A20	–	O	External bus · Address bit20 output pin
	P052			General-purpose I/O port(3V pin)
184	A19	–	O	External bus · Address bit19 output pin
	P051			General-purpose I/O port(3V pin)
185	A18	–	O	External bus · Address bit18 output pin
	P050			General-purpose I/O port (3V pin)
186	A13	–	O	External bus · Address bit13 output pin
	P043			General-purpose I/O port (3V pin)
	QSPI_CS0			HS_SPI SSEL0 Output pin
187	A10	–	O	External bus · Address bit10 output pin
	P040			General-purpose I/O port (3V pin)
	QSPI_SIO1			HS_SPI SDATA1 I/O pin
188	A07	–	O	External bus · Address bit7 output pin
	P035			General-purpose I/O port (3V pin)
189	A03	–	O	External bus · Address bit3 output pin
189	P031	–	O	General-purpose I/O port (3V pin)
190	VSS	–	–	GND pin
191	P024	–	O	General-purpose I/O port (3V pin)
192	CS0X	–	O	External bus · Chip select 0 output pin
	P021			General-purpose I/O port (3V pin)
193	BOUT1	–	O	Display digital B1 output pin
	D14			External bus · Data bit14 I/O pin
	P016			General-purpose I/O port (3V pin)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
194	ROUT1	–	O	Display digital R1 output pin
	D10			External bus · Data bit10 I/O pin
	P012			General-purpose I/O port (3V pin)
195	D5	–	O	External bus · Data bit5 I/O pin
	P005			General-purpose I/O port (3V pin)
	SCK3_1			LIN-UART ch.3 clock I/O pin (1)
	PPG5			PPG ch.5 output pin
	TOT1_2			Reload timer ch.1 output pin (2)
196	D2	–	O	External bus · Data bit2 I/O pin
	P002			General-purpose I/O port (3V pin)
	SCK2_1			LIN-UART ch.2 clock I/O pin (1)
	PPG2			PPG ch.2 output pin
	TIN2_2			Reload timer ch.2 event input pin (2)
197	DEOUT	P	O	Display enable display period output pin
	PG7	–		General-purpose I/O port (3V pin)
198	HSYNC	–	O	Display horizontal sync signal output pin (for Internal sync)/ Display horizontal sync signal input pin (for External sync)
	PG6			General-purpose I/O port (3V pin)
199	BOUT6	–	O	Display digital B6 output pin
	PF6			General-purpose I/O port (3V pin)
200	BOUT2	–	O	Display digital B2 output pin
	PF2			General-purpose I/O port (3V pin)
201	GOUT5	–	O	Display digital G5 output pin
	PE5			General-purpose I/O port (3V pin)
202	GOUT2	–	O	Display digital G2 output pin
	PE2			General-purpose I/O port (3V pin)
203	ROUT5	–	O	Display digital R5 output pin
	PD5			General-purpose I/O port (3V pin)
204	ROUT2	–	O	Display digital R2 output pin
	PD2			General-purpose I/O port (3V pin)
205	VSS	–	–	GND pin
206	CCLK	–	O	For capture, capture clock input pin
	PH3			General-purpose I/O port (3V pin)
207	VSIN	P	O	Capture vertical sync signal input pin
	PG1	–		General-purpose I/O port (3V pin)
208	VCC3	–	–	+3.3V power supply pin
209	VSS	–	–	GND pin
210	VSS	–	–	GND pin
211	VCC3	–	–	+3.3V power supply pin
212	VCC3	–	–	+3.3V power supply pin
213	VSS	–	–	GND pin
214	VCC5	–	–	+5.0V power supply pin
215	FRCK2	–	C	Free-run timer 2 clock input pin
	P117			General-purpose I/O port
	SCK4			LIN-UART ch.4 clock I/O pin
	TRG4			PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0			Reload timer ch.0 output pin
	SGO3			Sound generator ch.3 SGO output pin

Type	Circuit	Remarks
E		• Analog input, General-purpose I/O port • Output 1mA,2mA,30mA (large current for SMC) • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input
F1		• Schmitt input • Pull-up resistor control 50kΩ (5V cont)
F2		• Schmitt input • Pull-down resistor control 50kΩ (5V cont)
F3		• Schmitt input • Automotive input • Pull-down resister control 50kΩ (5V cont)

■GDC memory map

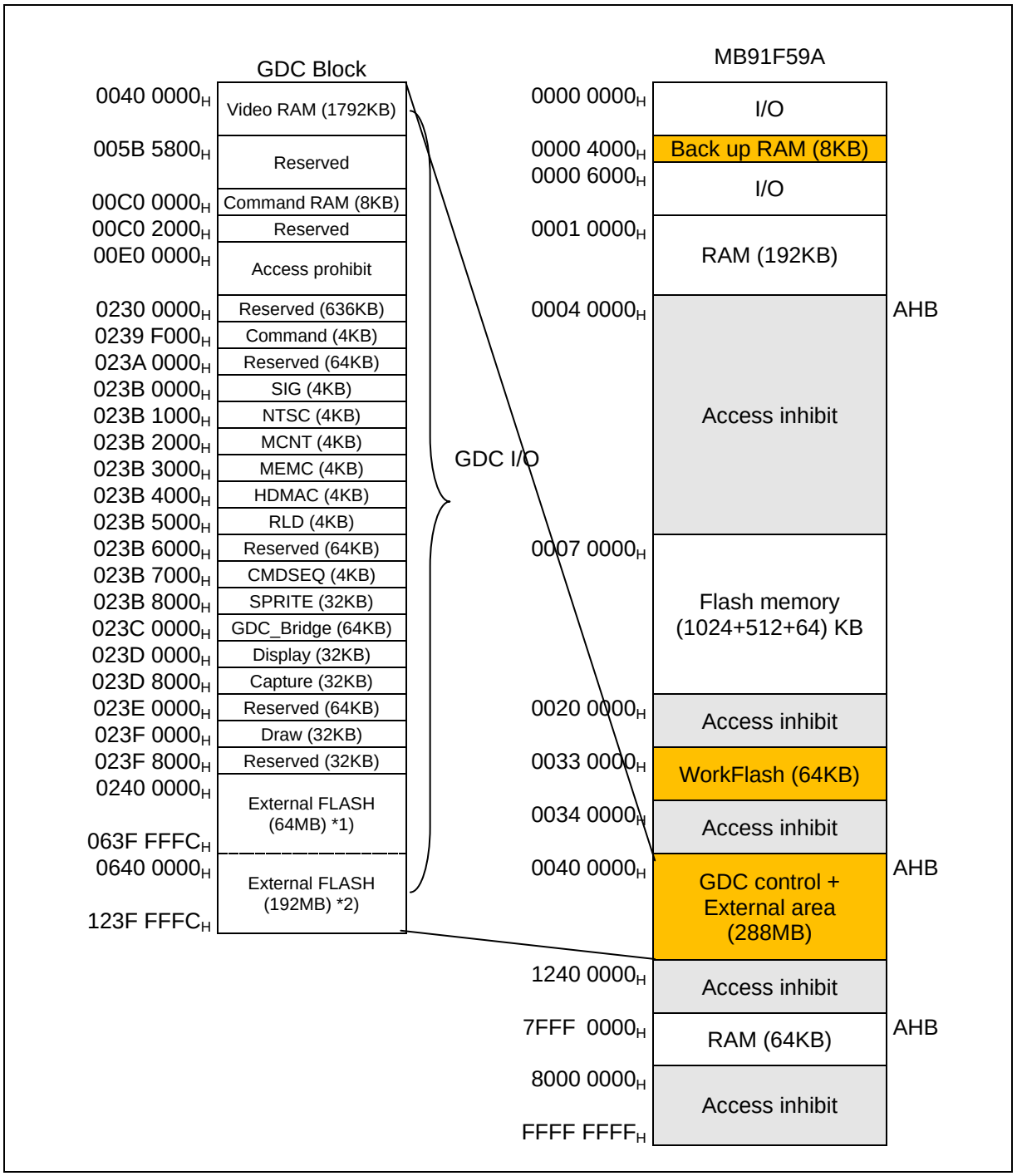


Note: The GDC area is executed mapping with the little endian.

*1) Parallel interface supports 64MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192MB of memory space from 0640_0000H to 123F_FFFFH.
(HS-SPI totally supports 256MB of memory space from 0240_0000H to 123F_FFFFH for External FLASH)

■GDC memory map



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*1) Parallel interface supports 64MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192MB of memory space from 0640_0000H to 123F_FFFCH.
(HS-SPI totally supports 256MB of memory space from 0240_0000H to 123F_FFFCH for External FLASH)

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -0000000 00000000		Base timer 1
000094_H	—	BT1STC [R/W] B 0000-000	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base timer 0,1
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	
$0000AC_H$	—	—	—	—	Reserved
$0000B0_H$	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-function serial 0 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000B4_H$	RDR0/(TDR0)[R/W] B,H,W *1 -------0 00000000		BGR0 [R/W] H,W 00000000 00000000		
$0000B8_H$	— / (ISMK0) [R/W] B,H,W -------- *2	— / (ISBA0) [R/W] B,H,W -------- *2	—	—	
$0000BC_H$	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	
$0000C0_H$	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-function serial 1 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000C4_H$	RDR1/(TDR1)[R/W] B,H,W *1 -------0 00000000		BGR1 [R/W] H,W 00000000 00000000		
$0000C8_H$	— / (ISMK1) [R/W] B,H,W -------- *2	— /(ISBA1) [R/W] B,H,W -------- *2	—	—	
$0000CC_H$	FCR11 [R/W] B, H, W ---00100	FCR01[R/W] B, H, W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
$0000D0_H$	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
$0000D4_H$	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
$0000D8_H$	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
$0000DC_H$	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$0001C0_H$	TMRLRA8 [R/W] H XXXXXXXX XXXXXXXX		TMR8 [R] H XXXXXXXX XXXXXXXX		Reload timer 8 MB91F59A/B only
$0001C4_H$	TMRLRB8 [R/W] H XXXXXXXX XXXXXXXX		TMCSR8 [R/W] B, H,W 00000000 0-000000		
$0001C8_H$	TMRLRA9 [R/W] H XXXXXXXX XXXXXXXX		TMR9 [R] H XXXXXXXX XXXXXXXX		Reload timer 9 MB91F59A/B only
$0001CC_H$	TMRLRB9 [R/W] H XXXXXXXX XXXXXXXX		TMCSR9 [R/W] B, H,W 00000000 0-000000		
$0001D0_H$	TMRLRA10 [R/W] H XXXXXXXX XXXXXXXX		TMR10 [R] H XXXXXXXX XXXXXXXX		Reload timer 10 MB91F59A/B only
$0001D4_H$	TMRLRB10 [R/W] H XXXXXXXX XXXXXXXX		TMCSR10 [R/W] B, H,W 00000000 0-000000		
$0001D8_H$ to $0001DC_H$	—	—	—	—	Reserved
$0001E0_H$	SCR10 [R/W] B,H,W 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R/W] B,H,W 0-000011	ESCR10 [R/W] B,H,W -0000000	Multi-function serial 10 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001E4_H$	RDR10/(TDR10)[R/W] B,H,W *1 -------0 00000000		BGR10 [R/W] H,W 00000000 00000000		
$0001E8_H$	—	—	—	—	
$0001EC_H$	FCR110 [R/W] B,H,W ---00100	FCR010 [R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
$0001F0_H$	SCR11 [R/W] B,H,W 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R/W] B,H,W 0-000011	ESCR11 [R/W] B,H,W -0000000	Multi-function serial 11 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001F4_H$	RDR11/(TDR11)[R/W] B,H,W *1 -------0 00000000		BGR11 [R/W] H,W 00000000 00000000		
$0001F8_H$	—	—	—	—	
$0001FC_H$	FCR111 [R/W] B,H,W ---00100	FCR011 [R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0008A4H	WRDR04[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Wild register [S]
0008A8H	WRAR05[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008ACH	WRDR05[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B0H	WRAR06[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008B4H	WRDR06[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008B8H	WRAR07[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008BCH	WRDR07[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C0H	WRAR08[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008C4H	WRDR08[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008C8H	WRAR09[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008CCH	WRDR09[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D0H	WRAR10[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008D4H	WRDR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008D8H	WRAR11[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008DCH	WRDR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E0H	WRAR12[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008E4H	WRDR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008E8H	WRAR13[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008ECH	WRDR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F0H	WRAR14[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008F4H	WRDR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0008F8H	WRAR15[R/W] W -------- --XXXXXX XXXXXXXX XXXXXX--				
0008FCH	WRDR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000900H to 000BF8H	—	—	—	—	Reserved
000BFCH	—	—	UER [W] B,H,W -------- -------X		OCDU

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
$000E10_H$	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
$000E14_H$	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
$000E18_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
$000E30_H$	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
$000E34_H$	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	
$000E38_H$ to $000E3C_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000EE0_H$	PILR00[R/W] B,H,W 11111111	PILR01[R/W] B,H,W 11111111	PILR02[R/W] B,H,W 11111111	PILR03[R/W] B,H,W 11111111	Port input level selection register
$000EE4_H$	PILR04[R/W] B,H,W 11111111	PILR05[R/W] B,H,W 11111111	PILR06[R/W] B,H,W 11111111	PILR07[R/W] B,H,W 11111111	
$000EE8_H$	PILR08[R/W] B,H,W 11111111	PILR09[R/W] B,H,W 11111111	PILR10[R/W] B,H,W 11111111	PILR11[R/W] B,H,W 11111111	
$000EEC_H$	PILR12[R/W] B,H,W 11111111	PILR13[R/W] B,H,W 11-11111	—	—	
$000EF0_H$	PILRA[R/W] B,H,W 111111--	PILRB[R/W] B,H,W 111111--	PILRC[R/W] B,H,W 111111--	PILRD[R/W] B,H,W 111111--	
$000EF4_H$	PILRE[R/W] B,H,W 111111--	PILRF[R/W] B,H,W 111111--	PILRG[R/W] B,H,W 11111111	PILRH[R/W] B,H,W ----1---	
$000EF8_H$ to $000EFC_H$	—	—	—	—	Reserved
$000F00_H$	—	—	—	—	Extended Port input level selection register
$000F04_H$	—	—	EPILR06[R/W] B,H,W 00000000	EPILR07[R/W] B,H,W 00000000	
$000F08_H$	EPILR08[R/W] B,H,W 00000000	EPILR09[R/W] B,H,W 00000000	EPILR10[R/W] B,H,W 00000000	EPILR11[R/W] B,H,W 00000000	
$000F0C_H$	EPILR12[R/W] B,H,W 00000000	EPILR13[R/W] B,H,W 00-00000	—	—	
$000F10_H$	—	—	—	—	
$000F14_H$	—	—	—	—	
$000F18_H$ to $000F1C_H$	—	—	—	—	Reserved
$000F20_H$	—	—	—	—	Port output drive register
$000F24_H$	—	—	PODR06[R/W] B,H,W 00000000	PODR07[R/W] B,H,W 00000000	
$000F28_H$	PODR08[R/W] B,H,W 00000000	PODR09[R/W] B,H,W 00000000	PODR10[R/W] B,H,W 00000000	PODR11[R/W] B,H,W 00000000	
$000F2C_H$	PODR12[R/W] B,H,W 00000000	PODR13[R/W] B,H,W 00-00000	—	—	
$000F30_H$	—	—	—	—	
$000F34_H$	—	—	—	—	
$000F38_H$	EPODR06[R/W] B,H,W 00000000	EPODR07[R/W] B,H,W 00000000	EPODR08[R/W] B,H,W 00000000	—	Extended Port output drive register
$000F3C_H$	EPODRGD [R/W]B,H,W ----1010	EPODRGF [R/W]B,H,W --101010	—	—	

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[*1,*2]	$V_{CC}5$	Vss-0.3	Vss+6.0	V	
	$V_{CC}3$	Vss-0.3	Vss+4.0	V	Vcc3 ≤ Vcc5
	DV_{CC}	Vss-0.3	Vss+6.0	V	DVcc ≤ Vcc5
Analog power supply voltage[*1,*2]	$AV_{CC}5$	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5 ≤ Vcc5
	$AV_{CC}3$	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3 ≤ Vcc3
Analog reference voltage[*1]	AVRH5	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5
	AVR3	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3
Input voltage[*1]	V_{I1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{I2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{I3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Analog pin input voltage[*1]	$V_{IA}5$	Vss-0.3	Vcc5+0.3	V	
	$V_{IA}3$	Vss-0.3	Vcc3+0.3	V	
Output voltage[*1]	V_{O1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{O2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{O3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Maximum clamp current	I_{CLAMP}	-4	4	mA	*9
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	–	20	mA	*9
"L" level maximum output current [*3]	I_{OL1}	–	7	mA	When setting to 2mA[*6]
	I_{OL2}	–	40	mA	When setting to 30mA[*7]
	I_{OL3}	–	30	mA	When setting to 20mA[*8]
"L" level average output current [*4]	I_{OLAV1}	–	2	mA	When setting to 2mA[*6]
	I_{OLAV2}	–	30	mA	When setting to 30mA[*7]
	I_{OLAV3}	–	20	mA	When setting to 20mA[*8]
"L" level total output current [*5]	ΣI_{OL1}	–	50	mA	*6
	ΣI_{OL2}	–	250	mA	*7
	ΣI_{OL3}	–	50	mA	*8
"H" level maximum output current [*3]	I_{OH1}	–	-7	mA	When setting to 2mA[*6]
	I_{OH2}	–	-40	mA	When setting to 30mA[*7]
	I_{OH3}	–	-30	mA	When setting to 20mA[*8]
"H" level average output current [*4]	I_{OHAV1}	–	-2	mA	When setting to 2mA[*6]
	I_{OHAV2}	–	-30	mA	When setting to 30mA[*7]
	I_{OHAV3}	–	-20	mA	When setting to 20mA[*8]
"H" level total output current [*5]	ΣI_{OH1}	–	-50	mA	*6
	ΣI_{OH2}	–	-250	mA	*7
	ΣI_{OH3}	–	-50	mA	*8
Power consumption	P_D	–	1250	mW	LQFP product
		–	2500	mW	BGA product TEQFP product HQFP product
Operating temperature	T_A	-40	+105	°C	*10
Storage temperature	Tstg	-55	+150	°C	

[*1]: These parameters are based on the condition that V_{SS}=AV_{SS}=DV_{SS}=0.0V

[*2]: Caution must be taken that $AV_{CC}5$ and DV_{CC} do not exceed $V_{CC}5$.Similarly,$AV_{CC}3$ must not exceed $V_{CC}3$.

[*3]: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

[*4]: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

[*5]: The total output current is defined as the maximum current value flowing through all of corresponding pins.

[*6]: Outputs other than P60-P87 and 3V pin.

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

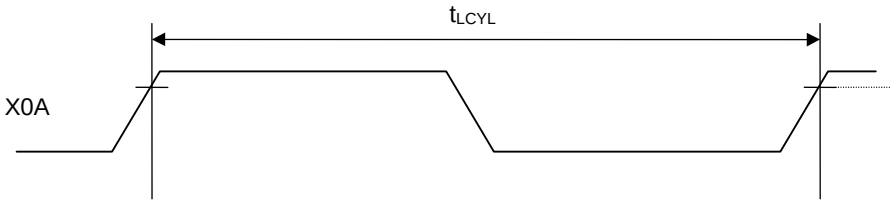
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level input voltage	V_{IL1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	CMOS input level is selected	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL2}		CMOS hysteresis Input level is selected	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL3}		Automotive input level is selected	Vss-0.3	–	0.5× $V_{CC}5$	V	
	V_{IL4}		TTL input level is selected	Vss-0.3	–	0.8	V	
	V_{IL5}	RSTX, NMIX, MD2	–	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL7}	MD0, MD1	–	Vss-0.3	–	0.3× $V_{CC}5$	V	
	V_{IL8}	DEBUGIF	–	Vss-0.3	–	0.8	V	
	V_{IL10}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	CMOS hysteresis input level is selected	Vss-0.3	–	0.3× $V_{CC}3$	V	3.3V dedicated pin
	V_{IL11}		TTL input level is selected	Vss-0.3	–	0.8	V	
	V_{IL12}	MD3	-	V_{SS}-0.3	-	0.3× V_{CC5}	V	BGA product only
	V_{IL13}	TDI, TMS, TRST, TCK	-	V_{SS}-0.3	-	0.3× V_{CC5}	V	BGA product only

11.4.1.1 Sub clock timing (products without s-suffix)

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	–	–	30.52	–	µs	

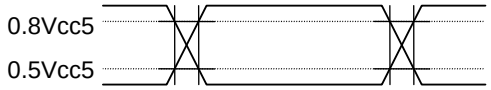
• X0A,X1A Clock Timing



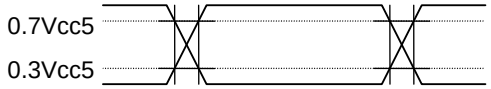
AC characteristics are specified by the following measurement reference voltage values.

• Input Signal Waveform

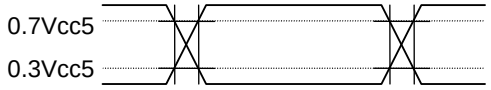
Hysteresis Input Pin (Automotive)



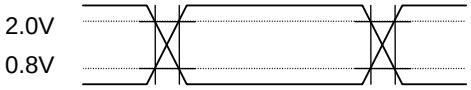
Hysteresis Input Pin (CMOS Normal)



Hysteresis Input Pin (CMOS Hysteresis)

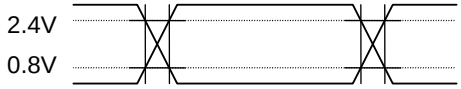


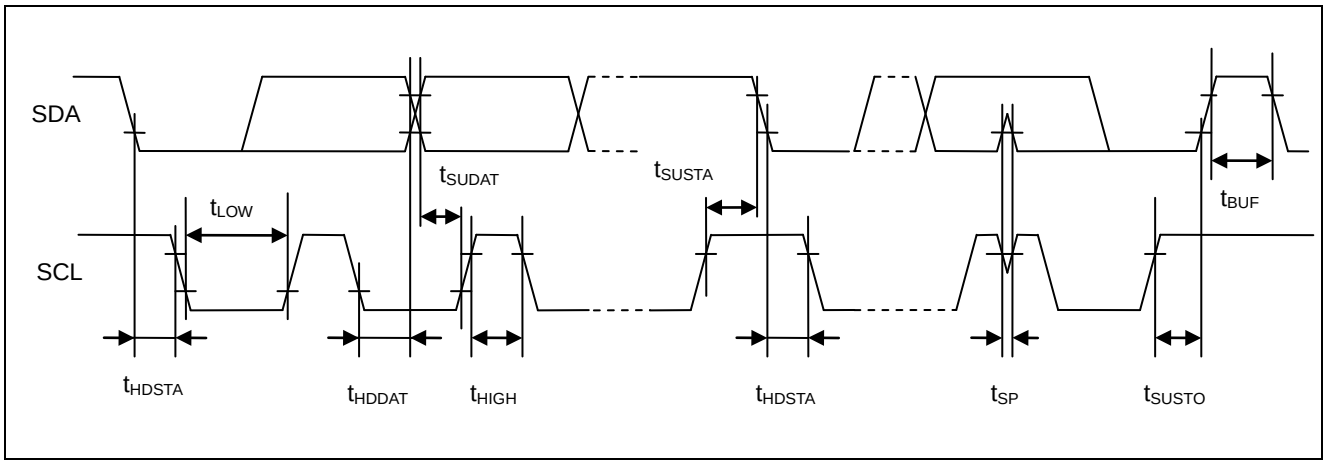
TTL Input Pin



• Output Signal Waveform

Output Pin




SDA
SCL
tLOW
tSUDAT
tSUSTA
tBUF
tHDSTA
tHDDAT
tHIGH
tHDSTA
tSP
tSUSTO

■Bit setting: ESCR: SCES=0, ECCR: SCDE=1

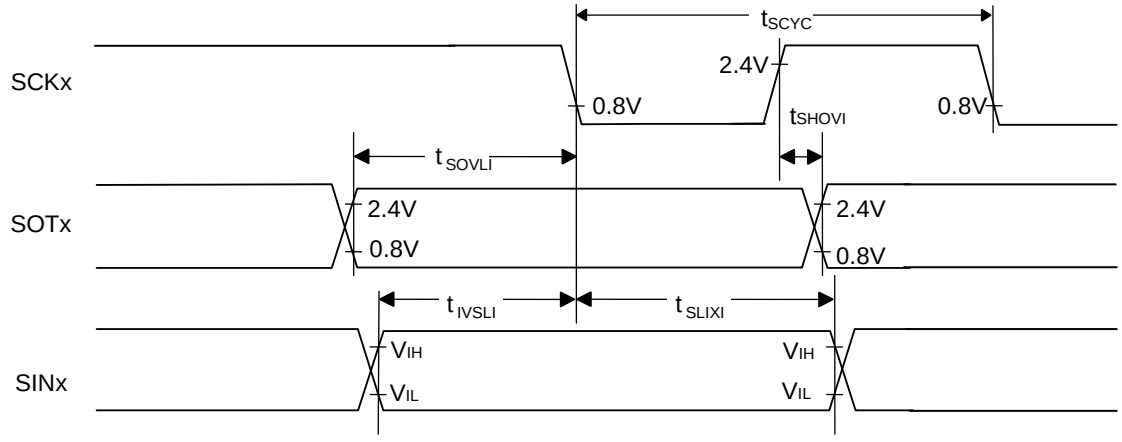
(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		$5t_{CPP}$	–	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5,	–	t_{CPP}+80	–	ns	Internal shift clock Mode: C_L=80pF + 1 • TTL
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		0	–	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• Internal Shift Clock Mode



■Bit setting: ESCR: SCES=1, ECCR: SCDE=1

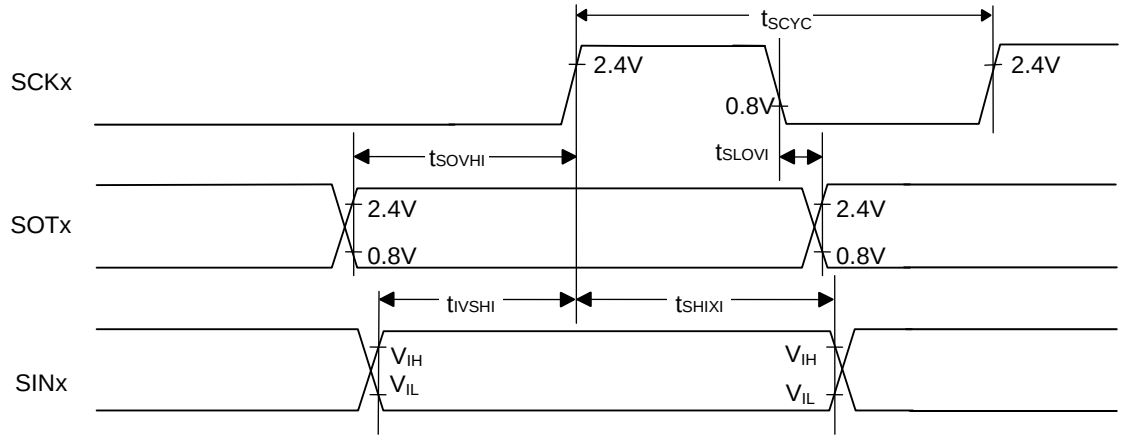
(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1 • TTL
SCK ↓ → SOT delay time	t_{SLOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns	
SOT → SCK ↑ delay time	t_{SOVHI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

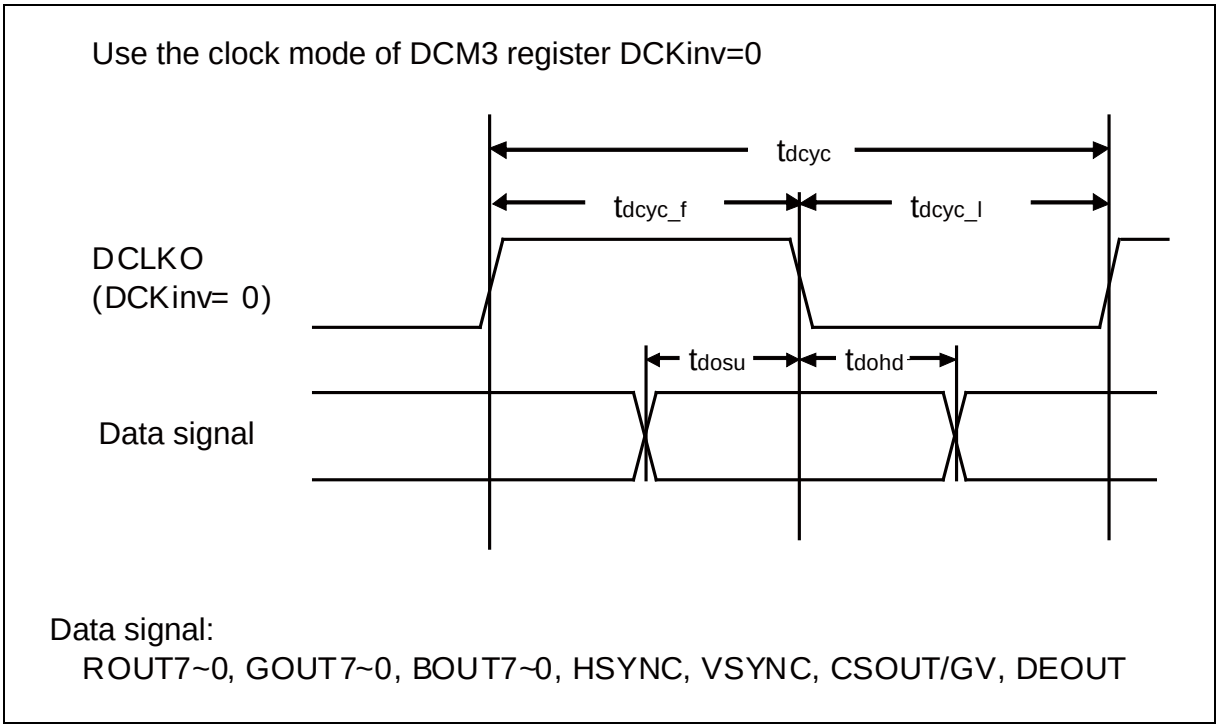
• Internal Shift Clock Mode



DCLKI Input Standard Mode (DCM3.DCKinv=0)

Figure 8 shows the setup/hold definition when the external display device (TFT) receives the signal at the falling edge of DCLKO.

Figure 8. DCLKI Input Standard Mode Setup/Hold Definition



DCLKI Input Reverse Edge Mode (DCM3.DCKinv=1)

Figure 9 shows the setup/hold definition when the external display device (TFT) receives the signal at the rising edge of DCLKO.

Figure 9. DCLKI Input Reverse Edge Mode Setup/Hold Definition