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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	308K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f591bspmc-gsk5e1

2.5 Pin Assignment (BGA Product)

(TOP VIEW)

▲	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A
B	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	21	B
C	75	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	95	22	C
D	74	143	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	161	96	23	D
E	73	142	203	256													219	162	97	24	E
F	72	141	202	255													220	163	98	25	F
G	71	140	201	254			257	258	259	260	261	262	263	264			221	164	99	26	G
H	70	139	200	253			284	285	286	287	288	289	290	265			222	165	100	27	H
J	69	138	199	252			283	304	305	306	307	308	291	266			223	166	101	28	J
K	68	137	198	251			282	303	316	317	318	309	292	267			224	167	102	29	K
L	67	136	197	250			281	302	315	320	319	310	293	268			225	168	103	30	L
M	66	135	196	249			280	301	314	313	312	311	294	269			226	169	104	31	M
N	65	134	195	248			279	300	299	298	297	296	295	270			227	170	105	32	N
P	64	133	194	247			278	277	276	275	274	273	272	271			228	171	106	33	P
R	63	132	193	246													229	172	107	34	R
T	62	131	192	245													230	173	108	35	T
U	61	130	191	244	243	242	241	240	239	238	237	236	235	234	233	232	231	174	109	36	U
V	60	129	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	110	37	V
W	59	128	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	38	W
Y	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

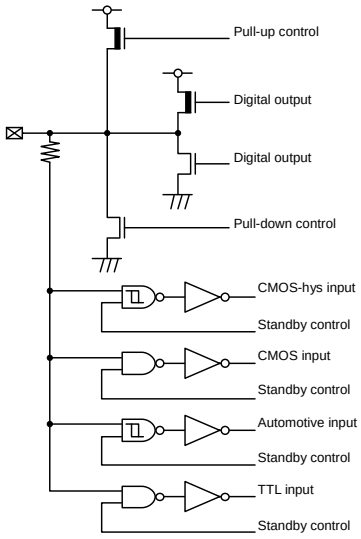
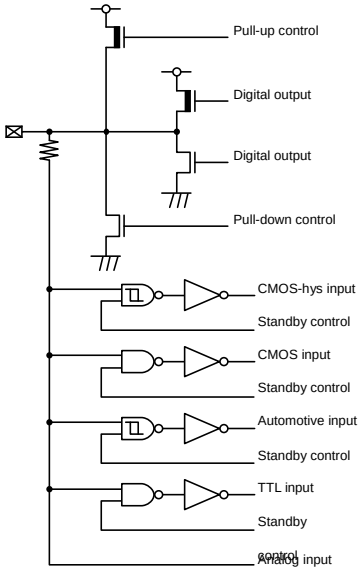
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
36	P125	–	A	General-purpose I/O port
	ICU0			Input capture ch.0 input pin
	SCK11			Multi-function serial ch.11 clock I/O pin
	OCU3			Output compare ch.3 output pin
	PPG10_2			PPG ch.10 output pin (2)
	TIN10			Reload timer ch.10 event input pin
37	P123	–	A	General-purpose I/O port
	SIN11			Multi-function serial ch.11 serial data input pin
	OCU1			Output compare ch.1 output pin
	PPG8_2			PPG ch.8 output pin (2)
	TIN8			Reload timer ch.8 event input pin
38	VSS	–	–	GND pin
39	VSS	–	–	GND pin
40	MD3	–	F3	Mode pin 3
41	DEBUGIF	–	G	DEBUG I/F pin
42	TX1	–	C	CAN transmission data1 output pin
	FRCK5			Free-run timer 5 clock input pin
	P110			General-purpose I/O port
	PPG1_2			PPG ch.1 output pin (2)
	TOT8_1			Reload timer ch.8 output pin (1)
43	P091	–	C	General-purpose I/O port
	ICU2_1			Input capture ch.2 input pin (1)
	INT12			INT12 External interrupt input pin
	SIN2			LIN-UART ch.2 serial data input pin
	PPG6_1			PPG ch.6 output pin (1)
	TOT2_1			Reload timer ch.2 output pin (1)
	SGA0			Sound generator ch.0 SGA output pin
44	VSS	–	–	GND pin
45	X0	–	L	Main clock oscillation input pin
46	X1	–	L	Main clock oscillation output pin
47	VSS	–	–	GND pin
48	A23	–	O	External bus · Address bit23 output pin
	P055			General-purpose I/O port (3V pin)
	SPI_SCK			SPI clock output pin
49	A22	–	O	External bus · Address bit22 output pin
	P054			General-purpose I/O port (3V pin)
	SPI_DI			SPI data input pin
50	C_2	–	–	Built-in regulator capacitor connected pin 2

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
51	A17	–	O	External bus · Address bit17 output pin
	P047			General-purpose I/O port (3V pin)
	QSPI_CLK			HS_SPI SCLK Output pin
52	A15	–	O	External bus · Address bit15 output pin
	P045			General-purpose I/O port (3V pin)
	QSPI_CS2			HS_SPI SSEL2 Output pin
53	A12	–	O	External bus · Address bit12 output pin
	P042			General-purpose I/O port (3V pin)
53	QSPI_SIO3	–	O	HS_SPI SDATA3 I/O pin
54	A09	–	O	External bus · Address bit9 output pin
	P037			General-purpose I/O port (3V pin)
	QSPI_SIO0			HS_SPI SDATA0 I/O pin
55	A05	–	O	External bus · Address bit5 output pin
	P033			General-purpose I/O port (3V pin)
56	A02	–	O	External bus · Address bit2 output pin
	P030			General-purpose I/O port (3V pin)
57	VSS	–	–	GND pin
58	VSS	–	–	GND pin
59	VSS	–	–	GND pin
60	P025	–	O	General-purpose I/O port (3V pin)
61	CS1X	–	O	External bus · Chip select 1 output pin
	P022			General-purpose I/O port (3V pin)
62	D15	–	O	External bus · Data bit15 I/O pin
	P017			General-purpose I/O port (3V pin)
63	GOUT1	–	O	Display digital G1 output pin
	D12			External bus · Data bit12 I/O pin
	P014			General-purpose I/O port (3V pin)
64	D8	–	O	External bus · Data bit8 I/O pin
	P010			General-purpose I/O port (3V pin)
65	D7	–	O	External bus · Data bit7 I/O pin
	P007			General-purpose I/O port (3V pin)
	PPG7			PPG ch.7 output pin
	TOT3_2			Reload timer ch.3 output pin (2)
66	D4	–	O	External bus · Data bit4 I/O pin
	P004			General-purpose I/O port (3V pin)
	SOT3_1			LIN-UART ch.3 serial data output pin (1)
	PPG4			PPG ch.4 output pin
	TOT0_2			Reload timer ch.0 output pin (2)
67	D1	–	O	External bus · Data bit1 I/O pin
	P001			General-purpose I/O port (3V pin)
	SOT2_1			LIN-UART ch.2 serial data output pin (1)
	PPG1			PPG ch.1 output pin
	TIN1_2			Reload timer ch.1 event input pin (2)
68	DCKOUT	–	O	Display reference clock output pin (for Internal sync)
	PG4			General-purpose I/O port (3V pin)
69	VSS	–	–	GND pin
70	C_3	–	–	Built-in regulator capacitor connected pin 3
71	BOUT4	–	O	Display digital B4 output pin
	PF4			General-purpose I/O port (3V pin)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
251	VSS	–	–	GND pin
252	VCC3	–	–	+3.3V power supply pin
253	VCC3	–	–	+3.3V power supply pin
254	VSS	–	–	GND pin
255	VCC3	–	–	+3.3V power supply pin
256	VCC3	–	–	+3.3V power supply pin
257	GND	–	–	GND pin
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
320	GND	–	–	GND pin

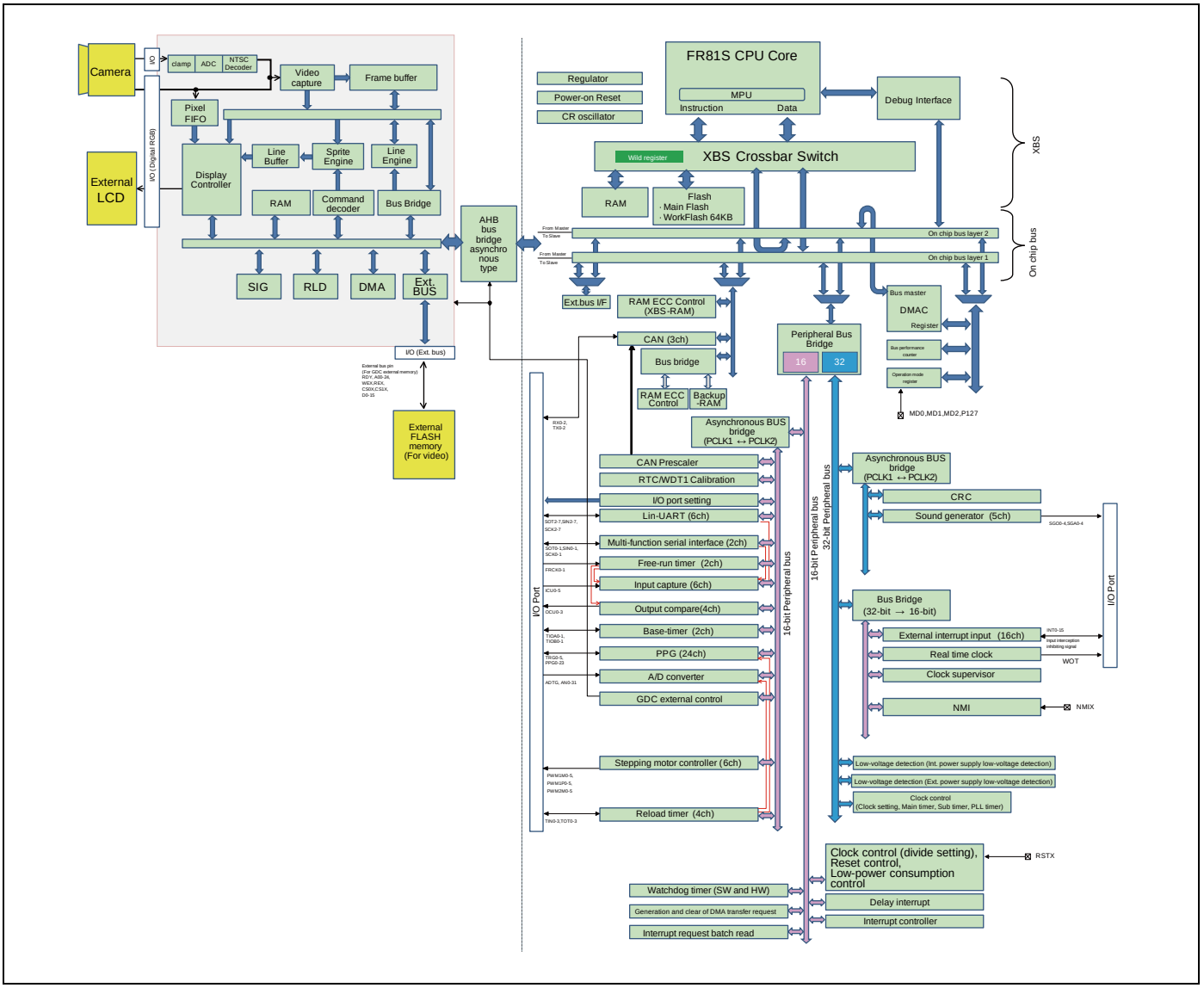
[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

4. I/O Circuit Type

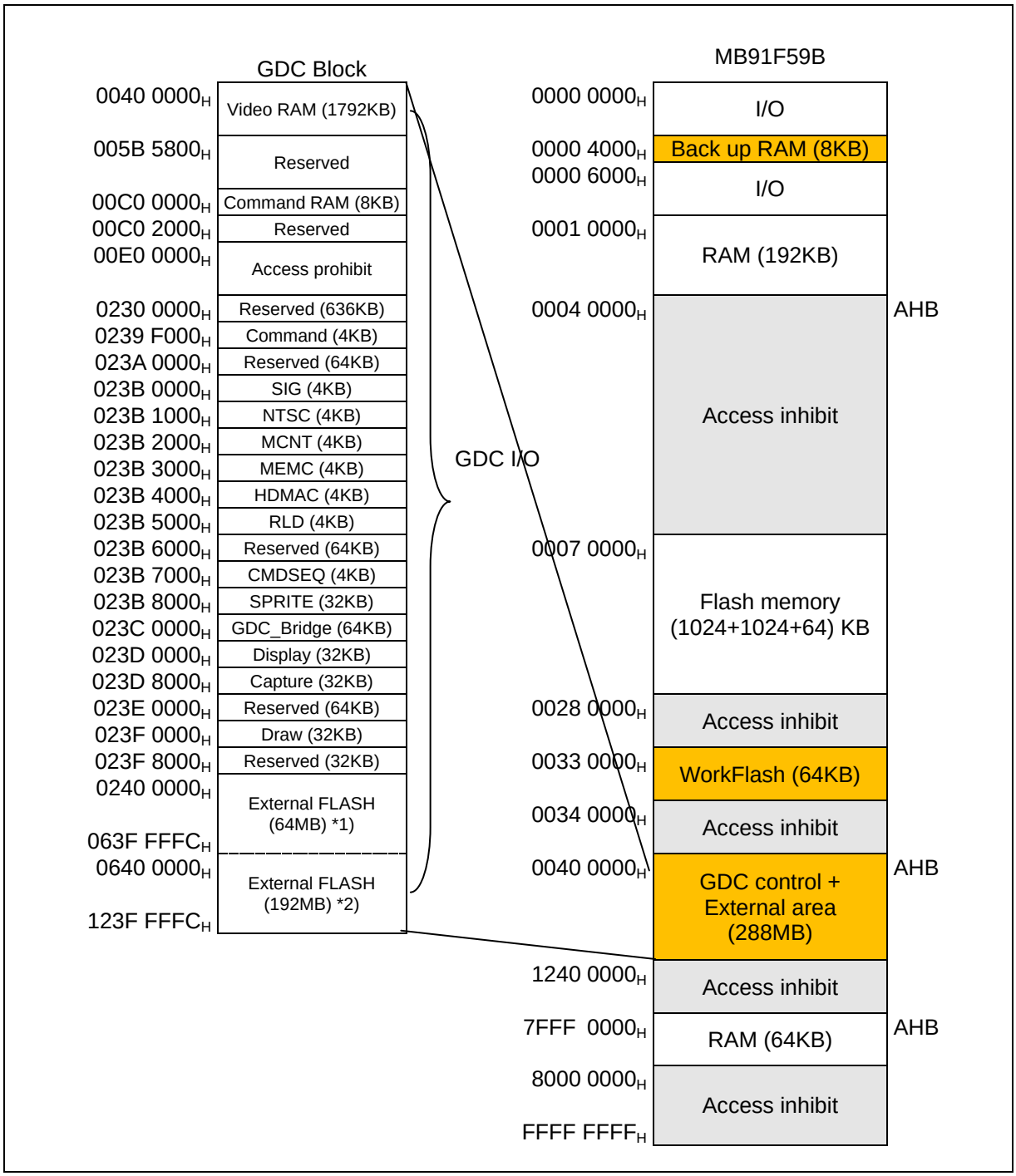
Type	Circuit	Remarks
A		• General-purpose I/O port • Output 1mA,2mA • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input
C		• Analog I/O, General-purpose I/O port • Output 1mA,2mA • Pull-up resistor control 50kΩ • Pull-down resistor control 50kΩ • CMOS input • Schmitt input • TTL input • Automotive input

7. Block Diagram

■MB91F591/592/594/596/597/599



■GDC memory map



Note: The GDC area is executed mapping with the little endian.

*1) Parallel interface supports 64MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192MB of memory space from 0640_0000H to 123F_FFFFH.
(HS-SPI totally supports 256MB of memory space from 0240_0000H to 123F_FFFFH for External FLASH)

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358_H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0004F0$_H$	SCR9 [R/W] B,H,W 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R/W] B,H,W 0-000011	ESCR9 [R/W] B,H,W -0000000	Multi-function serial 9 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
0004F4$_H$	RDR9/(TDR9)[R/W] B,H,W *1 -------0 00000000		BGR9 [R/W] H,W 00000000 00000000		
0004F8$_H$	—	—	—	—	
0004FC$_H$	FCR19 [R/W] B,H,W ---00100	FCR09 [R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
000500$_H$ to 00050C$_H$	—	—	—	—	Reserved
000510$_H$	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514$_H$	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518$_H$	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset [S]
00051C$_H$	—	—	—	—	Reserved [S]
000520$_H$	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524$_H$	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528$_H$	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		Clock control 2
00052C$_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530$_H$	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534$_H$	—	—	—	—	
000538$_H$	—	—	—	—	
00053C$_H$	—	—	—	—	
000540$_H$ to 00054C$_H$	—	—	—	—	Reserved
000550$_H$	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554$_H$	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558$_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002000_H	CTRLR0 [R/W] B,H,W -------- 000-0001		STATR0[R/W] B,H,W -------- 00000000		CAN0 (64msg)
002004_H	ERRCNT0 [R] B,H,W 00000000 00000000		BTR0[R/W] B,H,W -0100011 00000001		
002008_H	INTR0 [R] B,H,W 00000000 00000000		TESTR0[R/W] B,H,W -------- X00000--		
$00200C_H$	BRPER0 [R/W] B,H,W -------- ----0000		—		
002010_H	IF1CREQ0 [R/W] B,H,W 0------- 00000001		IF1CMSK0 [R/W] B,H,W -------- 00000000		
002014_H	IF1MSK20 [R/W] B,H,W 11-11111 11111111		IF1MSK10 [R/W] B,H,W 11111111 11111111		
002018_H	IF1ARB20 [R/W] B,H,W 00000000 00000000		IF1ARB10 [R/W] B,H,W 00000000 00000000		
$00201C_H$	IF1MCTR0 [R/W] B,H,W 00000000 0---0000		—		
002020_H	IF1DTA10 [R/W] B,H,W 00000000 00000000		IF1DTA20[R/W] B,H,W 00000000 00000000		
002024_H	IF1DTB10 [R/W] B,H,W 00000000 00000000		IF1DTB20 [R/W] B,H,W 00000000 00000000		
002028_H, $00202C_H$	Reserved				
002030_H, 002034_H	Reserved (IF1 data mirror)				
002038_H, $00203C_H$	Reserved				
002040_H	IF2CREQ0 [R/W] B,H,W 0------- 00000001		IF2CMSK0 [R/W] B,H,W -------- 00000000		
002044_H	IF2MSK20 [R/W] B,H,W 11-11111 11111111		IF2MSK10 [R/W] B,H,W 11111111 11111111		
002048_H	IF2ARB20 [R/W] B,H,W 00000000 00000000		IF2ARB10 [R/W] B,H,W 00000000 00000000		
$00204C_H$	IF2MCTR0 [R/W] B,H,W 00000000 0---0000		—		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002258H, 00225CH	Reserved				CAN2 (32msg)
002260H, 002264H	Reserved (IF2 data mirror)				
002268H to 00227CH	Reserved				
002280H	TREQR22[R] B,H,W 00000000 00000000		TREQR12[R] B,H,W 00000000 00000000		
002284H	—		—		
002288H	—		—		
00228CH	—		—		
002290 H	NEWDT22[R] B,H,W 00000000 00000000		NEWDT12[R] B,H,W 00000000 00000000		
002294H	—		—		
002298H	—		—		
00229CH	—		—		
0022A0H	INTPND22[R] B,H,W 00000000 00000000		INTPND12[R] B,H,W 00000000 00000000		
0022A4H	—		—		
0022A8H	—		—		
0022ACH	—		—		
0022B0H	MSGVAL22[R] B,H,W 00000000 00000000		MSGVAL12[R] B,H,W 00000000 00000000		
0022B4H	—		—		
0022B8H	—		—		
0022BCH	—		—		
0022C0H to 0022FCH	—	—	—	—	Reserved
002300H	DFCTLR[R/W]B,H,W -0------ --------		—	DFSTR [R/W] B,H,W -----001	WorkFlash
002304H	—	—	—	—	
002308H	FLIFCTLR [R/W] B,H,W ---0--00	—	FLIFFER1 [R/W] B,H,W --------	FLIFFER2 [R/W] B,H,W --------	
00230CH to 0023FCH	—	—	—	—	Reserved
002400H	SEEARX[R] B,H,W 00000000 00000000		DEEARX[R] B,H,W 00000000 00000000		XBS RAM ECC control register
002404H	EECSRX [R/W] B,H,W ----0000	—	EFEARX[R/W] B,H,W 00000000 00000000		
002408H	—	EFECRX[R/W] B,H,W -------0 00000000 00000000			
00240CH to 0024FCH	—	—	—	—	Reserved

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
High current output drive capacity Phase-to-phase deviation1	ΔV_{OH3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	DVcc=4.5V I_{OH}=-30.0mA Maximum deviation of V_{OH3}	–	–	90	mV	*2
High current output drive capacity Phase-to-phase deviation2	ΔV_{OL3}	PWM1Pn, PWM1Mn, PWM2Pn, PWM2Mn, n=0 to 5	DVcc=4.5V I_{OL}=30.0mA Maximum deviation of V_{OL3}	–	–	90	mV	*2

*1: The power supply current value when the external clock is supplied from the X1 pin. Note that the power supply current value when using the external clock is different from that using the oscillator.

*2: If PWM1P0/PWM1M0/PWM2P0/PWM2M0 of ch.0 is turned on simultaneously, the maximum deviation of V_{OH3} / V_{OL3} for each pin is defined. Same for other channels.

*3: This product contains both program Flash and WorkFlash. This parameter is defined when only one of them is in the write/erase state.

*4: MB91F591/2/4/6/7/9

*5: MB91F59A/B

11.4 AC Characteristics

11.4.1 Main Clock Timing

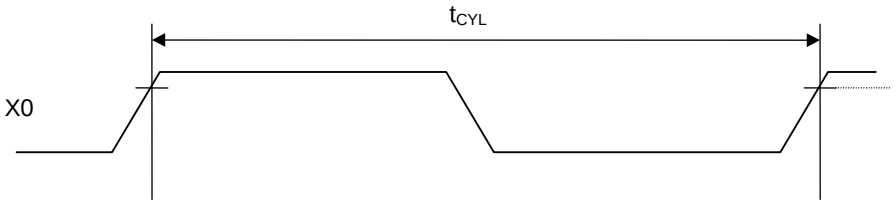
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	–	–	4	–	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		–	250	–	ns	
Internal operating clock frequency*1, *2	F_{CP}	–	–	2	–	128	MHz	CPU clock
	F_{CPP}	–	–	2	–	40	MHz	Peripheral bus clock
Internal operating clock cycle time*1, *2	t_{CP}	–	–	7.8125	–	500	ns	CPU clock
	t_{CPP}	–	–	25	–	500	ns	Peripheral bus clock
CAN PLL jitter (when lock)	t_{PJ}	–	–	-10	–	+10	ns	
Built-in CR oscillation frequency	F_{CCR}	–	–	50	100	200	kHz	

*1: The maximum frequency of CPU clock is described in the table of Product Type.

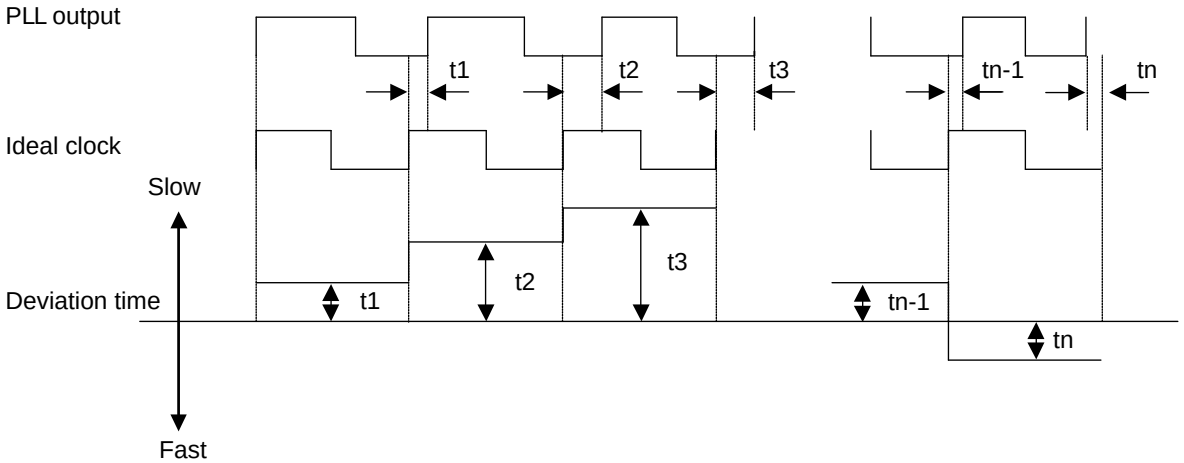
*2: The maximum / minimum value is defined when using the main clock and PLL clock.

• X0,X1 Clock Timing



• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.

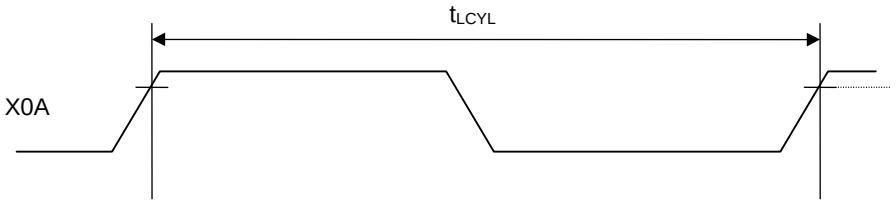


11.4.1.1 Sub clock timing (products without s-suffix)

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	–	–	30.52	–	µs	

• X0A,X1A Clock Timing



■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=0, SCR: SPI=1

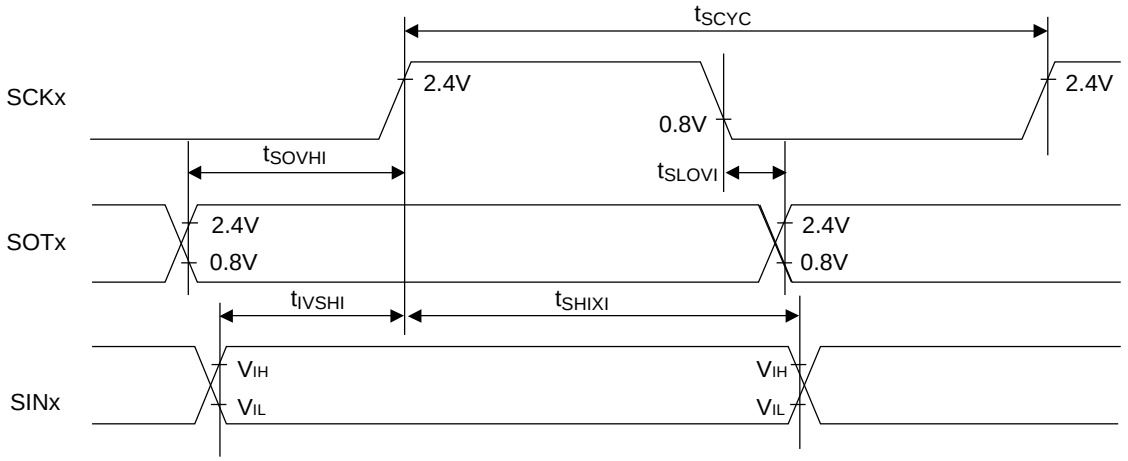
(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK ↑ → SOT delay time	t_{SHOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCKx, SINx		34	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns
SOT → SCK ↓ delay time	t_{SOVLI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H" pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↑ → SOT delay time	t_{SHOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCKx, SINx		10	–	ns
SCK ↓ → Valid SIN hold time	t_{SLIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

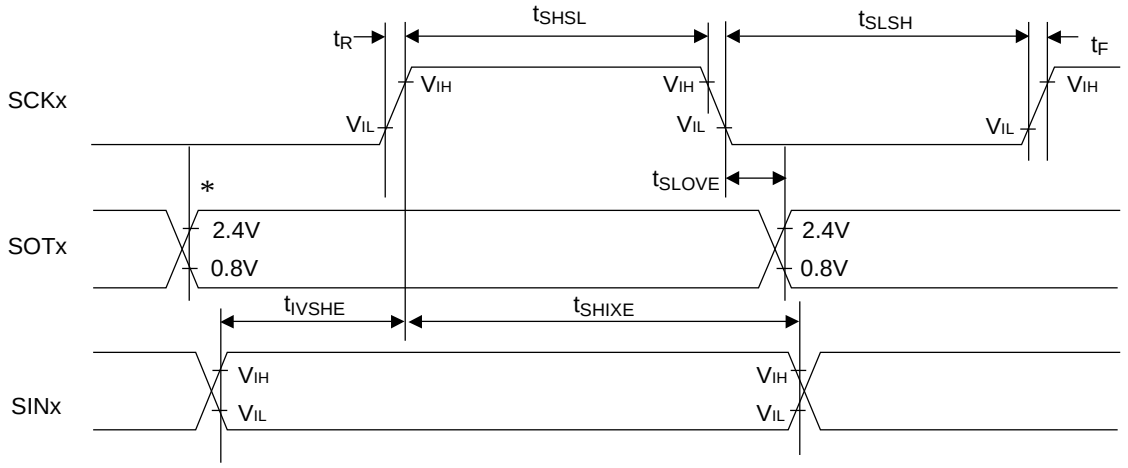
Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

• **Internal Shift Clock Mode**

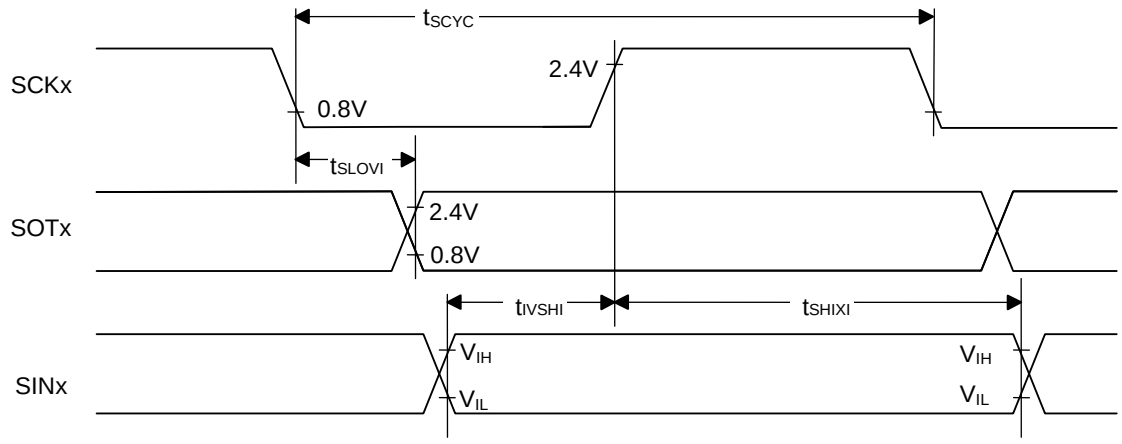


• **External Shift Clock Mode**

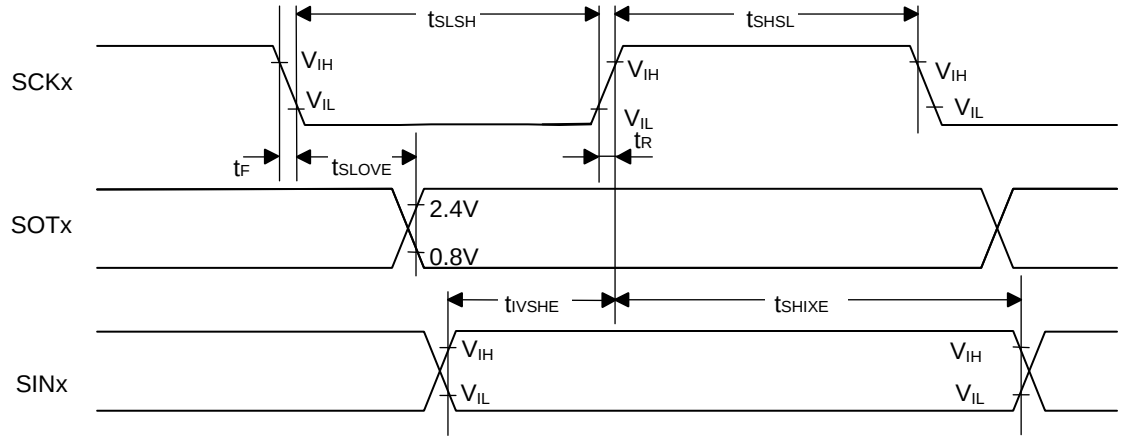


***: Changes when Writing to TDR Register**

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



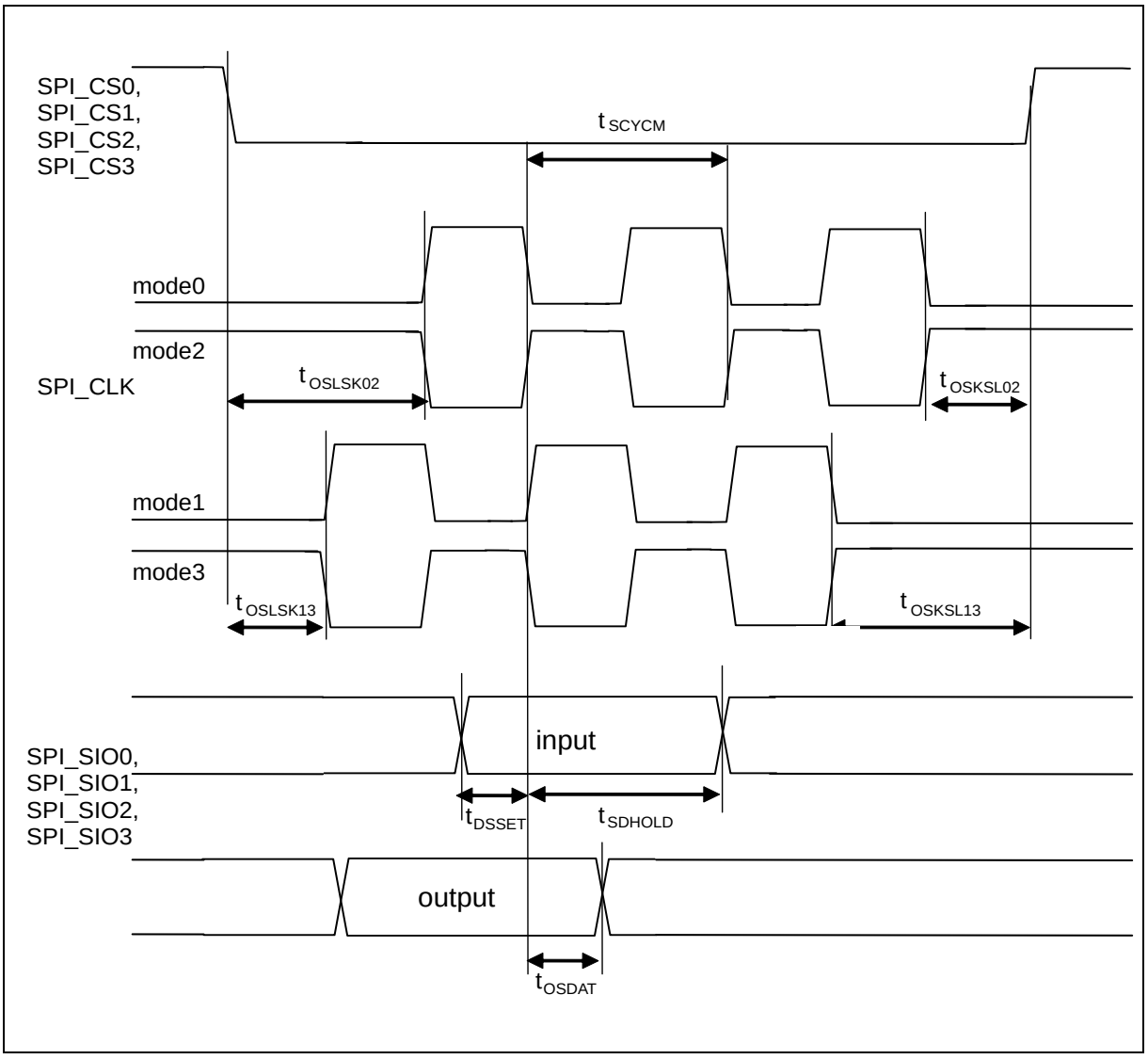
■Bit setting: ESCR: SCES=1, ECCR: SCDE=0

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

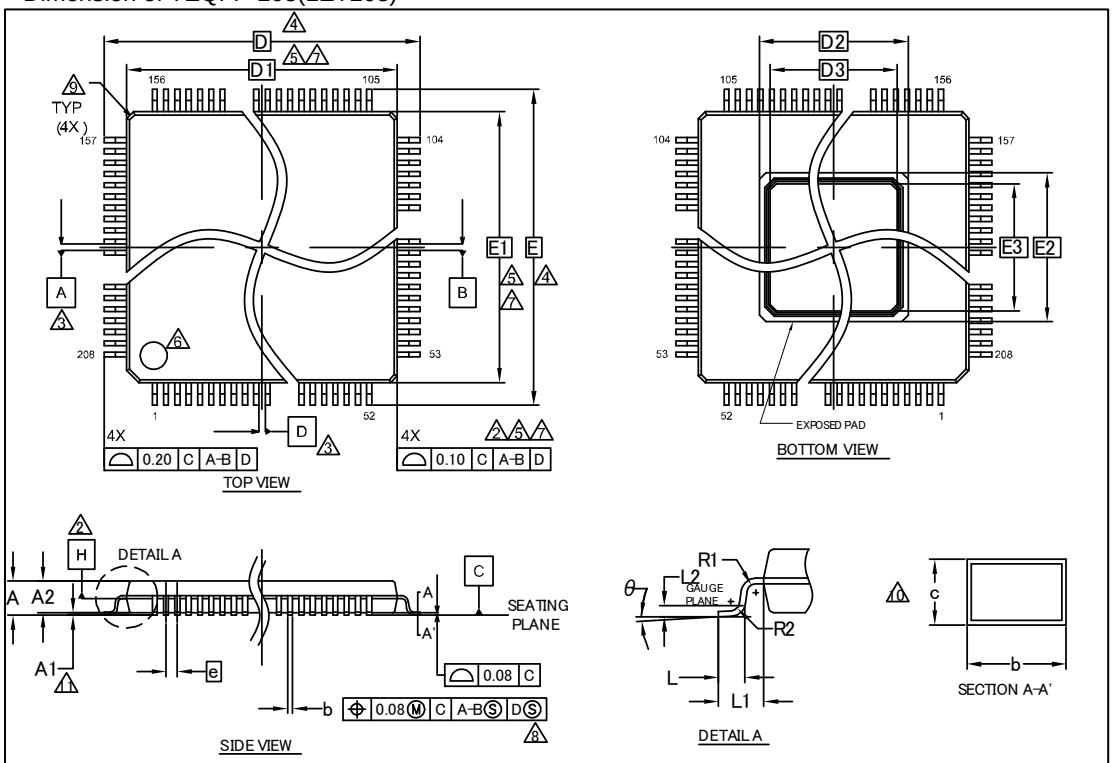
Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1 • TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80pF+1 • TTL
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		30	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.


SPI_CS0,
SPI_CS1,
SPI_CS2,
SPI_CS3
tSCYCM
mode0
mode2
SPI_CLK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
SPI_SIO0,
SPI_SIO1,
SPI_SIO2,
SPI_SIO3
input
tDSSET
tSDHOLD
output
tOSDAT

■Dimension of TEQFP-208(LET208)



SYMBOL	DIMENSION		
	MIN.	NOM.	MAX.
A	——	——	1.70
A1	0.05	——	0.15
A2	1.35	1.40	1.45
D	30.00 BSC		
D1	28.00 BSC		
D2	9.90 REF		
D3	8.71 REF		
E	30.00 BSC		
E1	28.00 BSC		
E2	9.90 REF		
E3	8.71 REF		
R1	0.08	——	——
R2	0.08	——	0.20
θ	0°	4°	8°
c	0.12	——	0.20
b	0.17	0.22	0.27
L	0.45	0.60	0.75
L1	1.00 REF		
L2	0.25		
e	0.50 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. EXACT SHAPE AND SIZE OF THIS FEATURE IS OPTIONAL.
10. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
11. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-13651 *A

PACKAGE OUTLINE, 208 LEAD TEQFP
28.0X28.0X1.7 MM LET208 REV*A