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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	848K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f592bhpmc-gsk5e1

Item \ Product		MB91F599B/BS*	MB91F599BH/BHS*
CPU core		FR81S	
Technology		90nm	
Package		HQFP208	
Sub clock		Yes (Non-S series) No (S series)	
Maximum CPU operating frequency		128MHz	
Maximum GDC operating frequency		81MHz	
Built-in CR oscillator		100kHz	
System clock		On chip PLL	
Flash	Main	1088KB	
	Work	64KB	
RAM	Main	64KB	
	Backup	8KB	
VRAM		800KB	
Watchdog timer		1ch Hardware 1ch Software	
Clock supervisor		Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes	
Low-voltage detection reset (Internal low-voltage detection)		Yes	
NMI function		Yes	
DMA Controller		16ch	
CAN		1ch (64msg) 2ch (32msg)	
LIN-UART		6ch	
Multi-function Serial Interface		2ch	
A/D Converter (8bit/10bit)		1unit/32ch	
Reload timer(16bit)		4ch	
Base timer(16bit)		2ch	
Free-run timer(32bit)		2ch	
Input capture(32bit)		6ch	
Output compare(32bit)		4ch	
PPG timer(16bit)		24ch	
Sound generator		5ch	
Real-time clock		Yes	
External interrupt		16ch	
CR/SUB compensation function		Yes	
CRC generation		Yes	
Stepping motor control		6ch	
Stop mode (including power shut-off)		Supported	
Power supply voltage		MICOM:4.5V to 5.5V GDC:3.0V to 3.6V	
Operating temperature		-40°C to +105°C	
Allowable power [mW]		2500	
Others		Flash product	
On chip debugger		Yes	

*: Under consideration. For detailed information about mount conditions, contact your sales representative.

*1:Under consideration.

*2: Start address of Work Flash memory is different between MB91F591/2/4/6/7/9 and MB91F59A/B.

*3: I^2C is supported with ch.0 and ch.1 only.

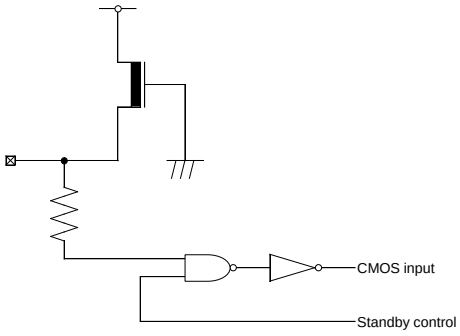
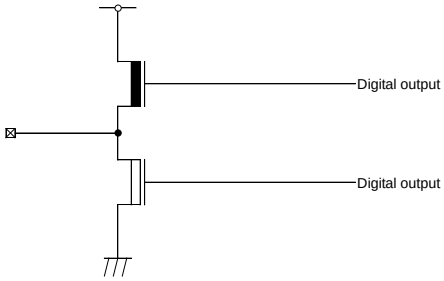
Main difference of functionality between MB91F594 and MB91F59B

Part	Item	MB91F594	MB91F59B
MCU part	FLASH (main)	1088KB	2112KB
	RAM (Main)	64KB	192KB
	RAM (Sub on AHB)	-	64KB
	Multi-function Serial Interface	2ch	6ch
	Free-run timer	2ch	8ch
	Input Capture	6ch	12ch
	Reload timer	4ch	8ch
	Up/down counter	-	3ch
	Package	LQFP208	BGA320/TEQPF-208*
	JTAG Boundary Scan Test	-	Yes (Only support BGA package products)
GDC part	VRAM	800KB	1792KB
	High Speed SPI	-	Yes

*: Under consideration.

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
166	P120	–	C	General-purpose I/O port
	FRCK1	–		Free-run timer 1 clock input pin
	SIN5	–		LIN-UART ch.5 serial data input pin
	INT6	–		INT6 External interrupt input pin
	TOT1	–		Reload timer ch.1 output pin
	PPG5_2	–		PPG ch.5 output pin (2)
167	P121	–	C	General-purpose I/O port
	FRCK0	–		Free-run timer 0 clock input pin
	SOT5	–		LIN-UART ch.5 serial data output pin
	INT7	–		INT7 External interrupt input pin
	TOT2	–		Reload timer ch.2 output pin
	PPG6_2	–		PPG ch.6 output pin (2)
168	P122	–	C	General-purpose I/O port
	OCU0	–		Output compare ch.0 output pin
	SCK5	–		LIN-UART ch.5 clock I/O pin
	TOT3	–		Reload timer ch.3 output pin
	PPG7_2	–		PPG ch.7 output pin (2)
108	P123	–	A	General-purpose I/O port
	OCU1	–		Output compare ch.1 output pin
	PPG8_2	–		PPG ch.8 output pin (2)
	TIN8	–		Reload timer ch.8 event input pin(MB91F59A/B only)
	SIN11	–		Multi-function serial ch.11 serial data input pin(MB91F59A/B only)
109	P124	–	A	General-purpose I/O port
	OCU2	–		Output compare ch.2 output pin
	ICU5_2	–		Input capture ch.5 input pin (2)
	PPG9_2	–		PPG ch.9 output pin (2)
	TIN9	–		Reload timer ch.9 event input pin(MB91F59A/B only)
	SOT11	–		Multi-function serial ch.11 serial data output pin(MB91F59A/B only)
110	P125	–	A	General-purpose I/O port
	OCU3	–		Output compare ch.3 output pin
	ICU0	–		Input capture ch.0 input pin
	PPG10_2	–		PPG ch.10 output pin (2)
	TIN10	–		Reload timer ch.10 event input pin(MB91F59A/B only)
	SCK11	–		Multi-function serial ch.11 clock I/O pin(MB91F59A/B only)
90	P126	–	A	General-purpose I/O port
	TRG0	–		PPG trigger 0 input pin (ch.0 to ch.3)
	SIN0	–		Multi-function serial ch.0 serial data input pin
	INT1	–		INT1 External interrupt input pin
91	P127	–	K	General-purpose I/O port
	SOT0	–		Multi-function serial ch.0 serial data output pin / I^2C ch.0 serial data I/O pin
92	P130	–	K	General-purpose I/O port
	SCK0	–		Multi-function serial ch.0 clock I/O pin / I^2C ch.0 clock I/O pin
	INT0	–		INT0 External interrupt input pin
	ICU1	–		Input capture ch.1 input pin
	TIOA0	–		Base timer TIOA0 output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
105	AN7	–	C	ADC Analog 7 input pin
	P107			General-purpose I/O port
	ICU11_1			Input capture ch.11 input pin (1)
	PPG5_1			PPG ch.5 output pin (1)
	TOT7_1			Reload timer ch.7 output pin (1)
	SGO4_1			Sound generator ch.4 SGO output pin
106	AN4	–	C	ADC Analog 4 input pin
106	P104	–	C	General-purpose I/O port
	ICU8_1			Input capture ch.8 input pin (1)
	SOT5_1			LIN-UART ch.5 serial data output pin (1)
	PPG2_1			PPG ch.2 output pin (1)
	TOT0_1			Reload timer ch.0 output pin (1)
107	AN2	–	C	ADC Analog 2 input pin
	P102			General-purpose I/O port
	ICU6_1			Input capture ch.6 input pin (1)
	SCK4_1			LIN-UART ch.4 clock I/O pin (1)
	PPG10			PPG ch.10 output pin
	TIN2_1			Reload timer ch.2 event input pin (1)
108	AVCC5	–	–	A/D convertor analog power supply pin
109	P124	–	A	General-purpose I/O port
	ICU5_2			Input capture ch.5 input pin (2)
	SOT11			Multi-function serial ch.11 serial data output pin
	OCU2			Output compare ch.2 output pin
	PPG9_2			PPG ch.9 output pin (2)
	TIN9			Reload timer ch.9 event input pin
110	RX0	–	A	CAN reception data0 input pin
	P096			General-purpose I/O port
	INT9			INT9 External interrupt input pin
111	VSS	–	–	GND pin
112	RX1	–	C	CAN reception data 1 input pin
	FRCK6			Free-run timer 6 clock input pin
	P111			General-purpose I/O port
	INT10			INT10 External interrupt input pin
	PPG2_2			PPG ch.2 output pin (2)
	TOT9_1			Reload timer ch.9 output pin (1)
113	P093	–	C	General-purpose I/O port
	ICU3_1			Input capture ch.3 input pin (1)
	INT14			INT14 External interrupt input pin
	SOT2			LIN-UART ch.2 serial data output pin
	PPG8_1			PPG ch.8 output pin (1)
	TIN8_1			Reload timer ch.8 event input pin (1)
	SGA1			Sound generator ch.1 SGA output pin
114	NMIX	N	F1	Non-masking interrupt input pin
115	TIOA1	–	A	Base timer TIOA1 I/O pin
	P131			General-purpose I/O port
	ICU2			Input capture ch.2 input pin
	INT4			INT4 External interrupt input pin
	SIN1			Multi-function serial ch.1 serial data input pin
	TRG1			PPG trigger 1 input pin (ch.4 to ch.7)
	TOT7			Reload timer ch.7 output pin

Type	Circuit	Remarks
V		• TRST (JTAG) • CMOS input • Pull-up resistor control 50kΩ (1.2V Cont)
W		• TDO (JTAG) In case of Boundary Scan Test mode. • High Impedance state In other case of Boundary Scan Test Mode. • 5mA output

■Crystal oscillation circuit
An external noise to the X0 pin or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out the X0 pin and the X1 pin, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 pin and X1 pin by ground circuits.

■Mode pins (MD2, MD1, MD0)
Connect the MD2, MD1and MD0 mode pin to the VCC pin or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and the VCC pin or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■During power-on
To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

■Notes during PLL clock operation
When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

■Treatment of A/D converter power supply pins
Connect the pins to have AVCC5=AVRH5=VCC5 and AVSS5/AVRL5=VSS even if the A/D converter is not used.

Also, similarly connect the pins of NTSC A/D converter power supply to have AVCC3=VCC3 and AVSS3=VSS. At this time, open VIN/REFOUT.

■Notes on using external clock
An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

■Power-on sequence of A/D converter analog inputs
Be sure to turn on the digital power supply (Vcc5) first, and then turn on the A/D converter power supplies (AVcc5, AVRH5, AVRL5) and analog inputs (AN0 to AN31). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc5). When the AVRH5 pin voltage is turned on or off, it must not exceed AVCC5. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc5. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

Be sure to similarly turn on the digital power supply (VCC3) first, and then turn on the A/D converter power supply (AVCC3) for NTSC and NTSC inputs (VIN, AVR). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (VCC3).

■Treatment of power supplies for high current output buffer pins (DVcc, DVss)
Be sure to turn on the digital power supply (Vcc) first, and then turn on the power supplies for high current output buffer pins (DVcc, DVss). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply (Vcc).

Even if the high current output buffer pins are used as general-purpose ports, the power supplies of high current output buffer pins (DVcc, DVss) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

■Treatment of C pin
This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

■Function switching of a multiplexed port
To switch between the port function and the multiplexed pin function, use the PFR (port function register).

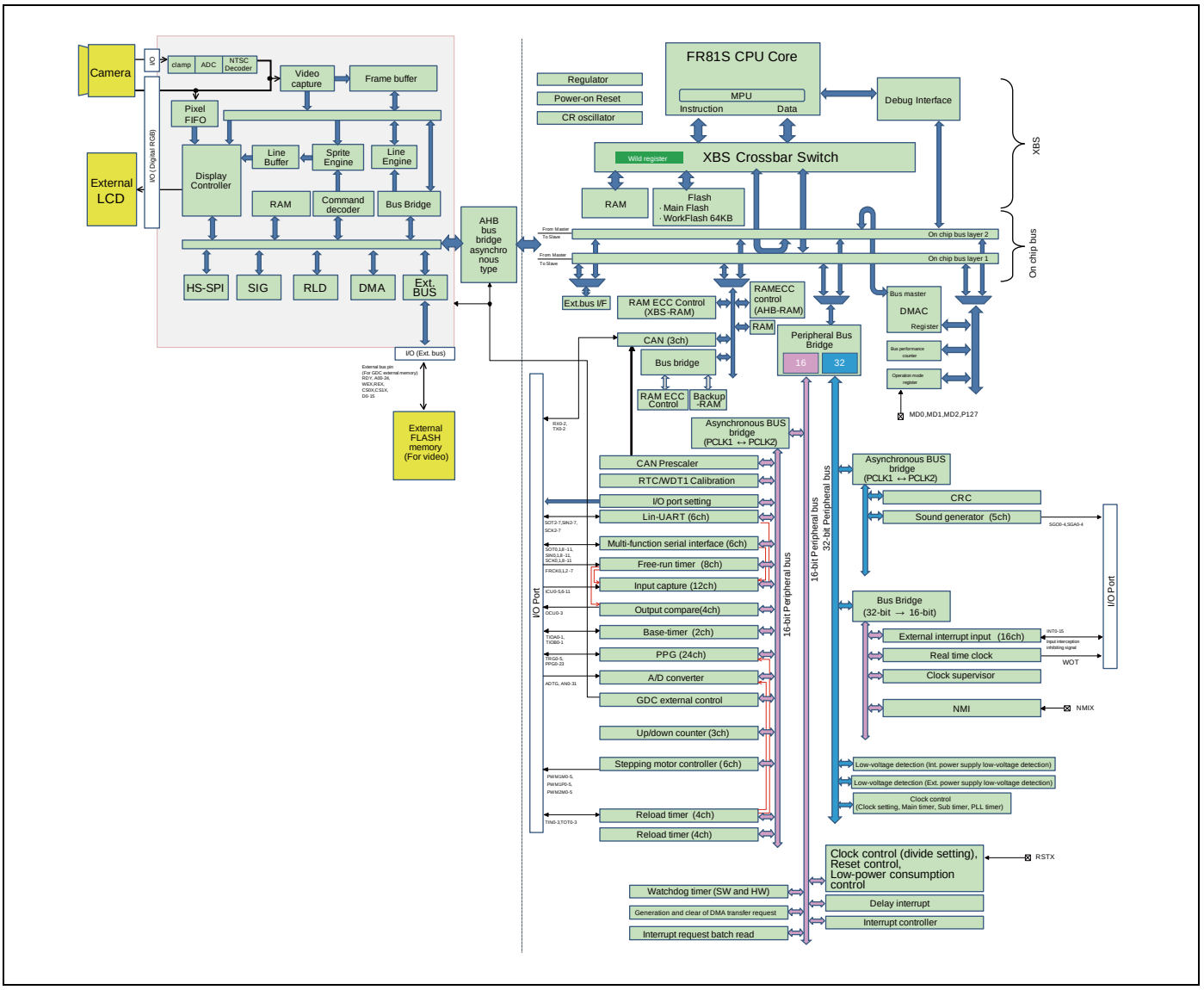
■Low-power consumption mode
To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL".

Power supply for GDC can be turned off separately from the microcontroller.

Take the following notes when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

■MB91F59A/59B



Note: I/O of peripheral functions can be confirmed at "PIN ASSIGNMENT" and "PIN DESCRIPTION".

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -0000000 00000000		Base timer 1
000094_H	—	BT1STC [R/W] B 0000-000	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base timer 0,1
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	
$0000AC_H$	—	—	—	—	Reserved
$0000B0_H$	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-function serial 0 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000B4_H$	RDR0/(TDR0)[R/W] B,H,W *1 -------0 00000000		BGR0 [R/W] H,W 00000000 00000000		
$0000B8_H$	— / (ISMK0) [R/W] B,H,W -------- *2	— / (ISBA0) [R/W] B,H,W -------- *2	—	—	
$0000BC_H$	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	
$0000C0_H$	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-function serial 1 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000C4_H$	RDR1/(TDR1)[R/W] B,H,W *1 -------0 00000000		BGR1 [R/W] H,W 00000000 00000000		
$0000C8_H$	— / (ISMK1) [R/W] B,H,W -------- *2	— /(ISBA1) [R/W] B,H,W -------- *2	—	—	
$0000CC_H$	FCR11 [R/W] B, H, W ---00100	FCR01[R/W] B, H, W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
$0000D0_H$	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
$0000D4_H$	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
$0000D8_H$	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
$0000DC_H$	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000200_H	PWC20 [R/W] H,W ------XX XXXXXXXX		PWC10 [R/W] H,W ------XX XXXXXXXX		Stepping motor controller
000204_H	—	PWC0 [R/W] B -00000--	PWS20 [R/W] B,H,W -0000000	PWS10 [R/W] B,H,W --000000	
000208_H	PWC21 [R/W] H,W ------XX XXXXXXXX		PWC11 [R/W] H,W ------XX XXXXXXXX		
$00020C_H$	—	PWC1 [R/W] B -00000--	PWS21 [R/W] B,H,W -0000000	PWS11 [R/W] B,H,W --000000	
000210_H	PWC22 [R/W] H,W ------XX XXXXXXXX		PWC12 [R/W] H,W ------XX XXXXXXXX		
000214_H	—	PWC2 [R/W] B -00000--	PWS22 [R/W] B,H,W -0000000	PWS12 [R/W] B,H,W --000000	
000218_H	PWC23 [R/W] H,W ------XX XXXXXXXX		PWC13 [R/W] H,W ------XX XXXXXXXX		
$00021C_H$	—	PWC3 [R/W] B -00000--	PWS23 [R/W] B,H,W -0000000	PWS13 [R/W] B,H,W --000000	
000220_H	PWC24 [R/W] H,W ------XX XXXXXXXX		PWC14 [R/W] H,W ------XX XXXXXXXX		
000224_H	—	PWC4 [R/W] B -00000--	PWS24 [R/W] B,H,W -0000000	PWS14 [R/W] B,H,W --000000	
000228_H	PWC25 [R/W] H,W ------XX XXXXXXXX		PWC15 [R/W] H,W ------XX XXXXXXXX		
$00022C_H$	—	PWC5 [R/W] B -00000--	PWS25 [R/W] B,H,W -0000000	PWS15 [R/W] B,H,W --000000	
000230_H to $00023C_H$	—	—	—	—	Reserved
000240_H	CPCLR0 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 0
000244_H	TCDT0 [R/W] W 00000000 00000000 00000000 00000000				
000248_H	TCCSH0 [R/W]B, H, W 0-----00	TCCSL0 [R/W]B, H, W -1-00000	—		
$00024C_H$	CPCLR1 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 1
000250_H	TCDT1 [R/W] W 00000000 00000000 00000000 00000000				
000254_H	TCCSH1 [R/W]B, H, W 0-----00	TCCSL1 [R/W]B, H, W -1-00000	—		
000258_H	—	—	—	—	Reserved
$00025C_H$	GCN10 [R/W] H 00110010 00010000		—	GCN20 [R/W] B ----0000	PPG0,1,2,3 control
000260_H	GCN11 [R/W] H 00110010 00010000		—	GCN21 [R/W] B ----0000	PPG4,5,6,7 control
000264_H	GCN12 [R/W] H 00110010 00010000		—	GCN22 [R/W] B ----0000	PPG8,9,10,11 control

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000268_H	—	—	—	PPGDIV [R/W] B ------00	PPG0
$00026C_H$	PTMR0 [R] H,W 11111111 11111111		PCSR0 [W] H,W XXXXXXXX XXXXXXXX		
000270_H	PDUT0 [W] H,W XXXXXXXX XXXXXXXX		PCN0 [R/W] B, H,W 0000000- 000000-0		
000274_H	PTMR1 [R] H,W 11111111 11111111		PCSR1 [W] H, W XXXXXXXX XXXXXXXX		PPG1
000278_H	PDUT1 [W] H,W XXXXXXXX XXXXXXXX		PCN1 [R/W] B, H,W 0000000- 000000-0		
$00027C_H$	PTMR2 [R] H,W 11111111 11111111		PCSR2 [W] H,W XXXXXXXX XXXXXXXX		PPG2
000280_H	PDUT2 [W] H,W XXXXXXXX XXXXXXXX		PCN2 [R/W] B, H,W 0000000- 000000-0		
000284_H	PTMR3 [R] H,W 11111111 11111111		PCSR3 [W] H,W XXXXXXXX XXXXXXXX		PPG3
000288_H	PDUT3 [W] H,W XXXXXXXX XXXXXXXX		PCN3 [R/W] B, H,W 0000000- 000000-0		
$00028C_H$	PTMR4 [R] H,W 11111111 11111111		PCSR4 [W] H,W XXXXXXXX XXXXXXXX		PPG4
000290_H	PDUT4 [W] H,W XXXXXXXX XXXXXXXX		PCN4 [R/W] B, H,W 0000000- 000000-0		
000294_H	PTMR5 [R] H,W 11111111 11111111		PCSR5 [W] H,W XXXXXXXX XXXXXXXX		PPG5
000298_H	PDUT5 [W] H,W XXXXXXXX XXXXXXXX		PCN5 [R/W] B, H,W 0000000- 000000-0		
$00029C_H$	PTMR6 [R] H,W 11111111 11111111		PCSR6 [W] H,W XXXXXXXX XXXXXXXX		PPG6
$0002A0_H$	PDUT6 [W] H,W XXXXXXXX XXXXXXXX		PCN6 [R/W] B, H,W 0000000- 000000-0		
$0002A4_H$	PTMR7 [R] H,W 11111111 11111111		PCSR7 [W] H,W XXXXXXXX XXXXXXXX		PPG7
$0002A8_H$	PDUT7 [W] H,W XXXXXXXX XXXXXXXX		PCN7 [R/W] B, H,W 0000000- 000000-0		
$0002AC_H$	PTMR8 [R] H,W 11111111 11111111		PCSR8 [W] H,W XXXXXXXX XXXXXXXX		PPG8
$0002B0_H$	PDUT8 [W] H,W XXXXXXXX XXXXXXXX		PCN8 [R/W] B, H,W 0000000- 000000-0		
$0002B4_H$	PTMR9 [R] H,W 11111111 11111111		PCSR9 [W] H,W XXXXXXXX XXXXXXXX		PPG9
$0002B8_H$	PDUT9 [W] H,W XXXXXXXX XXXXXXXX		PCN9 [R/W] B, H,W 0000000- 000000-0		
$0002BC_H$	PTMR10 [R] H,W 11111111 11111111		PCSR10 [W] H,W XXXXXXXX XXXXXXXX		PPG10
$0002C0_H$	PDUT10 [W] H,W XXXXXXXX XXXXXXXX		PCN10 [R/W] B, H,W 0000000- 000000-0		
$0002C4_H$	IPCP0 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 0,1
$0002C8_H$	IPCP1 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$0002CC_H$	ICFS01 [R/W] B, H, W ------00	—	LSYNS0 [R/W] B, H, W --000000	ICS01 [R/W] B, H, W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
00055C$_H$	—	—	WTDR[R/W] H 00000000 00000000		Real-time clock
000560$_H$	—	WTCRH [R/W] B ------00	WTCRM [R/W] B,H 00000000	WTCRL [R/W] B,H ----00-0	
000564$_H$	—	WTBRH [R/W] B --XXXXXX	WTBRM [R/W] B XXXXXXXX	WTBRL [R/W] B XXXXXXXX	
000568$_H$	WTHR [R/W] B,H ---00000	WTMR [R/W] B,H --000000	WTSR [R/W] B --000000	—	
00056C$_H$	—	CSVCR [R/W] B -001110- -001010-*4	—	—	Clock supervisor *4: An initial value is different by part number. For details, see the CSVCR register in chapter "Clock Supervisor"
000570$_H$ to 00057C$_H$	—	—	—	—	Reserved
000580$_H$	REGSEL [R/W] B,H,W 0110011-	—	—	—	Regulator control
000584$_H$	LVD5R [R/W] B,H,W -------1	LVD5F [R/W] B,H,W 0-100--1	LVD [R/W] B,H,W 01000--0	—	Low-power detection
000588$_H$	GLVD5R[R/W] B,H,W 0-01-0-X	GLVD5F[R/W] B,H,W 0-0100-X	GLVD[R/W] B,H,W 010000-X	—	
00058C$_H$	—	—	—	—	Reserved
000590$_H$	PMUSTR [R/W] B,H,W 0-----1X	PMUCTLR [R/W] B,H,W 0-00----	PWRTMCTL [R/W] B,H,W -----011	—	PMU
000594$_H$	PMUINTF0 [R/W] B,H,W 00000000	PMUINTF1 [R/W] B,H,W 00000000	PMUINTF2 [R/W] B,H,W 0000----	—	
000598$_H$	GSTR[R] B,H,W 0-------	GCTLR[R/W] B,H,W 0000-111	—	—	
00059C$_H$	—	—	—	—	
0005A0$_H$ to 0005FC$_H$	—	—	—	—	Reserved
000600$_H$ to 00060C$_H$	—	—	—	—	Reserved[S]
000610$_H$ to 00063C$_H$	—	—	—	—	Reserved[S]
000640$_H$ to 00064C$_H$	—	—	—	—	Reserved[S]
000650$_H$ to 00067C$_H$	—	—	—	—	Reserved[S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000680_H to $00068C_H$	—	—	—	—	Reserved[S]
000690_H to $0006BC_H$	—	—	—	—	Reserved[S]
$0006C0_H$ to $0006CC_H$	—	—	—	—	Reserved[S]
$0006D0_H$ to $0006F0_H$	—	—	—	—	Reserved
$0006F4_H$	—	—	—	—	Reserved
$0006F8_H$ to $00070C_H$	—	—	—	—	Reserved
000710_H	BPCCRA[R/W] B 00000000	BPCCRB[R/W] B 00000000	BPCCRC[R/W] B 00000000	—	Bus performance counter
000714_H	BPCTRA[R/W] W 00000000 00000000 00000000 00000000				
000718_H	BPCTRB[R/W] W 00000000 00000000 00000000 00000000				
$00071C_H$	BPCTRC[R/W] W 00000000 00000000 00000000 00000000				
000720_H to $0007F8_H$	—	—	—	—	Reserved
$0007FC_H$	BMODR[R] B, H, W XXXXXXXX	—	—	—	Operation mode
000800_H to $00083C_H$	—	—	—	—	Reserved [S]
000840_H	FCTLR[R/W] H -0--1000 0--0----		—	FSTR[R/W] B -----001	Flash memory register [S]
000844_H to 000854_H	—	—	—	—	Reserved [S]
000858_H	—	—	WREN[R/W] H 00000000 00000000		Wild register [S]
$00085C_H$ to $00087C_H$	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
$000E10_H$	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
$000E14_H$	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
$000E18_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
$000E30_H$	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
$000E34_H$	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	
$000E38_H$ to $000E3C_H$	—	—	—	—	Reserved

11.3 DC Characteristics

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	CMOS input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH2}		CMOS hysteresis input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH3}		Automotive input level is selected	0.8× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH4}		TTL input level is selected	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH5}	RSTX, NMIX, MD2	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH7}	MD0,MD1	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH8}	DEBUGIF	–	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH10}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	CMOS hysteresis input level is selected	0.7× $V_{CC}3$	–	$V_{CC}3$+ 0.3	V	3.3V dedicated pin
	V_{IH11}		TTL input level is selected	2.0	–	$V_{CC}3$+ 0.3	V	
	V_{IH12}	MD3	-	0.8× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only
	V_{IH13}	TDI, TMS, TRST, TCK	-	0.7× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only

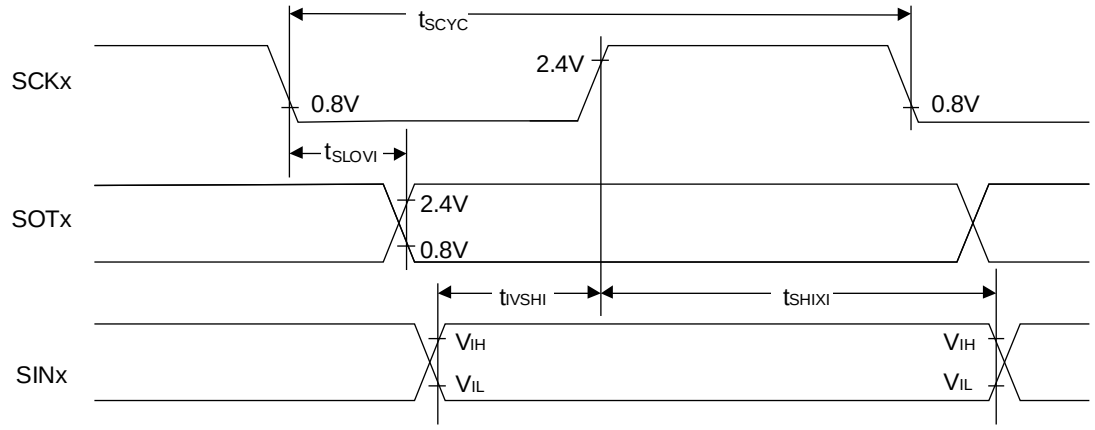
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"L" level output voltage	V_{OL1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	$V_{CC}5$ = 4.5V I_{OL} = 1.0mA	0	–	0.4	V	
	V_{OL2}		$V_{CC}5$ = 4.5V I_{OL} = 2.0mA	0	–	0.4	V	
	V_{OL3}	P060 to P067, P070 to P077, P080 to P087	DV_{CC} = 4.5V I_{OL} = 30.0mA	0	–	0.55	V	SMC shared pin
	V_{OL4}	P127, P130, P132, P133	$V_{CC}5$ = 4.5V I_{OL} = 3.0mA	0	–	0.4	V	I^2C shared pin (I^2C is selected)
	V_{OL5}	DEBUGIF	$V_{CC}5$ = 2.7V I_{OL} = 25.0mA	0	–	0.25	V	
	V_{OL6}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	$V_{CC}3$ = 3.0V I_{OL} = 2.0mA	0	–	0.4	V	3.3V dedicated pin
	V_{OL7}		$V_{CC}3$ = 3.0V I_{OL} = 5.0mA					
	V_{OL8}		$V_{CC}3$ = 3.0V I_{OL} = 10.0mA					
	V_{OL9}		$V_{CC}3$ = 3.0V I_{OL} = 20.0mA					
	V_{OL10}	TDO	$V_{CC}5$ = 4.5V I_{OH} = 5.0mA	0	–	0.4	V	BGA product only

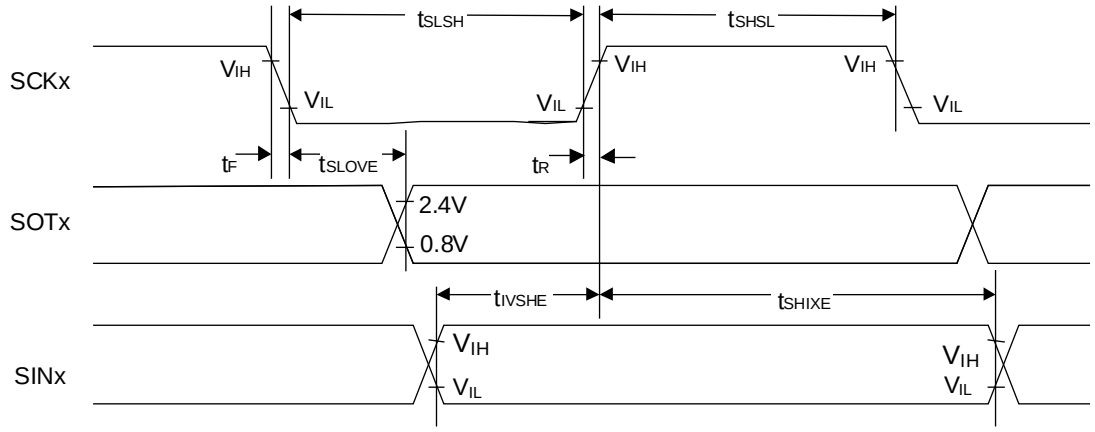
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	II_L	All input pins	VCC=DVCC=AVCC=5.5V VSS<VI<VCC	-5	–	+5	µA	
Pull-up resistance	R_{UP1}	RSTX, NMIX	–	25	–	100	kΩ	
	R_{UP2}	All 5V port input pins	Pull-up resistance is selected	25	–	100	kΩ	
	R_{UP3}	All 3V port input pins	Pull-up resistance is selected	17	–	66	kΩ	
Pull-down resistance	R_{DOWN1}	MD2	–	25	–	100	kΩ	
	R_{DOWN2}	All 5V port input pins	Pull-down resistance is selected	25	–	100	kΩ	
	R_{DOWN3}	All 3V port input pins	Pull-down resistance is selected	17	–	66	kΩ	
Input capacitance	C_{IN1}	Other than $V_{CC}3$, $V_{CC}5$, V_{SS}, DV_{CC}, DV_{SS}, $AV_{CC}3$,$AV_{SS}3$, $AV_{CC}5$,$AV_{SS}5$, C1,C2,C3, P060 to P067, P070 to P077, P080 to P087	–	–	5	15	pF	
	C_{IN2}	P060 to P067, P070 to P077, P080 to P087	When using SMC	–	15	45	pF	

• Internal shift clock mode



• External shift clock mode



11.4.1.12 External memory interface

Memory Controller

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip Select delay time	t_{cso}	MEM_XCS0, MEM_XCS1	12pF/10mA	–	18	ns	*1
				–	14	ns	*2
Address delay time	t_{ao}	MEM_EA[24:0]		–	18	ns	*1
				–	14	ns	*2
Data output delay time	t_{do}	MEM_ED[15:0]		–	18	ns	*1
				–	17	ns	*2
Data output → HiZ time	t_{doz}			–	18	ns	*1
				–	17	ns	*2
NOR Flash data setup time	t_{dsr}			20	–	ns	*1
				11	–	ns	*2
NOR Flash data hold time	t_{dhr}			0	–	ns	*1
				0	–	ns	*2
NOR Flash page Read data setup time	t_{dsp}			20	–	ns	*1
				8.5	–	ns	*2
NOR Flash page Read data hold time	t_{dhp}			0	–	ns	*1
				0	–	ns	*2
XRD delay time	t_{rdo}	MEM_XRD		–	18	ns	*1
				–	14	ns	*2
XWR delay time	t_{wro}	MEM_XWR		–	18	ns	*1
				–	14	ns	*2

Output delay is reference clock is an internal clock. The reference clock of MEM_RDY is an internal clock.

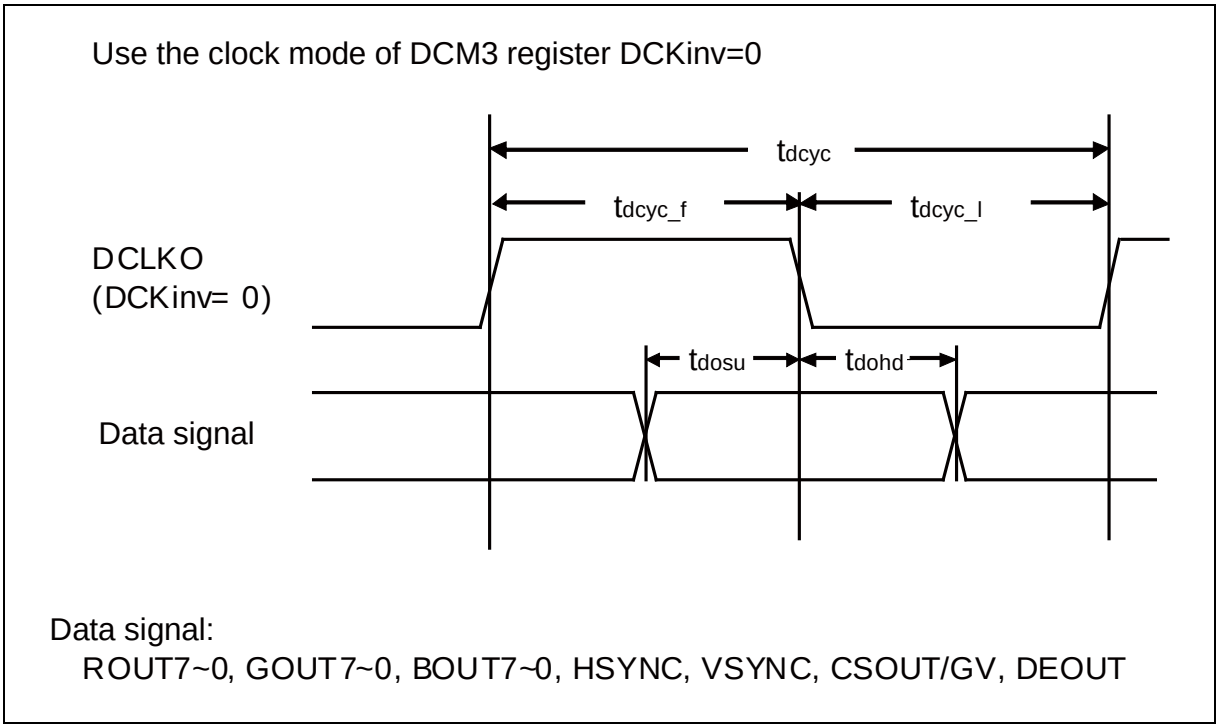
*1: MB91F591/2/4/6/7/9

*2: MB91F59A/B

DCLKI Input Standard Mode (DCM3.DCKinv=0)

Figure 8 shows the setup/hold definition when the external display device (TFT) receives the signal at the falling edge of DCLKO.

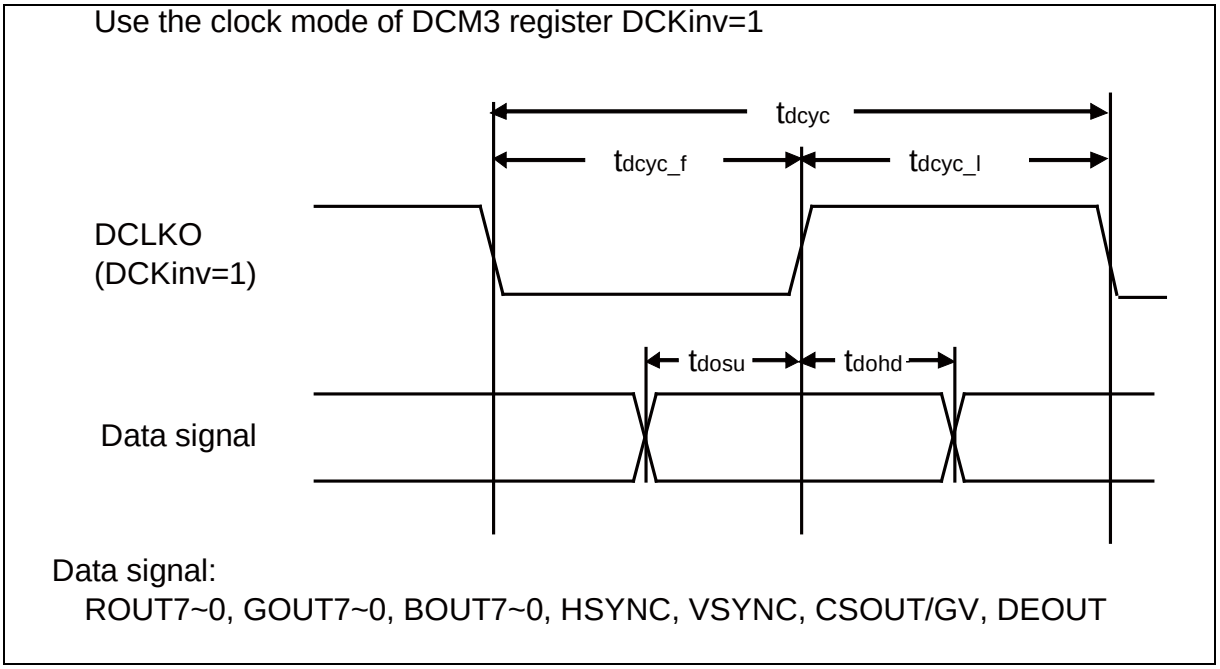
Figure 8. DCLKI Input Standard Mode Setup/Hold Definition



DCLKI Input Reverse Edge Mode (DCM3.DCKinv=1)

Figure 9 shows the setup/hold definition when the external display device (TFT) receives the signal at the rising edge of DCLKO.

Figure 9. DCLKI Input Reverse Edge Mode Setup/Hold Definition



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**	-	NNAS	06/19/2015	Migrated to Cypress and assigned document number 002-04712. No change to document contents or format.
*A	5139796	NNAS	02/19/2016	Updated to Cypress format.
*B	5973870	HMIZ	12/01/2017	12. Ordering Information [Improve] Updated "Ordering Information" [Improve] Delete *2: Under consideration
				13. Package Dimensions [Improve] Updated PKG figure for LQR208, LET208 and BYA320
				Updated Sales page.