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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	848K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f592bpmc-gsk5e1

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Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>1</sup>	Function <sup>*2</sup>			
	P067	-		General-purpose I/O port			
	PWM2M1	-		SMC ch.1 output pin			
	AN15	-		ADC Analog 15 input pin			
134	UDCAIN0	-	E	Up/down counter ch.0 AIN input pin (MB91F59A/B only)			
	SIN9	-		Multi-function serial ch.9 serial data input pin(MB91F59A/B only)			
	P070	-		General-purpose I/O port			
	PWM1P2	-		SMC ch.2 output pin			
137	AN16	-	E	ADC Analog 16 input pin			
	SOT9	-		Multi-function serial ch.9 serial data output pin(MB91F59A/B only)			
	P071	-		General-purpose I/O port			
138	PWM1M2	-	]  E	SMC ch.2 output pin			
130	AN17	-	]=	ADC Analog 17 input pin			
	SCK9	-	-	Multi-function serial ch.9 clock I/O pin(MB91F59A/B only)			
	P072	-		General-purpose I/O port			
	PWM2P2	-		SMC ch.2 output pin			
139	AN18	-	E	ADC Analog 18 input pin			
100	39 SIN8			Multi-function serial ch.8 serial data input pin(MB91F59A/B only)			
	ICU11	-		Input capture ch.11 input pin(MB91F59A/B only)			
	P073	-		General-purpose I/O port			
	PWM2M2	-		SMC ch.2 output pin			
140	AN19	-	E	ADC Analog 19 input pin			
110	SOT8	-		Multi-function serial ch.8 serial data output pin(MB91F59A/B only)			
	ICU10	-		Input capture ch.10 input pin(MB91F59A/B only)			
	P074	-		General-purpose I/O port			
	PWM1P3	-		SMC ch.3 output pin			
141	AN20	-	-E	ADC Analog 20 input pin			
141	PPG12_1	-	]_	PPG ch.12 output pin (1)			
	SCK8	-		Multi-function serial ch.8 clock I/O pin(MB91F59A/B only)			
	ICU9	-		Input capture ch.9 input pin(MB91F59A/B only)			
	P075	-		General-purpose I/O port			
	PWM1M3	-		SMC ch.3 output pin			
142	AN21	-	E	ADC Analog 21 input pin			
142	SIN7_1	-		LIN-UART ch.7 serial data input pin			
	PPG13_1	-		PPG ch.13 output pin (1)			
	ICU8	-		Input capture ch.8 input pin(MB91F59A/B only)			
	P076	-	_	General-purpose I/O port			
	PWM2P3	-	1	SMC ch.3 output pin			
143	AN22	-	E	ADC Analog 22 input pin			
10	SOT7_1	-	1-	LIN-UART ch.7 serial data output pin			
	PPG14_1	-	1	PPG ch.14 output pin (1)			
	ICU7	-		Input capture ch.7 input pin(MB91F59A/B only)			





Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>1</sup>	Function <sup>*2</sup>
	P087	-		General-purpose I/O port
	PWM2M5	-		SMC ch.5 output pin
154	AN31	-	E	ADC Analog 31 input pin
	ICU4_2	-		Input capture ch.4 input pin (2)
	PPG23	-		PPG ch.23 output pin
	P090	-		General-purpose I/O port
157	ADTG	-	A	A/D convertor external trigger input pin
157	PPG0_2		A	PPG ch.0 output pin (2)
	TIN7_1	-		Reload timer ch.7 event input pin (1) (MB91F59A/B only)
	P091	-		General-purpose I/O port
	SGA0	-		Sound generator ch.0 SGA output pin
	SIN2	-		LIN-UART ch.2 serial data input pin
98	INT12	-	С	INT12 External interrupt input pin
	TOT2_1	-		Reload timer ch.2 output pin (1)
	ICU2_1	-		Input capture ch.2 input pin (1)
	PPG6_1	-		PPG ch.6 output pin (1)
	P092	-		General-purpose I/O port
	SGO0	-		Sound generator ch.0 SGO output pin
	SCK2	-		LIN-UART ch.2 clock I/O pin
99	INT13	-	С	INT13 External interrupt input pin
	TOT3_1	-		Reload timer ch.3 output pin (1)
	ICU0_1	-	-	Input capture ch.0 input pin (1)
	PPG7_1	-		PPG ch.7 output pin (1)
	P093	-		General-purpose I/O port
	SGA1	-		Sound generator ch.1 SGA output pin
	SOT2	-		LIN-UART ch.2 serial data output pin
100	INT14	-	С	INT14 External interrupt input pin
	ICU3_1	-		Input capture ch.3 input pin (1)
	PPG8_1	-		PPG ch.8 output pin (1)
	TIN8_1	-		Reload timer ch.8 event input pin (1) (MB91F59A/B only)
	P094	-		General-purpose I/O port
	SGO1	-		Sound generator ch.1 SGO output pin
	SIN3	-		LIN-UART ch.3 serial data input pin
160	INT15	-	С	INT15 External interrupt input pin
	ICU1_1	-		Input capture ch.1 input pin (1)
	PPG9_1	-		PPG ch.9 output pin (1)
	TIN9_1	-		Reload timer ch.9 event input pin (1) (MB91F59A/B only)
	P095	-		General-purpose I/O port
106	TX0	-	А	CAN transmission data0 output pin
	PPG10_1	-	1	PPG ch.10 output pin (1)
	P096	-		General-purpose I/O port
107	RX0	-	А	CAN reception data0 input pin
	INT9	-	1	INT9 External interrupt input pin



Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>*1</sup>	Function <sup>*2</sup>	
13	PE7	-	0	General-purpose I/O port (3V pin)	
15	GOUT7	-	0	Display digital G7 output pin	
14	PF2	-	0	General-purpose I/O port (3V pin)	
14	BOUT2	-	0	Display digital B2 output pin	
45	PF3	-	0	General-purpose I/O port (3V pin)	
15	BOUT3	-	0	Display digital B3 output pin	
40	PF4	-		General-purpose I/O port (3V pin)	
16	BOUT4	-	0	Display digital B4 output pin	
	PF5	-		General-purpose I/O port (3V pin)	
17	BOUT5	-	0	Display digital B5 output pin	
	PF6	_	-	General-purpose I/O port (3V pin)	
21	BOUT6	_	0	Display digital B6 output pin	
	PF7	_		General-purpose I/O port(3V pin)	
22	BOUT7	_	0	Display digital B7 output pin	
	PG0	_		General-purpose I/O port (3V pin)	
200	DCKIN	-	0	Display reference clock input pin (for External sync)	
200	CMDTRG			GDC command trigger input pin	
	PG1			General-purpose I/O port (3V pin)	
197	VSIN	P	0	Capture vertical sync signal input pin	
		F			
198	PG2	-	0	General-purpose I/O port (3V pin)	
	HSIN	Р		Capture horizontal sync signal input pin	
100	PG3	-		General-purpose I/O port (3V pin)	
199	CSOUT	-	0	Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin	
23	PG4	-	0	General-purpose I/O port (3V pin)	
25	DCKOUT	-	U	Display reference clock output pin (for Internal sync)	
	PG5	-		General-purpose I/O port (3V pin)	
24	VSYNC	-	0	Display vertical sync signal output pin (for Internal sync)/Display vertical sync signal input pin (for External sync)	
	PG6	-		General-purpose I/O port (3V pin)	
25	HSYNC	_	0	Display horizontal sync signal output pin (for Internal sync)/Display horizontal sync signal input pin (for External sync)	
	PG7	-		General-purpose I/O port (3V pin)	
26	DEOUT	Р	0	Display enable display period output pin	
	PH3	_	-	General-purpose I/O port (3V pin)	
196	CCLK	_	0	For capture, capture clock input pin	
204	REFOUT	_	т	Clamp level output pin	
203	AVR3	_	S	"L" side reference voltage for NTSC A/D converter pin	
205	VIN	_	S	NTSC signal input pin	
111	AVCC5	-	-	AD convertor analog power supply pin	
201, 207	AVCC3		_	For NTSC, AD convertor analog power supply pin	
112	AVCC3 AVRH5		_	AD convertor upper limit reference voltage pin	
112	AVRH5 AVSS5/	-	-		
113	AVRL5	-	-	AD convertor GND/ AD convertor lower limit reference voltage pin	
202, 206	AVSS3	-	-	NTSC AD convertor GND pin	
124	C_1	-	-	Built-in regulator capacitor connected pin 1	
73	C_2	-	-	Built-in regulator capacitor connected pin 2	
20	C_3	<b>—</b>	-	Built-in regulator capacitor connected pin 3	



## 3.2 MB91F59A/B (BGA320)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>*1</sup>	Function <sup>*2</sup>
1	VSS	-	-	GND pin
2	VSS	-	-	GND pin
3	AVCC3	-	-	For NTSC, AD convertor analog power supply pin
4	VIN	_	S	NTSC signal input pin
5	REFOUT	_	Т	Clamp level output pin
6	AVCC3	_	_	For NTSC, AD convertor analog power supply pin
	BIN5			Capture B5 input pin (RGB mode)
7	PC5	1-	0	General-purpose I/O port (3V pin)
_	BIN2			Capture B2 input pin (RGB mode)
8	PC2	1-	0	General-purpose I/O port (3V pin)
_	GIN5			Capture G5 input pin (RGB mode)
9	PB5	-	0	General-purpose I/O port (3V pin)
	GIN2			Capture G2 input pin (RGB mode)
10	VIN6	<b> </b> _	0	Capture VIN6 input pin (656 mode)
	PB2		_	General-purpose I/O port (3V pin)
	RIN5			Capture R5 input pin (RGB mode)
11	VIN3	1_	0	Capture VIN3 input pin (656 mode)
	PA5	-	•	General-purpose I/O port (3V pin)
	RIN2			Capture R2 input pin (RGB mode)
12	VINO	1_	0	Capture VIN0 input pin (656 mode)
	PA2	-	Ũ	General-purpose I/O port (3V pin)
13	VSS	_	_	GND pin
	P136		A	General-purpose I/O port (Single clock product)
14	(X1A)	-	N	Sub clock oscillation output pin (Dual clock product)
	P137	_	A	General-purpose I/O port (Single clock product)
15	(X0A)	_	N	Sub clock oscillation input pin (Dual clock product)
16	VSS	_	-	GND pin
10	P094			General-purpose I/O port
	ICU1_1	-		Input capture ch.1 input pin (1)
	INT15	-		INT15 External interrupt input pin
17	SIN3	l_	с	LIN-UART ch.3 serial data input pin
17	PPG9_1		Ŭ	PPG ch.9 output pin (1)
	TIN9_1			Reload timer ch.9 event input pin (1)
	SGO1			Sound generator ch.1 SGO output pin
	ADTG			A/D convertor external trigger input pin
	P090	-		General-purpose I/O port
18	P090 PPG0_2	-	А	PPG ch.0 output pin (2)
10	TIN7_1		11	Reload timer ch.7 event input pin (1)
19	TCK	-	U	Test Clock (JTAG Boundary Scan Test)
20	VSS	-	-	GND pin
21	TMS	-	U	Test Mode State (JTAG Boundary Scan Test)
22	TDO	-	W	Test Data Out (JTAG Boundary Scan Test)
	AN31	-		ADC Analog 31 input pin
23	P087	-	Е	General-purpose I/O port
	ICU4_2	4		Input capture ch.4 input pin (2)
L	PPG23			PPG ch.23 output pin
23	PWM2M5	-	E	SMC ch.5 output pin



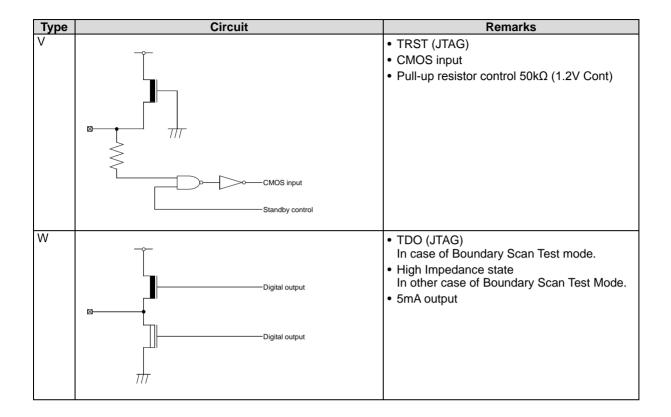


BGA Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>*1</sup>	Function <sup>*2</sup>
	AN28			ADC Analog 28 input pin
	P084			General-purpose I/O port
24	ICU1_2		-	Input capture ch.1 input pin (2)
24	PPG20	_	E	PPG ch.20 output pin
	PWM1P5			SMC ch.5 output pin
	UDCBIN2			Up/down counter ch.2 BIN input pin
	AN25			ADC Analog 25 input pin
	P081			General-purpose I/O port
25	SOT6		-	LIN-UART ch.6 serial data output pin
25	PPG17	_	E	PPG ch.17 output pin
	PWM1M4			SMC ch.4 output pin
	UDCBIN0_1			Up/down counter ch.0 BIN input pin (1)
	AN22			ADC Analog 22 input pin
	P076			General-purpose I/O port
	ICU7		_	Input capture ch.7 input pin
26	SOT7_1	-	E	LIN-UART ch.7 serial data output pin
	PPG14_1			PPG ch.14 output pin (1)
	PWM2P3			SMC ch.3 output pin
	AN19			ADC Analog 19 input pin
	P073			General-purpose I/O port
27	ICU10	_	E	Input capture ch.10 input pin
	SOT8	-		Multi-function serial ch.8 serial data output pin
	PWM2M2	-		SMC ch.2 output pin
	AN16			ADC Analog 16 input pin
	P070		_	General-purpose I/O port
28	SOT9	-	E	Multi-function serial ch.9 serial data output pin
	PWM1P2			SMC ch.2 output pin
	AN13			ADC Analog 13 input pin
	P065		_	General-purpose I/O port
29	PWM1M1	-	E	SMC ch.1 output pin
	UDCZIN0			Up/down counter ch.0 ZIN input pin
	AN10			ADC Analog 10 input pin
	P062			General-purpose I/O port
30	SCK10	_	E	Multi-function serial ch.10 clock I/O pin
	PWM2P0	-	_	SMC ch.0 output pin
	UDCZIN1			Up/down counter ch.1 ZIN input pin
31	VSS	_	_	GND pin
32	C_1	_	_	Built-in regulator capacitor connected pin 1
	AN5			ADC Analog 5 input pin
	P105			General-purpose I/O port
	ICU9_1	1		Input capture ch.9 input pin (1)
33	SCK5_1	-	С	LIN-UART ch.5 clock I/O pin (1)
	PPG3_1			PPG ch.3 output pin (1)
	TOT1_1	1		Reload timer ch.1 output pin (1)
	AVSS5			A/D convertor GND
34	AVRL5	-	-	A/D convertor lower limit reference voltage pin
35	AVRE5	_	_	A/D convertor upper limit reference voltage pin
55				The convertor upper minic relevence voltage pill



BGA Pin No.	Pin Name	Polarity	I/O Circuit Types <sup>1</sup>	Function <sup>*2</sup>
	SOT5			LIN-UART ch.5 serial data output pin
155	PPG6_2	_	С	PPG ch.6 output pin (2)
	TOT2			Reload timer ch.2 output pin
	FRCK1			Free-run timer 1 clock input pin
	P120			General-purpose I/O port
450	INT6			INT6 External interrupt input pin
156	SIN5	]_	С	LIN-UART ch.5 serial data input pin
	PPG5_2			PPG ch.5 output pin (2)
	TOT1			Reload timer ch.1 output pin
	FRCK3			Free-run timer 3 clock input pin
	P116			General-purpose I/O port
157	SOT4	1_	С	LIN-UART ch.4 serial data output pin
	TIN3	-		Reload timer ch.3 event input pin
	SGA3			Sound generator ch.3 SGA output pin
	P097			General-purpose I/O port
158	ICU4_1			Input capture ch.4 input pin (1)
	INT8			INT8 External interrupt input pin
	SOT3	1_	С	LIN-UART ch.3 serial data output pin
158	PPG0_1		Ũ	PPG ch.0 output pin (1)
100				Reload timer ch.0 event input pin
	WOT			RTC overflow output pin
	TX2			CAN transmission data 2 output pin
	P112			General-purpose I/O port
159	PPG3_2	-	С	PPG ch.3 output pin (2)
	TOT10_1			Reload timer ch.10 output pin (1)
160	VSS			GND pin
100	AN29	-	-	ADC Analog 29 input pin
	P085			General-purpose I/O port
	ICU2_2	_		Input capture ch.2 input pin (2)
161	PPG21	-	E	
		-		PPG ch.21 output pin
	PWM1M5			SMC ch.5 output pin
	UDCAIN2			Up/down counter ch.2 AIN input pin
	AN26			ADC Analog 26 input pin
	P082			General-purpose I/O port
162	SCK6	-	E	LIN-UART ch.6 clock I/O pin
	PPG18			PPG ch.18 output pin
	PWM2P4			SMC ch.4 output pin
	UDCZIN0_1			Up/down counter ch.0 ZIN input pin (1)
	AN23	-		ADC Analog 23 input pin
	P077	4		General-purpose I/O port
163	ICU6	-	E	Input capture ch.6 input pin
	SCK7_1	4		LIN-UART ch.7 clock I/O pin
	PPG15_1	-		PPG ch.15 output pin (1)
	PWM2M3			SMC ch.3 output pin
	AN20	1		ADC Analog 20 input pin
164	P074	-	E	General-purpose I/O port
	ICU9			Input capture ch.9 input pin
	SCK8			Multi-function serial ch.8 clock I/O pin
164	PPG12_1	-	E	PPG ch.12 output pin (1)
	PWM1P3			SMC ch.3 output pin

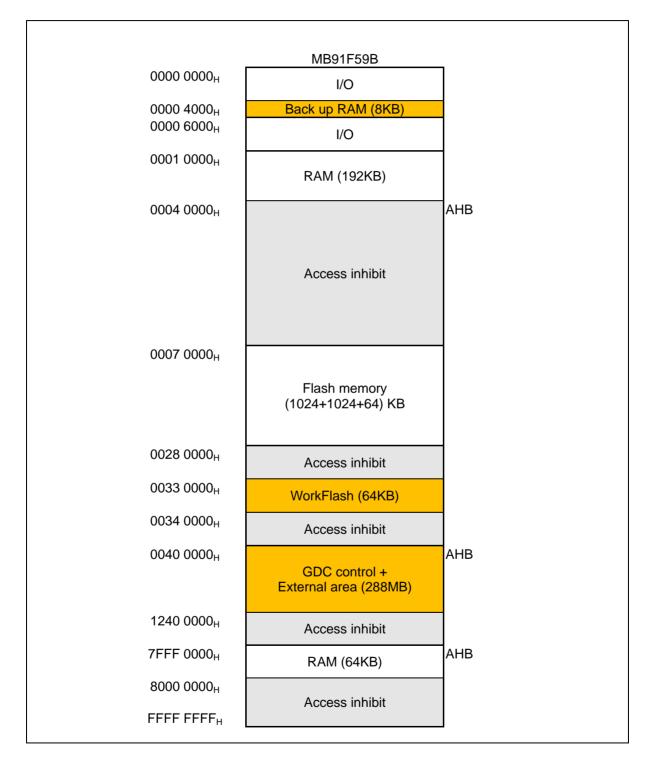






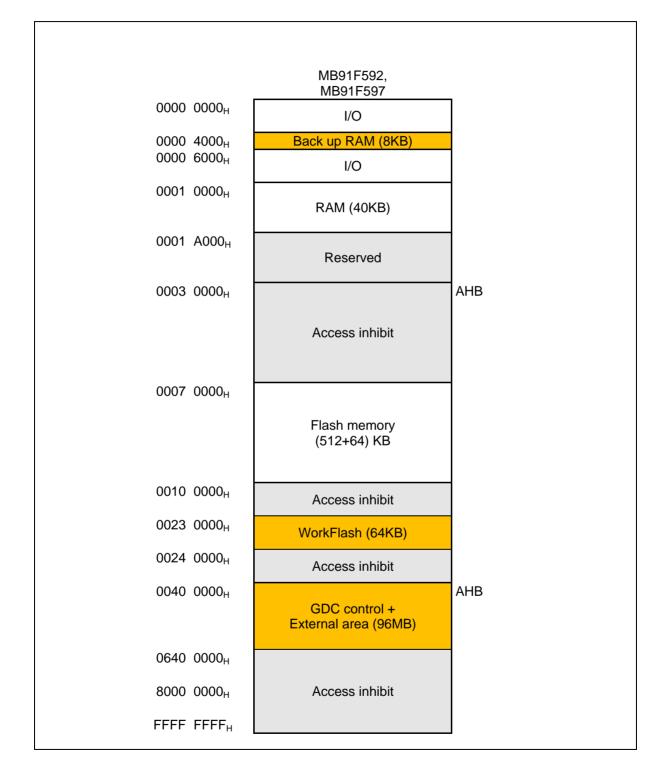
## 8. Memory Map

Memory map





#### Memory map





- <sup>\*1</sup>: Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.
- \*2: The status of the multi-function serial interface does not support a DMA transfer caused by I<sup>2</sup>C reception.
- <sup>\*3</sup>: The clock calibration unit does not support a DMA transfer caused by an interrupt.
- <sup>\*4</sup>: RAM ECC bit error does not support a DMA transfer caused by an interrupt.
- \*5: REALOS is a trademark of Cypress
- <sup>\*6</sup>: An interrupt of Up/down counter ch.2 does not support a DMA transfer.
- <sup>\*7</sup>: An interrupt related GDC does not support a DMA transfer.
- \*\*: Only supported by MB91F59A/B

UDCn: Up/down counter ch.n ICUn: Input capture unit.n OCUn: Output compare unit.n



(T <sub>A</sub> : Recommended operating conditions, V <sub>CC</sub> 5=5.0V ± 10%, V <sub>CC</sub> 3=3.3V ± 10%, V <sub>SS</sub> =										
Parameter	Symbol	Pin Name	Conditions	Min	Value Typ	Max	Unit	Remarks		
	V <sub>OH1</sub>	P060 to P067, P070 to P077, P080 to P087, P090 to P097,	V <sub>CC</sub> 5 = 4.5V I <sub>OH</sub> = -1.0mA	V <sub>cc</sub> 5- 0.5	-	V <sub>CC</sub> 5	v			
	V <sub>OH2</sub>	P100 to P107, P110 to P117, P120 to P127, P130 to P137	V <sub>CC</sub> 5 = 4.5V I <sub>OH</sub> = -2.0mA	V <sub>CC</sub> 5- 0.5	_	V <sub>CC</sub> 5	v			
	V <sub>OH3</sub>	P060 to P067, P070 to P077, P080 to P087	DV <sub>CC</sub> = 4.5V I <sub>OH</sub> = -30.0mA	DV <sub>CC</sub> - 0.5	_	DV <sub>cc</sub>	v	SMC shared pin		
"H" level output voltage	V <sub>OH4</sub>	P000 to P007, P010 to P017, P020 to P027, P030 to P037,	V <sub>CC</sub> 3 = 3.0V I <sub>OH</sub> = -2.0mA	V <sub>cc</sub> 3- 0.5		V <sub>cc</sub> 3	v	3.3V dedicated pin		
	V <sub>OH5</sub>		V <sub>CC</sub> 3 = 3.0V I <sub>OH</sub> = -5.0mA							
	V <sub>OH6</sub>		V <sub>CC</sub> 3 = 3.0V I <sub>OH</sub> = -10.0mA		_					
	V <sub>OH7</sub>	PF2 to PF7, PG0 to PG7, PH3	V <sub>CC</sub> 3 = 3.0V I <sub>OH</sub> = -20.0mA							
	V <sub>OH8</sub>	TDO	V <sub>CC</sub> 5 = 4.5V I <sub>OH</sub> = -5.0mA	V <sub>CC</sub> 5- 0.5	_	V <sub>CC</sub> 5	V	BGA product only		

(	T <sub>A</sub> : Recommend	ed operating cond	itions, $V_{CC}5=5.0V$	± 10%, V <sub>CC</sub>	3=3.3V ± 10%,	, V <sub>SS</sub> =DV <sub>SS</sub> =,	AV <sub>SS</sub> =0.0V)



## 11.4.1.3 Power-on Conditions

(T<sub>A</sub>: Recommended operating conditions, V<sub>SS</sub>=0.0V)

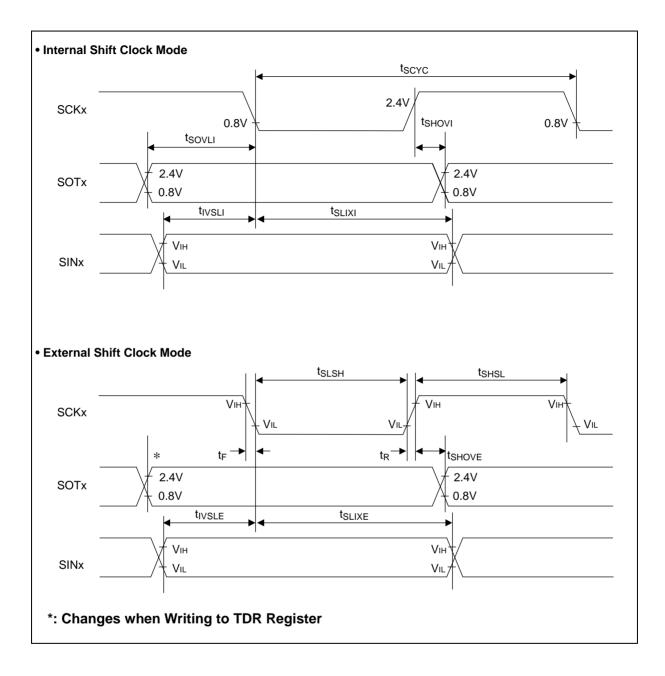
Parameter	Symbol	Pin	Conditions		Value			Remarks
Farameter	Symbol	Name	Conditions	Min	Тур	Max	Unit	Rellidiks
Level detection voltage	_	V <sub>CC</sub> 5	_	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	-	$V_{CC}5$	-	-	-	125	mV	During voltage drop
Level detection time	-	-	-	-	-	30	us	*1
Specification for voltage slope detection	_	V <sub>CC</sub> 5	V <sub>CC</sub> 5 = at level detection release level time	_	_	4	mV/µs	*2
Power off time	t <sub>OFF</sub>	V <sub>cc</sub> 5	-	50	-	-	ms	*3

<sup>\*1</sup>: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

<sup>\*2</sup>: When setting the power supply fluctuation to this specification or less, it is possible to suppress the voltage slope detection. This is the specification when the power supply fluctuation is stable.

<sup>\*3</sup>: This time is to start the voltage slope detection at next power on after power down and internal charge loss.







■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1 (T<sub>A</sub>: Recommended operating conditions, V<sub>CC</sub>5=5.0V ± 10%, V<sub>SS</sub>=AV<sub>SS</sub>=0.0V)

Parameter	Symbol	Din Nama	Pin Name Conditions			Unit
Parameter	Symbol	Fin Name	Min	Max	Unit	
Serial clock cycle time	tscyc	SCKx		4t <sub>CPP</sub>	-	ns
$\begin{array}{l} SCK \downarrow \to SOT \text{ delay} \\ time \end{array}$	t <sub>SLOVI</sub>	SCKx, SOTx	Internal shift clock mode	-30	+30	ns
Valid SIN $\rightarrow$ SCK $\uparrow$ setup time	t <sub>IVSHI</sub>		capability is 2mA or more.)	34	_	ns
$\begin{array}{l} SCK \uparrow \rightarrow \\ Valid \ SIN \ hold \ time \end{array}$	t <sub>SHIXI</sub>	SCRX, SIINX	CKx, SINx C <sub>L</sub> =20pF(When drive capability is 1mA)			ns
$\begin{array}{l} \text{SOT} \rightarrow \text{SCK} \uparrow \text{delay} \\ \text{time} \end{array}$	t <sub>SOVHI</sub>	SCKx, SOTx		2t <sub>CPP</sub> -30	_	ns
Serial clock "H"pulse width	t <sub>SHSL</sub>	SCKx		t <sub>CPP</sub> +10	_	ns
Serial clock "L" pulse width	t <sub>SLSH</sub>	SUNX	External shift clock mode	2t <sub>CPP</sub> -10	_	ns
$\begin{array}{l} SCK \downarrow \to SOT \text{ delay} \\ time \end{array}$	t <sub>SLOVE</sub>	SCKx, SOTx	C <sub>L</sub> =50pF(When drive	-	33	ns
Valid SIN $\rightarrow$ SCK $\uparrow$ setup time	t <sub>IVSHE</sub>	SCKx, SINx	capability is 2mA or more.) C <sub>L</sub> =20pF(When drive capability is 1mA)	10	_	ns
$\begin{array}{l} SCK \uparrow \rightarrow \\ Valid \; SIN \; hold \; time \end{array}$	t <sub>SHIXE</sub>			20	_	ns
SCK fall time	t <sub>F</sub>	SCKx	< <u>x</u>		5	ns
SCK rise time	t <sub>R</sub>	SCKx		-	5	ns

### Notes:

- AC characteristic in CLK synchronized mode.
- C<sub>L</sub> is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.



## ■Bit setting: ESCR: SCES=1, ECCR: SCDE=0

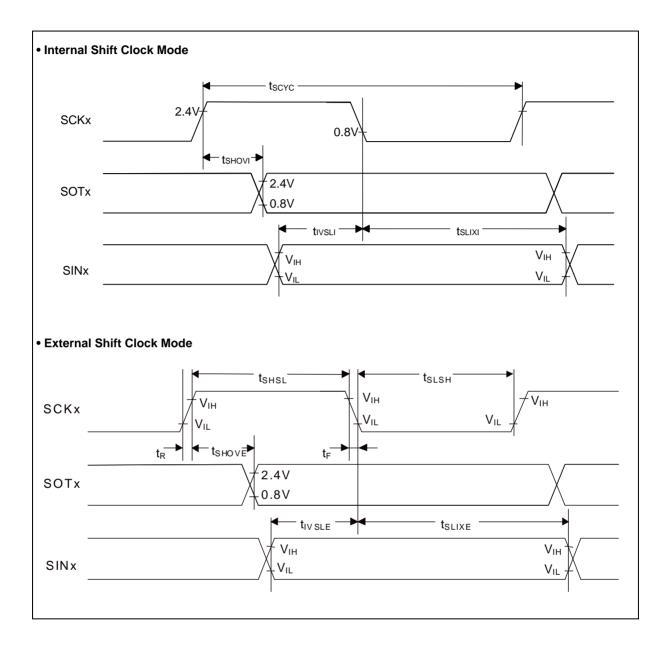
Parameter	Symbol	Pin Name	Conditions		lue	Unit	Remarks
Farameter	Symbol	Fin Name	Conditions	Min	Max	Unit	Relliarks
Serial clock cycle time	tscyc	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		5t <sub>CPP</sub>	-	ns	
SCK ↑ → SOT delay time	t <sub>shovi</sub>	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7	_	-50	+50	ns	Internal shift clock mode: C∟=80pF+1 ∙ TTL
Valid SIN $\rightarrow$ SCK $\downarrow$ setup time	t <sub>IVSLI</sub>	SCK2,SCK3, SCK4,SCK5,		t <sub>CPP</sub> +80	-	ns	
SCK ↓ → Valid SIN hold time	t <sub>SLIXI</sub>	SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		0	-	ns	
Serial clock "H" pulse width	t <sub>SHSL</sub>	SCK2,SCK3, SCK4,SCK5,		3t <sub>CPP</sub> -t <sub>R</sub>	_	ns	
Serial clock "L" pulse width	t <sub>SLSH</sub>	SCK6,SCK7		t <sub>CPP</sub> +10	-	ns	
SCK ↑ → SOT delay time	t <sub>SHOVE</sub>	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7	_	_	2t <sub>CPP</sub> +60	ns	External shift clock mode:
Valid SIN → SCK ↓ setup time	t <sub>IVSLE</sub>	SCK2,SCK3, SCK4,SCK5,		30	-	ns	C <sub>L</sub> =80pF+1 ● TTL
SCK ↓ → Valid SIN hold time	t <sub>SLIXE</sub>	SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t <sub>CPP</sub> +30	_	ns	
SCK fall time	t <sub>F</sub>	SCK2,SCK3,	1	-	10	ns	
SCK rise time	t <sub>R</sub>	SCK4,SCK5, SCK6,SCK7		_	40	ns	

## (T<sub>A</sub>: Recommended operating conditions, $V_{CC}5=5.0V \pm 10\%$ , $V_{SS}=AV_{SS}=0.0V$ )

#### Notes:

- C<sub>L</sub> is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.







## AC Characteristics of Display Output Signal

#### Clock Mode

There are multiple clock modes for display output clocks, as shown in Table 1. The AC timing parameters vary depending on modes. The AC timing parameters are specified for each mode.

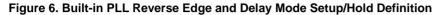
## Table 1. Clock Mode for Display Output

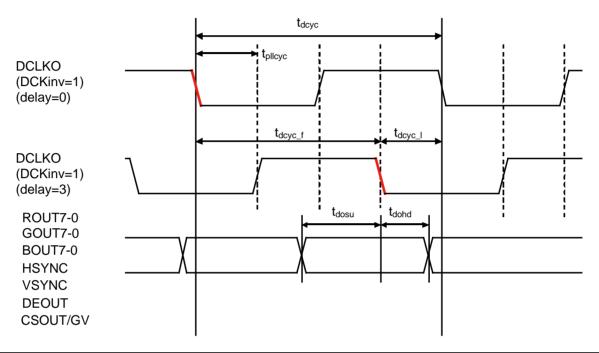
	Setting Reg	ister Bit Field				
DCM1	DCM3			Clock Mode Name		
CKS	DCKed	DCKD	DCKinv			
0	0	0	0	Built-in PLL standard mode		
0	0	0	1	Built-in PLL reverse edge mode		
0	1	0	0	Cannot be used.		
0	1	0	1	Cannot be used.		
0	0	Other than 0	0	Built-in PLL delay mode		
0	0	Other than 0	1	Built-in PLL reverse edge and delay mode		
0	1	Other than 0	0	Duilt in DLL both adda and delay made		
0	1	Other than 0	1	Built-in PLL both edge and delay mode		
1	0	0	0	DCLKI input standard mode		
1	0	0	1	DCLKI input reverse edge mode		
1	1	0	0			
1	1	0	1			
1	0	Other than 0	0	Connethe wood		
1	0	Other than 0	1	Cannot be used.		
1	1	Other than 0	0			
1	1	Other than 0	1			



#### Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

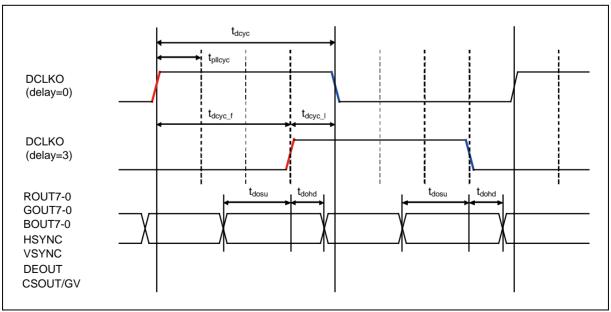




Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition





## 11.4.1.14 GDC ommand trigger signal

Parameter	Symbol	Pin Name	Val Min	lue Max	Unit	Remarks		
Input trigger pulse width	Ttrg	CMDTRG	160		ns			
	Ttrg							
			iug					



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