Infineon Technologies - MB91F592BPMC-GSK5E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	848K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f592bpmc-gsk5e1

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
134	P067	–	E	General-purpose I/O port
	PWM2M1	–		SMC ch.1 output pin
	AN15	–		ADC Analog 15 input pin
	UDCAIN0	–		Up/down counter ch.0 AIN input pin (MB91F59A/B only)
	SIN9	–		Multi-function serial ch.9 serial data input pin(MB91F59A/B only)
137	P070	–	E	General-purpose I/O port
	PWM1P2	–		SMC ch.2 output pin
	AN16	–		ADC Analog 16 input pin
	SOT9	–		Multi-function serial ch.9 serial data output pin(MB91F59A/B only)
138	P071	–	E	General-purpose I/O port
	PWM1M2	–		SMC ch.2 output pin
	AN17	–		ADC Analog 17 input pin
	SCK9	–		Multi-function serial ch.9 clock I/O pin(MB91F59A/B only)
139	P072	–	E	General-purpose I/O port
	PWM2P2	–		SMC ch.2 output pin
	AN18	–		ADC Analog 18 input pin
	SIN8	–		Multi-function serial ch.8 serial data input pin(MB91F59A/B only)
	ICU11	–		Input capture ch.11 input pin(MB91F59A/B only)
140	P073	–	E	General-purpose I/O port
	PWM2M2	–		SMC ch.2 output pin
	AN19	–		ADC Analog 19 input pin
	SOT8	–		Multi-function serial ch.8 serial data output pin(MB91F59A/B only)
	ICU10	–		Input capture ch.10 input pin(MB91F59A/B only)
141	P074	–	E	General-purpose I/O port
	PWM1P3	–		SMC ch.3 output pin
	AN20	–		ADC Analog 20 input pin
	PPG12_1	–		PPG ch.12 output pin (1)
	SCK8	–		Multi-function serial ch.8 clock I/O pin(MB91F59A/B only)
	ICU9	–		Input capture ch.9 input pin(MB91F59A/B only)
142	P075	–	E	General-purpose I/O port
	PWM1M3	–		SMC ch.3 output pin
	AN21	–		ADC Analog 21 input pin
	SIN7_1	–		LIN-UART ch.7 serial data input pin
	PPG13_1	–		PPG ch.13 output pin (1)
	ICU8	–		Input capture ch.8 input pin(MB91F59A/B only)
143	P076	–	E	General-purpose I/O port
	PWM2P3	–		SMC ch.3 output pin
	AN22	–		ADC Analog 22 input pin
	SOT7_1	–		LIN-UART ch.7 serial data output pin
	PPG14_1	–		PPG ch.14 output pin (1)
	ICU7	–		Input capture ch.7 input pin(MB91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
154	P087	–	E	General-purpose I/O port
	PWM2M5	–		SMC ch.5 output pin
	AN31	–		ADC Analog 31 input pin
	ICU4_2	–		Input capture ch.4 input pin (2)
	PPG23	–		PPG ch.23 output pin
157	P090	–	A	General-purpose I/O port
	ADTG	–		A/D convertor external trigger input pin
	PPG0_2	–		PPG ch.0 output pin (2)
	TIN7_1	–		Reload timer ch.7 event input pin (1) (MB91F59A/B only)
98	P091	–	C	General-purpose I/O port
	SGA0	–		Sound generator ch.0 SGA output pin
	SIN2	–		LIN-UART ch.2 serial data input pin
	INT12	–		INT12 External interrupt input pin
	TOT2_1	–		Reload timer ch.2 output pin (1)
	ICU2_1	–		Input capture ch.2 input pin (1)
	PPG6_1	–		PPG ch.6 output pin (1)
99	P092	–	C	General-purpose I/O port
	SGO0	–		Sound generator ch.0 SGO output pin
	SCK2	–		LIN-UART ch.2 clock I/O pin
	INT13	–		INT13 External interrupt input pin
	TOT3_1	–		Reload timer ch.3 output pin (1)
	ICU0_1	–		Input capture ch.0 input pin (1)
	PPG7_1	–		PPG ch.7 output pin (1)
100	P093	–	C	General-purpose I/O port
	SGA1	–		Sound generator ch.1 SGA output pin
	SOT2	–		LIN-UART ch.2 serial data output pin
	INT14	–		INT14 External interrupt input pin
	ICU3_1	–		Input capture ch.3 input pin (1)
	PPG8_1	–		PPG ch.8 output pin (1)
	TIN8_1	–		Reload timer ch.8 event input pin (1) (MB91F59A/B only)
160	P094	–	C	General-purpose I/O port
	SGO1	–		Sound generator ch.1 SGO output pin
	SIN3	–		LIN-UART ch.3 serial data input pin
	INT15	–		INT15 External interrupt input pin
	ICU1_1	–		Input capture ch.1 input pin (1)
	PPG9_1	–		PPG ch.9 output pin (1)
	TIN9_1	–		Reload timer ch.9 event input pin (1) (MB91F59A/B only)
106	P095	–	A	General-purpose I/O port
	TX0	–		CAN transmission data0 output pin
	PPG10_1	–		PPG ch.10 output pin (1)
107	P096	–	A	General-purpose I/O port
	RX0	–		CAN reception data0 input pin
	INT9	–		INT9 External interrupt input pin

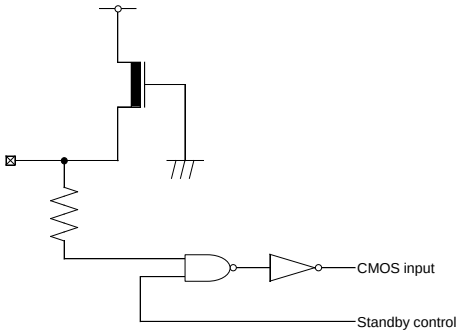
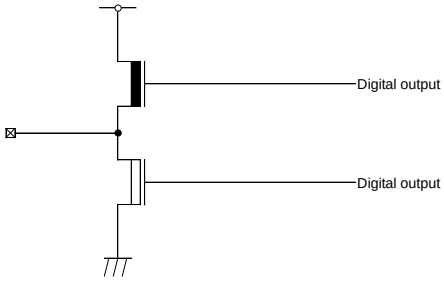
Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
13	PE7	–	O	General-purpose I/O port (3V pin)
	GOUT7	–		Display digital G7 output pin
14	PF2	–	O	General-purpose I/O port (3V pin)
	BOUT2	–		Display digital B2 output pin
15	PF3	–	O	General-purpose I/O port (3V pin)
	BOUT3	–		Display digital B3 output pin
16	PF4	–	O	General-purpose I/O port (3V pin)
	BOUT4	–		Display digital B4 output pin
17	PF5	–	O	General-purpose I/O port (3V pin)
	BOUT5	–		Display digital B5 output pin
21	PF6	–	O	General-purpose I/O port (3V pin)
	BOUT6	–		Display digital B6 output pin
22	PF7	–	O	General-purpose I/O port(3V pin)
	BOUT7	–		Display digital B7 output pin
200	PG0	–	O	General-purpose I/O port (3V pin)
	DCKIN	–		Display reference clock input pin (for External sync)
	CMDTRG	–		GDC command trigger input pin
197	PG1	–	O	General-purpose I/O port (3V pin)
	VSIN	P		Capture vertical sync signal input pin
198	PG2	–	O	General-purpose I/O port (3V pin)
	HSIN	P		Capture horizontal sync signal input pin
199	PG3	–	O	General-purpose I/O port (3V pin)
	CSOUT	–		Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin
23	PG4	–	O	General-purpose I/O port (3V pin)
	DCKOUT	–		Display reference clock output pin (for Internal sync)
24	PG5	–	O	General-purpose I/O port (3V pin)
	VSYNC	–		Display vertical sync signal output pin (for Internal sync)/Display vertical sync signal input pin (for External sync)
25	PG6	–	O	General-purpose I/O port (3V pin)
	HSYNC	–		Display horizontal sync signal output pin (for Internal sync)/Display horizontal sync signal input pin (for External sync)
26	PG7	–	O	General-purpose I/O port (3V pin)
	DEOUT	P		Display enable display period output pin
196	PH3	–	O	General-purpose I/O port (3V pin)
	CCLK	–		For capture, capture clock input pin
204	REFOUT	–	T	Clamp level output pin
203	AVR3	–	S	"L" side reference voltage for NTSC A/D converter pin
205	VIN	–	S	NTSC signal input pin
111	AVCC5	–	–	AD convertor analog power supply pin
201, 207	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
112	AVRH5	–	–	AD convertor upper limit reference voltage pin
113	AVSS5/ AVRL5	–	–	AD convertor GND/ AD convertor lower limit reference voltage pin
202, 206	AVSS3	–	–	NTSC AD convertor GND pin
124	C_1	–	–	Built-in regulator capacitor connected pin 1
73	C_2	–	–	Built-in regulator capacitor connected pin 2
20	C_3	–	–	Built-in regulator capacitor connected pin 3

3.2 MB91F59A/B (BGA320)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
1	VSS	–	–	GND pin
2	VSS	–	–	GND pin
3	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
4	VIN	–	S	NTSC signal input pin
5	REFOUT	–	T	Clamp level output pin
6	AVCC3	–	–	For NTSC, AD convertor analog power supply pin
7	BIN5	–	O	Capture B5 input pin (RGB mode)
	PC5			General-purpose I/O port (3V pin)
8	BIN2	–	O	Capture B2 input pin (RGB mode)
	PC2			General-purpose I/O port (3V pin)
9	GIN5	–	O	Capture G5 input pin (RGB mode)
	PB5			General-purpose I/O port (3V pin)
10	GIN2	–	O	Capture G2 input pin (RGB mode)
	VIN6			Capture VIN6 input pin (656 mode)
	PB2			General-purpose I/O port (3V pin)
11	RIN5	–	O	Capture R5 input pin (RGB mode)
	VIN3			Capture VIN3 input pin (656 mode)
	PA5			General-purpose I/O port (3V pin)
12	RIN2	–	O	Capture R2 input pin (RGB mode)
	VIN0			Capture VIN0 input pin (656 mode)
	PA2			General-purpose I/O port (3V pin)
13	VSS	–	–	GND pin
14	P136	–	A	General-purpose I/O port (Single clock product)
	(X1A)		N	Sub clock oscillation output pin (Dual clock product)
15	P137	–	A	General-purpose I/O port (Single clock product)
	(X0A)	–	N	Sub clock oscillation input pin (Dual clock product)
16	VSS	–	–	GND pin
17	P094	–	C	General-purpose I/O port
	ICU1_1			Input capture ch.1 input pin (1)
	INT15			INT15 External interrupt input pin
	SIN3			LIN-UART ch.3 serial data input pin
	PPG9_1			PPG ch.9 output pin (1)
	TIN9_1			Reload timer ch.9 event input pin (1)
	SGO1			Sound generator ch.1 SGO output pin
18	ADTG	–	A	A/D convertor external trigger input pin
	P090			General-purpose I/O port
	PPG0_2			PPG ch.0 output pin (2)
	TIN7_1			Reload timer ch.7 event input pin (1)
19	TCK	–	U	Test Clock (JTAG Boundary Scan Test)
20	VSS	–	–	GND pin
21	TMS	–	U	Test Mode State (JTAG Boundary Scan Test)
22	TDO	–	W	Test Data Out (JTAG Boundary Scan Test)
23	AN31	–	E	ADC Analog 31 input pin
	P087			General-purpose I/O port
	ICU4_2			Input capture ch.4 input pin (2)
	PPG23			PPG ch.23 output pin
23	PWM2M5	–	E	SMC ch.5 output pin

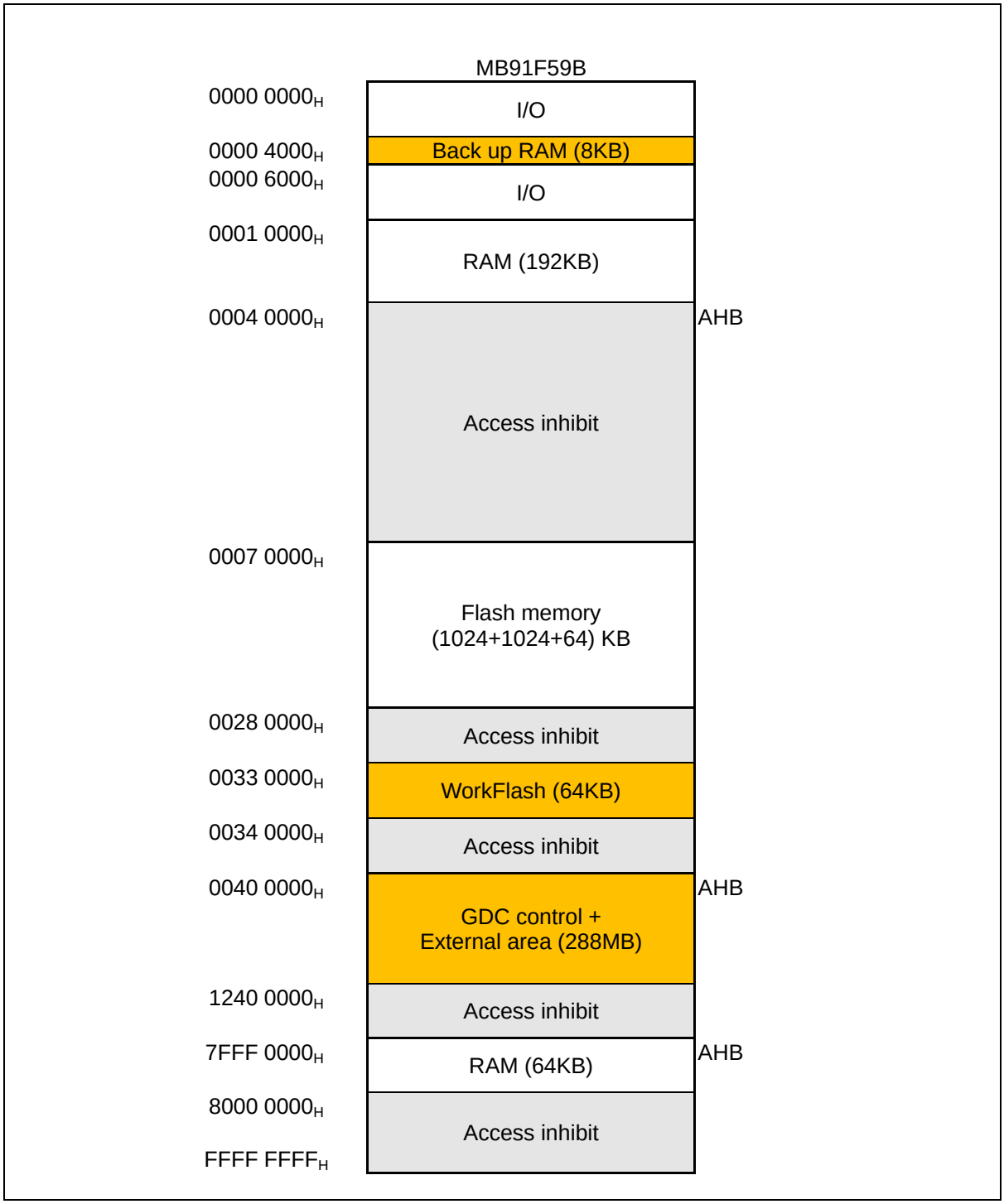
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
24	AN28	–	E	ADC Analog 28 input pin
	P084			General-purpose I/O port
	ICU1_2			Input capture ch.1 input pin (2)
	PPG20			PPG ch.20 output pin
	PWM1P5			SMC ch.5 output pin
	UDCBIN2			Up/down counter ch.2 BIN input pin
25	AN25	–	E	ADC Analog 25 input pin
	P081			General-purpose I/O port
	SOT6			LIN-UART ch.6 serial data output pin
	PPG17			PPG ch.17 output pin
	PWM1M4			SMC ch.4 output pin
	UDCBIN0_1			Up/down counter ch.0 BIN input pin (1)
26	AN22	–	E	ADC Analog 22 input pin
	P076			General-purpose I/O port
	ICU7			Input capture ch.7 input pin
	SOT7_1			LIN-UART ch.7 serial data output pin
	PPG14_1			PPG ch.14 output pin (1)
	PWM2P3			SMC ch.3 output pin
27	AN19	–	E	ADC Analog 19 input pin
	P073			General-purpose I/O port
	ICU10			Input capture ch.10 input pin
	SOT8			Multi-function serial ch.8 serial data output pin
	PWM2M2			SMC ch.2 output pin
28	AN16	–	E	ADC Analog 16 input pin
	P070			General-purpose I/O port
	SOT9			Multi-function serial ch.9 serial data output pin
	PWM1P2			SMC ch.2 output pin
29	AN13	–	E	ADC Analog 13 input pin
	P065			General-purpose I/O port
	PWM1M1			SMC ch.1 output pin
	UDCZIN0			Up/down counter ch.0 ZIN input pin
30	AN10	–	E	ADC Analog 10 input pin
	P062			General-purpose I/O port
	SCK10			Multi-function serial ch.10 clock I/O pin
	PWM2P0			SMC ch.0 output pin
	UDCZIN1			Up/down counter ch.1 ZIN input pin
31	VSS	–	–	GND pin
32	C_1	–	–	Built-in regulator capacitor connected pin 1
33	AN5	–	C	ADC Analog 5 input pin
	P105			General-purpose I/O port
	ICU9_1			Input capture ch.9 input pin (1)
	SCK5_1			LIN-UART ch.5 clock I/O pin (1)
	PPG3_1			PPG ch.3 output pin (1)
	TOT1_1			Reload timer ch.1 output pin (1)
34	AVSS5	–	–	A/D convertor GND
	AVRL5			A/D convertor lower limit reference voltage pin
35	AVRH5	–	–	A/D convertor upper limit reference voltage pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
155	SOT5	–	C	LIN-UART ch.5 serial data output pin
	PPG6_2			PPG ch.6 output pin (2)
	TOT2			Reload timer ch.2 output pin
156	FRCK1	–	C	Free-run timer 1 clock input pin
	P120			General-purpose I/O port
	INT6			INT6 External interrupt input pin
	SIN5			LIN-UART ch.5 serial data input pin
	PPG5_2			PPG ch.5 output pin (2)
	TOT1			Reload timer ch.1 output pin
157	FRCK3	–	C	Free-run timer 3 clock input pin
	P116			General-purpose I/O port
	SOT4			LIN-UART ch.4 serial data output pin
	TIN3			Reload timer ch.3 event input pin
	SGA3			Sound generator ch.3 SGA output pin
158	P097	–	C	General-purpose I/O port
	ICU4_1			Input capture ch.4 input pin (1)
158	INT8			INT8 External interrupt input pin
	SOT3			LIN-UART ch.3 serial data output pin
	PPG0_1			PPG ch.0 output pin (1)
	TIN0			Reload timer ch.0 event input pin
	WOT			RTC overflow output pin
159	TX2	–	C	CAN transmission data 2 output pin
	P112			General-purpose I/O port
	PPG3_2			PPG ch.3 output pin (2)
	TOT10_1			Reload timer ch.10 output pin (1)
160	VSS	–	–	GND pin
161	AN29	–	E	ADC Analog 29 input pin
	P085			General-purpose I/O port
	ICU2_2			Input capture ch.2 input pin (2)
	PPG21			PPG ch.21 output pin
	PWM1M5			SMC ch.5 output pin
	UDCAIN2			Up/down counter ch.2 AIN input pin
162	AN26	–	E	ADC Analog 26 input pin
	P082			General-purpose I/O port
	SCK6			LIN-UART ch.6 clock I/O pin
	PPG18			PPG ch.18 output pin
	PWM2P4			SMC ch.4 output pin
	UDCZIN0_1			Up/down counter ch.0 ZIN input pin (1)
163	AN23	–	E	ADC Analog 23 input pin
	P077			General-purpose I/O port
	ICU6			Input capture ch.6 input pin
	SCK7_1			LIN-UART ch.7 clock I/O pin
	PPG15_1			PPG ch.15 output pin (1)
	PWM2M3			SMC ch.3 output pin
164	AN20	–	E	ADC Analog 20 input pin
	P074			General-purpose I/O port
	ICU9			Input capture ch.9 input pin
164	SCK8	–	E	Multi-function serial ch.8 clock I/O pin
	PPG12_1			PPG ch.12 output pin (1)
	PWM1P3			SMC ch.3 output pin

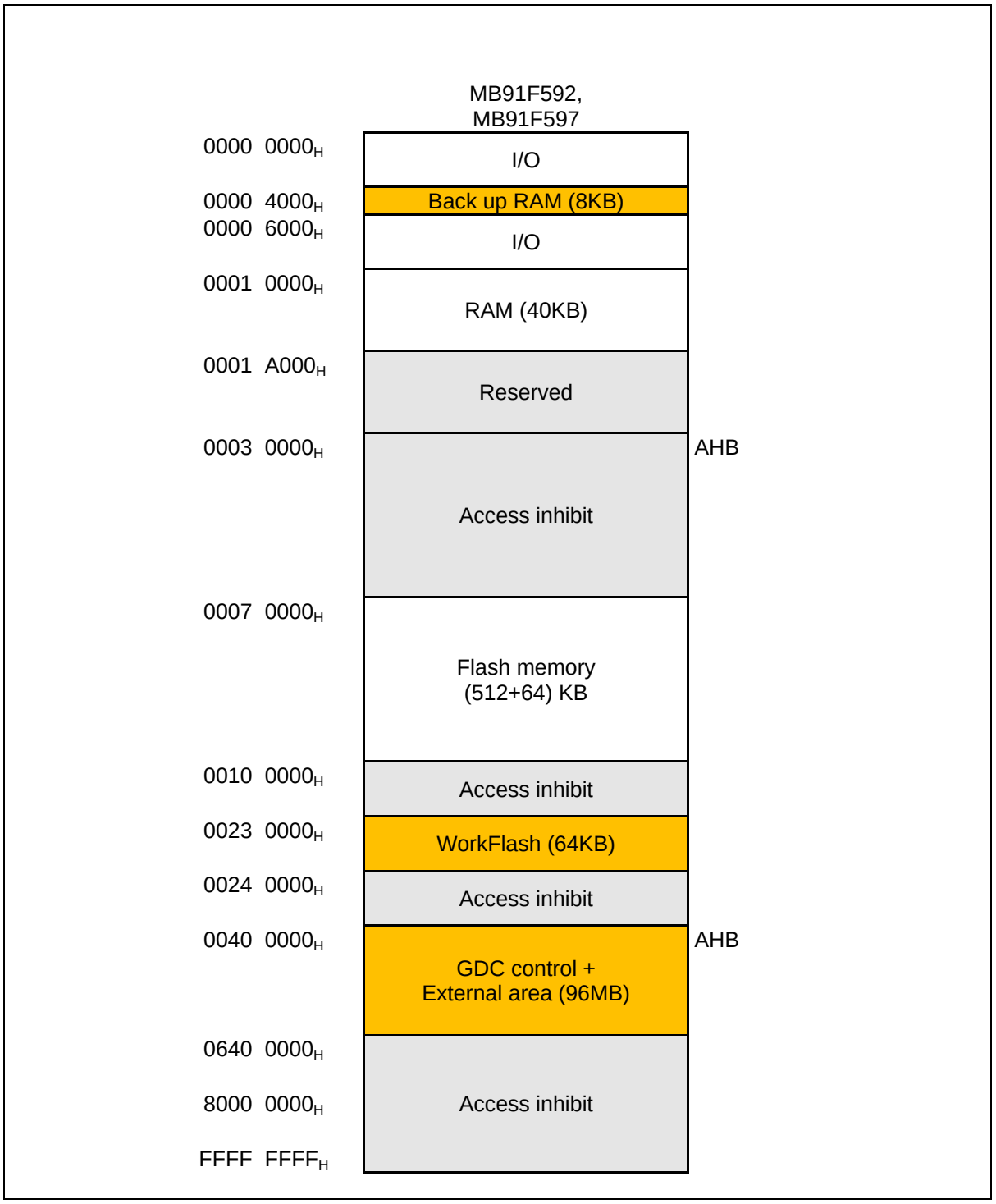
Type	Circuit	Remarks
V		• TRST (JTAG) • CMOS input • Pull-up resistor control 50kΩ (1.2V Cont)
W		• TDO (JTAG) In case of Boundary Scan Test mode. • High Impedance state In other case of Boundary Scan Test Mode. • 5mA output

8. Memory Map

■Memory map



■Memory map


MB91F592,
MB91F597
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (40KB)
0001 A000H
Reserved
0003 0000H
AHB
Access inhibit
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
AHB
GDC control +
External area (96MB)
0640 0000H
Access inhibit
8000 0000H
FFFF FFFFH

*1: Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*2: The status of the multi-function serial interface does not support a DMA transfer caused by I^2C reception.

*3: The clock calibration unit does not support a DMA transfer caused by an interrupt.

*4: RAM ECC bit error does not support a DMA transfer caused by an interrupt.

*5: REALOS is a trademark of Cypress

*6: An interrupt of Up/down counter ch.2 does not support a DMA transfer.

*7: An interrupt related GDC does not support a DMA transfer.

**: Only supported by MB91F59A/B

UDCn: Up/down counter ch.n

ICUn: Input capture unit.n

OCUn: Output compare unit.n

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	$V_{CC}5$ = 4.5V I_{OH} = -1.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH2}		$V_{CC}5$ = 4.5V I_{OH} = -2.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH3}	P060 to P067, P070 to P077, P080 to P087	DV_{CC} = 4.5V I_{OH} = -30.0mA	DV_{CC}-0.5	–	DV_{CC}	V	SMC shared pin
	V_{OH4}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	$V_{CC}3$ = 3.0V I_{OH} = -2.0mA	$V_{CC}3$-0.5	–	$V_{CC}3$	V	3.3V dedicated pin
	V_{OH5}		$V_{CC}3$ = 3.0V I_{OH} = -5.0mA					
	V_{OH6}		$V_{CC}3$ = 3.0V I_{OH} = -10.0mA					
	V_{OH7}		$V_{CC}3$ = 3.0V I_{OH} = -20.0mA					
	V_{OH8}	TDO	$V_{CC}5$ = 4.5V I_{OH} = -5.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	BGA product only

11.4.1.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

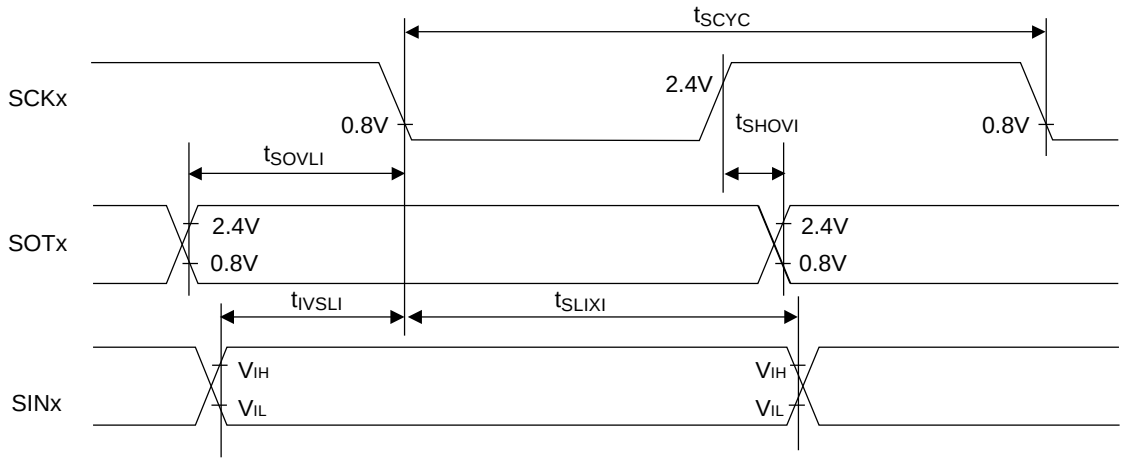
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	$V_{CC}5$	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	$V_{CC}5$	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Specification for voltage slope detection	–	$V_{CC}5$	$V_{CC}5$ = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	$V_{CC}5$	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

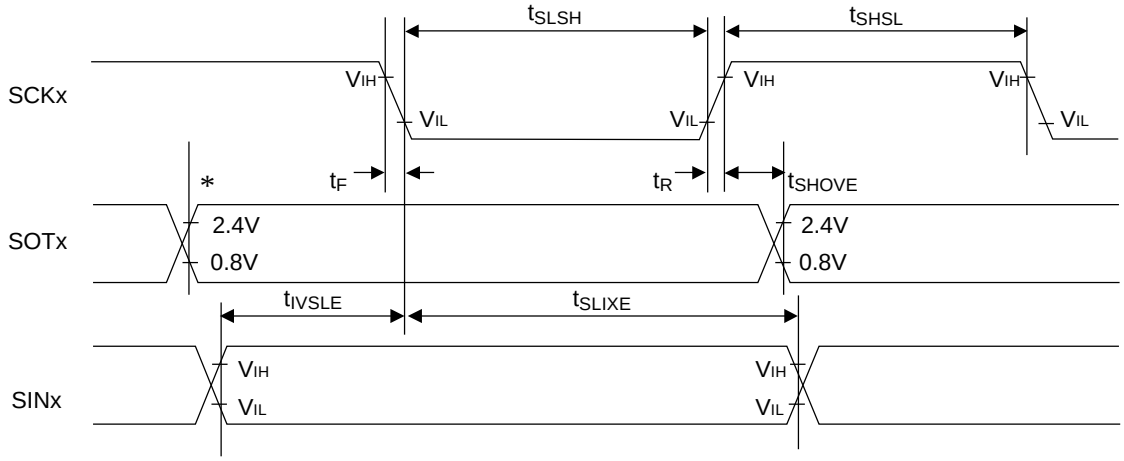
*2: When setting the power supply fluctuation to this specification or less, it is possible to suppress the voltage slope detection. This is the specification when the power supply fluctuation is stable.

*3: This time is to start the voltage slope detection at next power on after power down and internal charge loss.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



***: Changes when Writing to TDR Register**

■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		34	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H"pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

■Bit setting: ESCR: SCES=1, ECCR: SCDE=0

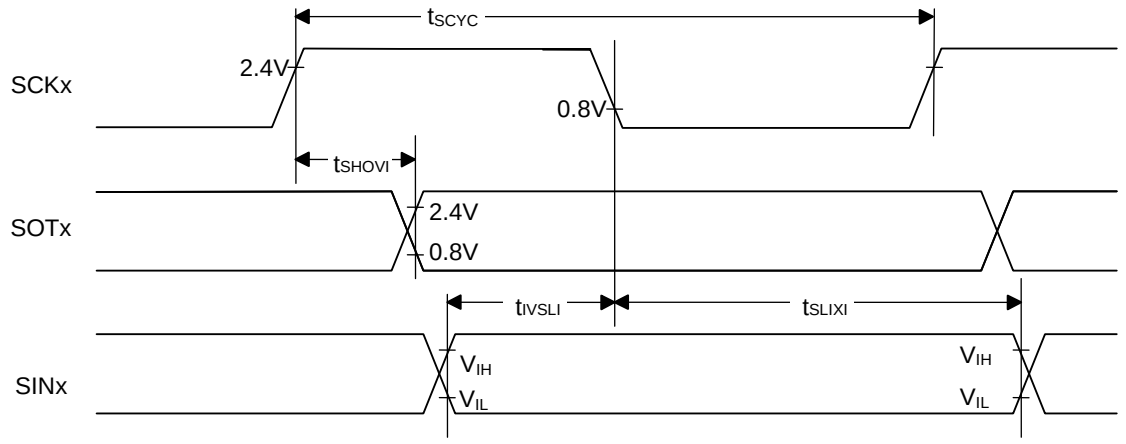
(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$5t_{CPP}$	–	ns	Internal shift clock mode: C_L=80pF+1 • TTL
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		t_{CPP}+80	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXI}			0	–	ns	
Serial clock "H" pulse width	t_{SHSL}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7	–	$3t_{CPP}$-t_R	–	ns	External shift clock mode: C_L=80pF+1 • TTL
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	–	ns	
SCK ↑ → SOT delay time	t_{SHOVE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		–	$2t_{CPP}$+60	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLE}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		30	–	ns	
SCK ↓ → Valid SIN hold time	t_{SLIXE}			t_{CPP}+30	–	ns	
SCK fall time	t_F	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		–	10	ns	
SCK rise time	t_R			–	40	ns	

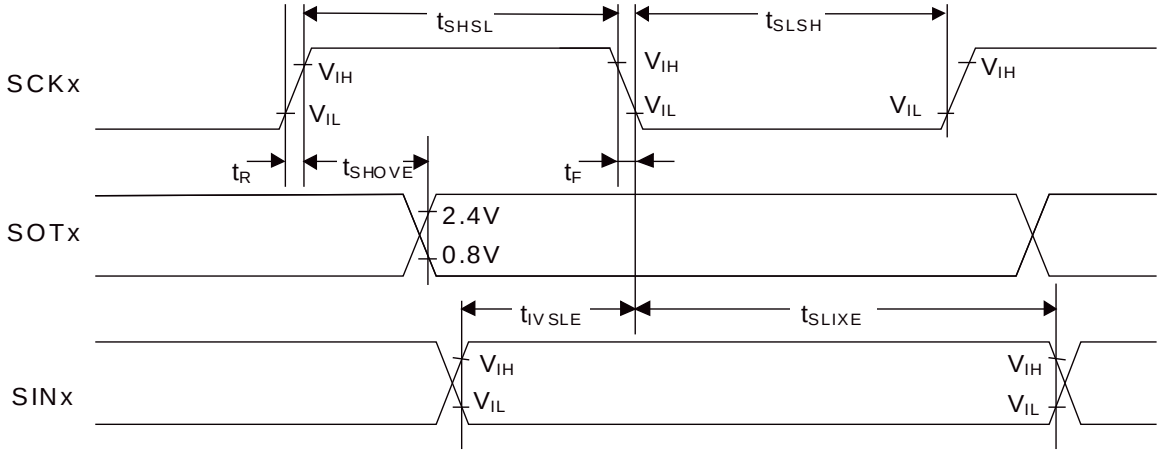
Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



AC Characteristics of Display Output Signal

■Clock Mode

There are multiple clock modes for display output clocks, as shown in Table 1. The AC timing parameters vary depending on modes. The AC timing parameters are specified for each mode.

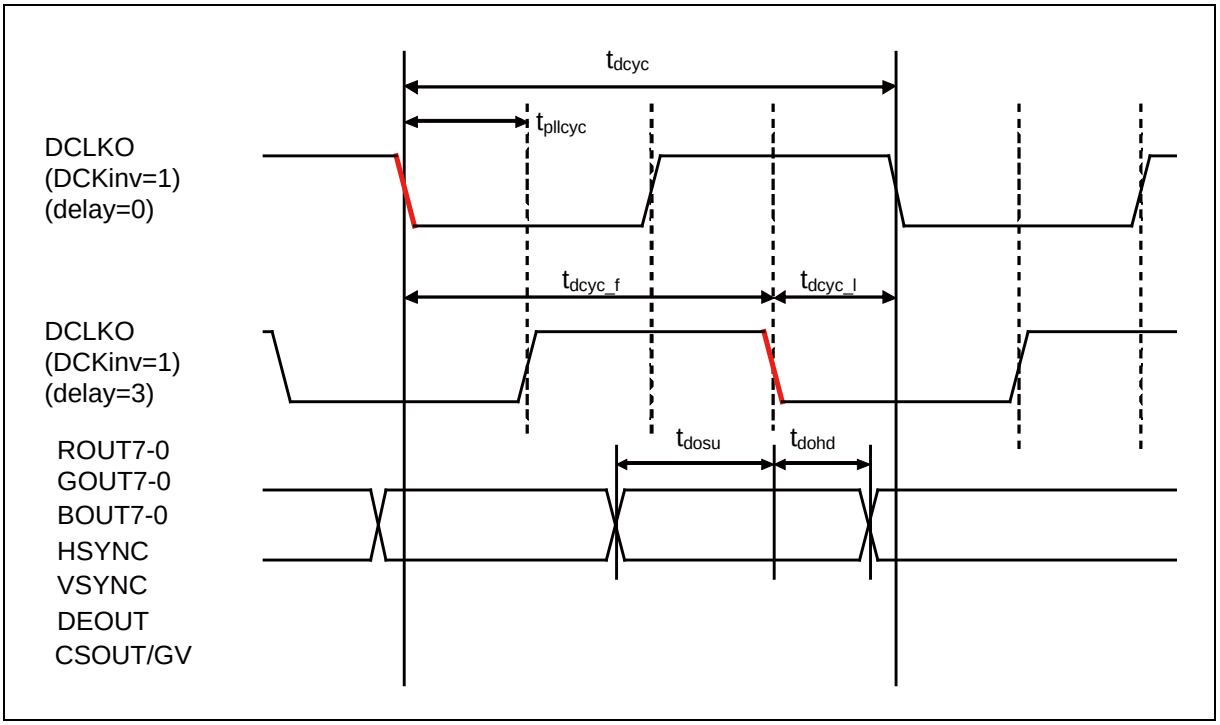
Table 1. Clock Mode for Display Output

Setting Register Bit Field				Clock Mode Name
DCM1	DCM3			
CKS	DCKed	DCKD	DCKinv	
0	0	0	0	Built-in PLL standard mode
0	0	0	1	Built-in PLL reverse edge mode
0	1	0	0	Cannot be used.
0	1	0	1	
0	0	Other than 0	0	Built-in PLL delay mode
0	0	Other than 0	1	Built-in PLL reverse edge and delay mode
0	1	Other than 0	0	Built-in PLL both edge and delay mode
0	1	Other than 0	1	
1	0	0	0	DCLKI input standard mode
1	0	0	1	DCLKI input reverse edge mode
1	1	0	0	Cannot be used.
1	1	0	1	
1	0	Other than 0	0	
1	0	Other than 0	1	
1	1	Other than 0	0	
1	1	Other than 0	1	

Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

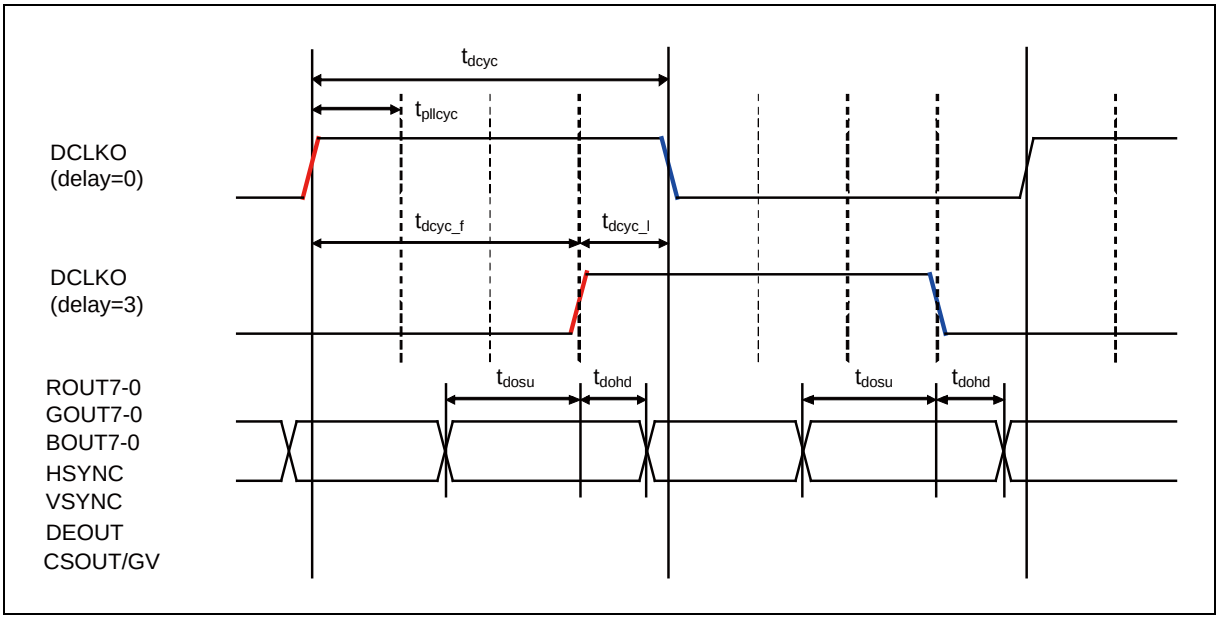
Figure 6. Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

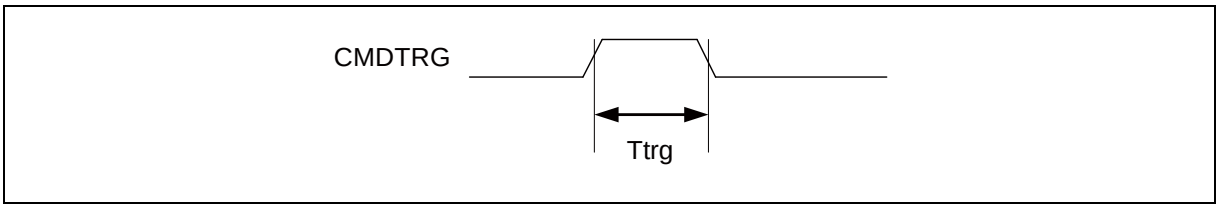
Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



11.4.1.14 GDC ommand trigger signal

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input trigger pulse width	Ttrg	CMDTRG	160	–	ns	



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