Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	576KB (576K x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	848K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f592bspmc-gsk5e1

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
134	P067	–	E	General-purpose I/O port
	PWM2M1	–		SMC ch.1 output pin
	AN15	–		ADC Analog 15 input pin
	UDCAIN0	–		Up/down counter ch.0 AIN input pin (MB91F59A/B only)
	SIN9	–		Multi-function serial ch.9 serial data input pin(MB91F59A/B only)
137	P070	–	E	General-purpose I/O port
	PWM1P2	–		SMC ch.2 output pin
	AN16	–		ADC Analog 16 input pin
	SOT9	–		Multi-function serial ch.9 serial data output pin(MB91F59A/B only)
138	P071	–	E	General-purpose I/O port
	PWM1M2	–		SMC ch.2 output pin
	AN17	–		ADC Analog 17 input pin
	SCK9	–		Multi-function serial ch.9 clock I/O pin(MB91F59A/B only)
139	P072	–	E	General-purpose I/O port
	PWM2P2	–		SMC ch.2 output pin
	AN18	–		ADC Analog 18 input pin
	SIN8	–		Multi-function serial ch.8 serial data input pin(MB91F59A/B only)
	ICU11	–		Input capture ch.11 input pin(MB91F59A/B only)
140	P073	–	E	General-purpose I/O port
	PWM2M2	–		SMC ch.2 output pin
	AN19	–		ADC Analog 19 input pin
	SOT8	–		Multi-function serial ch.8 serial data output pin(MB91F59A/B only)
	ICU10	–		Input capture ch.10 input pin(MB91F59A/B only)
141	P074	–	E	General-purpose I/O port
	PWM1P3	–		SMC ch.3 output pin
	AN20	–		ADC Analog 20 input pin
	PPG12_1	–		PPG ch.12 output pin (1)
	SCK8	–		Multi-function serial ch.8 clock I/O pin(MB91F59A/B only)
	ICU9	–		Input capture ch.9 input pin(MB91F59A/B only)
142	P075	–	E	General-purpose I/O port
	PWM1M3	–		SMC ch.3 output pin
	AN21	–		ADC Analog 21 input pin
	SIN7_1	–		LIN-UART ch.7 serial data input pin
	PPG13_1	–		PPG ch.13 output pin (1)
	ICU8	–		Input capture ch.8 input pin(MB91F59A/B only)
143	P076	–	E	General-purpose I/O port
	PWM2P3	–		SMC ch.3 output pin
	AN22	–		ADC Analog 22 input pin
	SOT7_1	–		LIN-UART ch.7 serial data output pin
	PPG14_1	–		PPG ch.14 output pin (1)
	ICU7	–		Input capture ch.7 input pin(MB91F59A/B only)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
36	P125	–	A	General-purpose I/O port
	ICU0			Input capture ch.0 input pin
	SCK11			Multi-function serial ch.11 clock I/O pin
	OCU3			Output compare ch.3 output pin
	PPG10_2			PPG ch.10 output pin (2)
	TIN10			Reload timer ch.10 event input pin
37	P123	–	A	General-purpose I/O port
	SIN11			Multi-function serial ch.11 serial data input pin
	OCU1			Output compare ch.1 output pin
	PPG8_2			PPG ch.8 output pin (2)
	TIN8			Reload timer ch.8 event input pin
38	VSS	–	–	GND pin
39	VSS	–	–	GND pin
40	MD3	–	F3	Mode pin 3
41	DEBUGIF	–	G	DEBUG I/F pin
42	TX1	–	C	CAN transmission data1 output pin
	FRCK5			Free-run timer 5 clock input pin
	P110			General-purpose I/O port
	PPG1_2			PPG ch.1 output pin (2)
	TOT8_1			Reload timer ch.8 output pin (1)
43	P091	–	C	General-purpose I/O port
	ICU2_1			Input capture ch.2 input pin (1)
	INT12			INT12 External interrupt input pin
	SIN2			LIN-UART ch.2 serial data input pin
	PPG6_1			PPG ch.6 output pin (1)
	TOT2_1			Reload timer ch.2 output pin (1)
	SGA0			Sound generator ch.0 SGA output pin
44	VSS	–	–	GND pin
45	X0	–	L	Main clock oscillation input pin
46	X1	–	L	Main clock oscillation output pin
47	VSS	–	–	GND pin
48	A23	–	O	External bus · Address bit23 output pin
	P055			General-purpose I/O port (3V pin)
	SPI_SCK			SPI clock output pin
49	A22	–	O	External bus · Address bit22 output pin
	P054			General-purpose I/O port (3V pin)
	SPI_DI			SPI data input pin
50	C_2	–	–	Built-in regulator capacitor connected pin 2

■Precautions when writing to registers including the status flag
When writing data in the register that has a status flag (especially, an interrupt request flag) to control function, taking care not to clear its status flag erroneously must be followed.

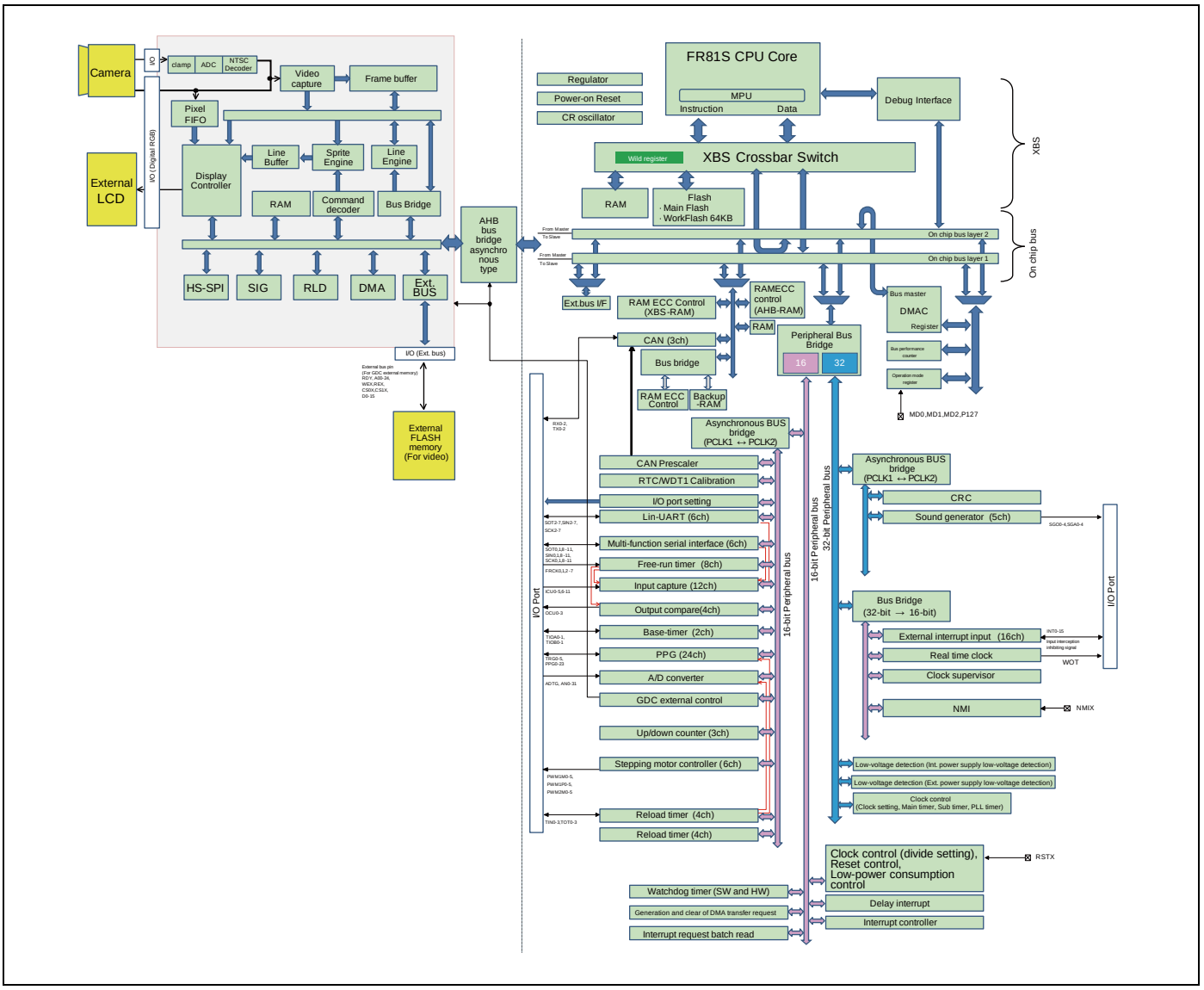
The program must be written not to clear the flag to the status bit, and then to set the control bits to have the desired value.

Especially, if multiple control bits are used, the bit instruction cannot be used. (The bit instruction can access to a single bit only.) By the Byte, Half-word, or Word access, data is written to the control bits and status flag simultaneously. During this time, take care not to clear other bits (in this case, the bits of status flag) erroneously.

Note:

These points can be ignored because the bit instructions to a register which supports RMW are already taken the points into consideration. Care must be taken when the bit instruction is used to a register which does not support RMW.

■MB91F59A/59B



Note: I/O of peripheral functions can be confirmed at "PIN ASSIGNMENT" and "PIN DESCRIPTION".

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$0001C0_H$	TMRLRA8 [R/W] H XXXXXXXX XXXXXXXX		TMR8 [R] H XXXXXXXX XXXXXXXX		Reload timer 8 MB91F59A/B only
$0001C4_H$	TMRLRB8 [R/W] H XXXXXXXX XXXXXXXX		TMCSR8 [R/W] B, H,W 00000000 0-000000		
$0001C8_H$	TMRLRA9 [R/W] H XXXXXXXX XXXXXXXX		TMR9 [R] H XXXXXXXX XXXXXXXX		Reload timer 9 MB91F59A/B only
$0001CC_H$	TMRLRB9 [R/W] H XXXXXXXX XXXXXXXX		TMCSR9 [R/W] B, H,W 00000000 0-000000		
$0001D0_H$	TMRLRA10 [R/W] H XXXXXXXX XXXXXXXX		TMR10 [R] H XXXXXXXX XXXXXXXX		Reload timer 10 MB91F59A/B only
$0001D4_H$	TMRLRB10 [R/W] H XXXXXXXX XXXXXXXX		TMCSR10 [R/W] B, H,W 00000000 0-000000		
$0001D8_H$ to $0001DC_H$	—	—	—	—	Reserved
$0001E0_H$	SCR10 [R/W] B,H,W 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R/W] B,H,W 0-000011	ESCR10 [R/W] B,H,W -0000000	Multi-function serial 10 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001E4_H$	RDR10/(TDR10)[R/W] B,H,W *1 -------0 00000000		BGR10 [R/W] H,W 00000000 00000000		
$0001E8_H$	—	—	—	—	
$0001EC_H$	FCR110 [R/W] B,H,W ---00100	FCR010 [R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
$0001F0_H$	SCR11 [R/W] B,H,W 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R/W] B,H,W 0-000011	ESCR11 [R/W] B,H,W -0000000	Multi-function serial 11 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001F4_H$	RDR11/(TDR11)[R/W] B,H,W *1 -------0 00000000		BGR11 [R/W] H,W 00000000 00000000		
$0001F8_H$	—	—	—	—	
$0001FC_H$	FCR111 [R/W] B,H,W ---00100	FCR011 [R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000490_H	IORR0[R/W] B, H, W -0000000	IORR1[R/W] B, H, W -0000000	IORR2[R/W] B, H, W -0000000	IORR3[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B, H, W -0000000	IORR5[R/W] B, H, W -0000000	IORR6[R/W] B, H, W -0000000	IORR7[R/W] B, H, W -0000000	
000498_H	IORR8[R/W] B, H, W -0000000	IORR9[R/W] B, H, W -0000000	IORR10[R/W] B, H, W -0000000	IORR11[R/W] B, H, W -0000000	
$00049C_H$	IORR12[R/W] B, H, W -0000000	IORR13[R/W] B, H, W -0000000	IORR14[R/W] B, H, W -0000000	IORR15[R/W] B, H, W -0000000	
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ----0000	—	—	—	CAN prescaler
$0004A8_H$	CPCLR6 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 6 MB91F59A/B only
$0004AC_H$	TCDT6 [R/W] W 00000000 00000000 00000000 00000000				
$0004B0_H$	TCCSH6 [R/W] B, H, W 0-----00	TCCSL6 [R/W] B, H, W -1-00000	—		
$0004B4_H$	—	—	—	—	Reserved
$0004B8_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration (Calibration)
$0004BC_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
$0004C0_H$	—	—	—	—	
$0004C4_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		
$0004C8_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$	CRTR [R/W] B,H,W 01111111	—	—	—	RC trimming setting register
$0004D0_H$	CPCLR7 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 7 MB91F59A/B only
$0004D4_H$	TCDT7 [R/W] W 00000000 00000000 00000000 00000000				
$0004D8_H$	TCCSH7 [R/W] B, H, W 0-----00	TCCSL7 [R/W] B, H, W -1-00000	—		
$0004DC_H$	—	—	—	—	Reserved
$0004E0_H$	SCR8 [R/W] B,H,W 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R/W] B,H,W 0-000011	ESCR8 [R/W] B,H,W -0000000	Multi-function serial 8 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0004E4_H$	RDR8/(TDR8)[R/W] B,H,W *1 -------0 00000000		BGR8 [R/W] H,W 00000000 00000000		
$0004E8_H$	—	—	—	—	
$0004EC_H$	FCR18 [R/W] B,H,W ---00100	FCR08 [R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
0004F0$_H$	SCR9 [R/W] B,H,W 0--00000	SMR9 [R/W] B,H,W 000-0000	SSR9 [R/W] B,H,W 0-000011	ESCR9 [R/W] B,H,W -0000000	Multi-function serial 9 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
0004F4$_H$	RDR9/(TDR9)[R/W] B,H,W *1 -------0 00000000		BGR9 [R/W] H,W 00000000 00000000		
0004F8$_H$	—	—	—	—	
0004FC$_H$	FCR19 [R/W] B,H,W ---00100	FCR09 [R/W] B,H,W -0000000	FBYTE29 [R/W] B,H,W 00000000	FBYTE19 [R/W] B,H,W 00000000	
000500$_H$ to 00050C$_H$	—	—	—	—	Reserved
000510$_H$	CSELR [R/W] B,H,W 001---00	CMONR [R] B,H,W 001---00	MTMCR [R/W] B,H,W 00001111	STMCR [R/W] B,H,W 0000-111	Clock control [S]
000514$_H$	PLLCR [R/W] B,H,W -------- 11110000		CSTBR [R/W] B,H,W -0000000	PTMCR [R/W] B,H,W 00------	
000518$_H$	—	—	CPUAR [R/W] B,H,W 0----XXX	—	Reset [S]
00051C$_H$	—	—	—	—	Reserved [S]
000520$_H$	CCPSSELR [R/W] B,H,W -------0	—	—	CCPSDIVR [R/W] B,H,W -000-000	Clock control 2
000524$_H$	—	CCPLLFBR [R/W] B,H,W -0000000	CCSSFBR0 [R/W] B,H,W --000000	CCSSFBR1 [R/W] B,H,W ---00000	
000528$_H$	—	CCSSCCR0 [R/W] B,H,W ----0000	CCSSCCR1 [R/W] H,W 000----- --------		Clock control 2
00052C$_H$	—	CCCGRCR0 [R/W] B,H,W 00----00	CCCGRCR1 [R/W] B,H,W 00000000	CCCGRCR2 [R/W] B,H,W 00000000	
000530$_H$	CCRTSELR [R/W] B,H,W 0------0	—	CCPMUCR0 [R/W] B,H,W 0-----00	CCPMUCR1 [R/W] B,H,W 0--00000	
000534$_H$	—	—	—	—	
000538$_H$	—	—	—	—	
00053C$_H$	—	—	—	—	
000540$_H$ to 00054C$_H$	—	—	—	—	Reserved
000550$_H$	EIRR0 [R/W] B,H,W XXXXXXXX	ENIR0 [R/W] B,H,W 00000000	ELVR0 [R/W] B,H,W 00000000 00000000		External interrupt (INT0 to INT7)
000554$_H$	EIRR1 [R/W] B,H,W XXXXXXXX	ENIR1 [R/W] B,H,W 00000000	ELVR1 [R/W] B,H,W 00000000 00000000		External interrupt (INT8 to INT15)
000558$_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000C50_H$	DCCR5[R/W] W 0----000 --00--00 00000000 0-000000				DMA controller [S]
$000C54_H$	DCSR5[R/W] H 0------- -----000		DTCR5[R/W] H 00000000 00000000		
$000C58_H$	DSAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C5C_H$	DDAR5[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C60_H$	DCCR6[R/W] W 0----000 --00--00 00000000 0-000000				
$000C64_H$	DCSR6[R/W] H 0------- -----000		DTCR6[R/W] H 00000000 00000000		
$000C68_H$	DSAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C6C_H$	DDAR6[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C70_H$	DCCR7[R/W] W 0----000 --00--00 00000000 0-000000				
$000C74_H$	DCSR7[R/W] H 0------- -----000		DTCR7[R/W] H 00000000 00000000		
$000C78_H$	DSAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C7C_H$	DDAR7[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C80_H$	DCCR8[R/W] W 0----000 --00--00 00000000 0-000000				
$000C84_H$	DCSR8[R/W] H 0------- -----000		DTCR8[R/W] H 00000000 00000000		
$000C88_H$	DSAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C8C_H$	DDAR8[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C90_H$	DCCR9[R/W] W 0----000 --00--00 00000000 0-000000				
$000C94_H$	DCSR9[R/W] H 0------- -----000		DTCR9[R/W] H 00000000 00000000		
$000C98_H$	DSAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000C9C_H$	DDAR9[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$000CA0_H$	DCCR10[R/W] W 0----000 --00--00 00000000 0-000000				
$000CA4_H$	DCSR10[R/W] H 0------- -----000		DTCR10[R/W] H 00000000 00000000		
$000CA8_H$	DSAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002050_H	IF2DTA10 [R/W] B,H,W 00000000 00000000		IF2DTA20 [R/W] B,H,W 00000000 00000000		CAN0 (64msg)
002054_H	IF2DTB10 [R/W] B,H,W 00000000 00000000		IF2DTB20 [R/W] B,H,W 00000000 00000000		
002058_H, $00205C_H$	Reserved				
002060_H, 002064_H	Reserved (IF2 data mirror)				
002068_H to $00207C_H$	Reserved				
002080_H	TREQR20 [R] B,H,W 00000000 00000000		TREQR10 [R] B,H,W 00000000 00000000		
002084_H	TREQR40 [R] B,H,W 00000000 00000000		TREQR30 [R] B,H,W 00000000 00000000		
002088_H	—		—		
$00208C_H$	—		—		
002090_H	NEWDT20 [R] B,H,W 00000000 00000000		NEWDT10 [R] B,H,W 00000000 00000000		
002094_H	NEWDT40 [R] B,H,W 00000000 00000000		NEWDT30 [R]B,H,W 00000000 00000000		
002098_H	—		—		
$00209C_H$	—		—		
$0020A0_H$	INTPND20 [R] B,H,W 00000000 00000000		INTPND10 [R] B,H,W 00000000 00000000		
$0020A4_H$	INTPND40 [R] B,H,W 00000000 00000000		INTPND30 [R] B,H,W 00000000 00000000		
$0020A8_H$	—		—		
$0020AC_H$	—		—		
$0020B0_H$	MSGVAL20 [R] B,H,W 00000000 00000000		MSGVAL10 [R] B,H,W 00000000 00000000		
$0020B4_H$	MSGVAL40 [R] B,H,W 00000000 00000000		MSGVAL30 [R] B,H,W 00000000 00000000		
$0020B8_H$	—		—		
$0020BC_H$	—		—		
$0020C0_H$ to $0020FC_H$	Reserved				

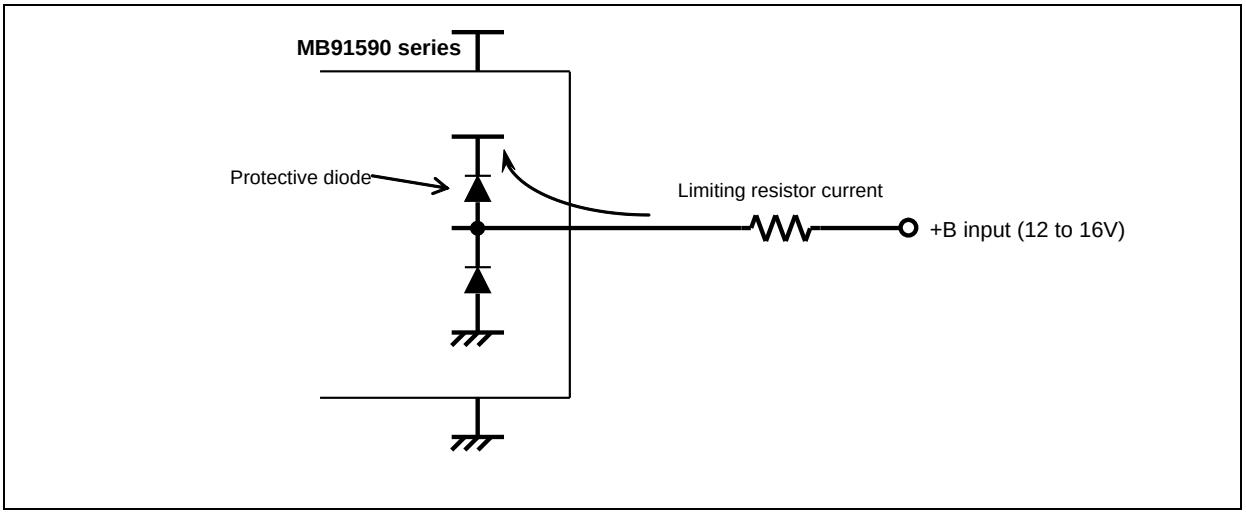
*7: Output of P60-P87 pins.

*8: Output of 3V pin.

*9: Corresponding pins: all general-purpose ports except P90/ADTG.(Except for the dedicated analog port)

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The + B signal should always be applied by connecting a limiting resistor between the + B signal and the microcontroller.
- The value of the limiting resistor should be set so that the current input to the microcontroller pin does not exceed rated values at any time regardless of instantaneously or constantly when the + B signal is input.
- Note that when the microcontroller drive current is low, such as in the low power consumption modes, the + B input potential can increase the potential at the VCC pin via a protective diode, possibly affecting other devices.
- Note that if the + B signal is input when the microcontroller is off (not fixed at 0 V), since the power is supplied through the pin, the microcontroller may operate incompletely.
- Note that if the +B signal is input at power-on, since the power is supplied through the pin, the power-on reset may not function in the power supply voltage.
- Do not leave + B input pins open.

Sample recommended Circuit



*10: To use this product at T_A=105°C, equip this on a multilayer board with four or more layers.

WARNING

Semiconductor devices may be permanently damaged by application of stress (including, without limitation, voltage, current or temperature) in excess of absolute maximum ratings. Do not exceed any of these ratings.

11.4 AC Characteristics

11.4.1 Main Clock Timing

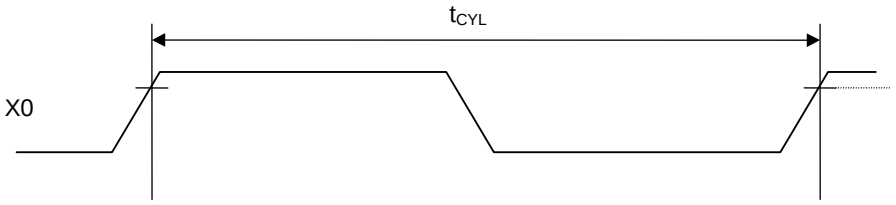
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_C	X0, X1	–	–	4	–	MHz	
Source oscillation clock cycle time	t_{CYL}	X0, X1		–	250	–	ns	
Internal operating clock frequency*1, *2	F_{CP}	–	–	2	–	128	MHz	CPU clock
	F_{CPP}	–	–	2	–	40	MHz	Peripheral bus clock
Internal operating clock cycle time*1, *2	t_{CP}	–	–	7.8125	–	500	ns	CPU clock
	t_{CPP}	–	–	25	–	500	ns	Peripheral bus clock
CAN PLL jitter (when lock)	t_{PJ}	–	–	-10	–	+10	ns	
Built-in CR oscillation frequency	F_{CCR}	–	–	50	100	200	kHz	

*1: The maximum frequency of CPU clock is described in the table of Product Type.

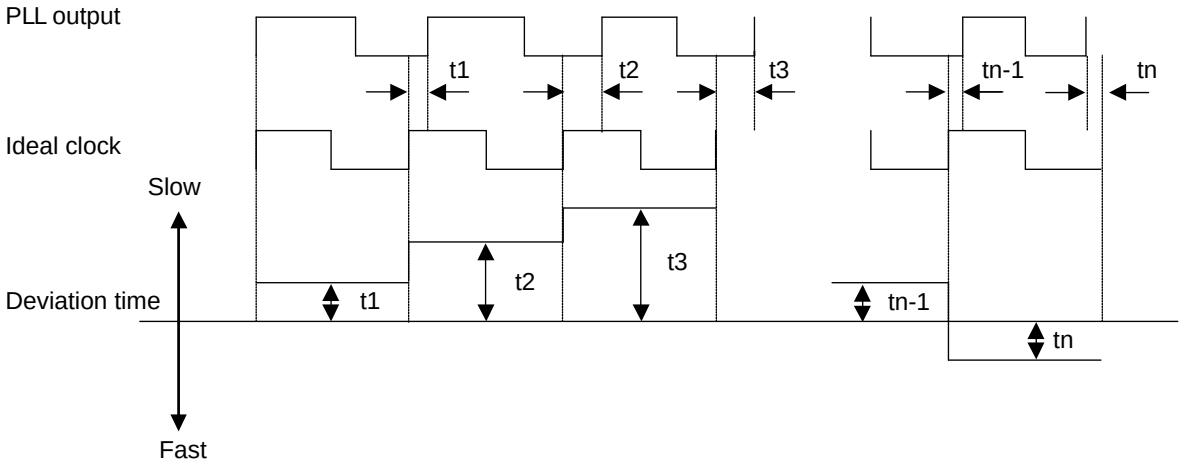
*2: The maximum / minimum value is defined when using the main clock and PLL clock.

• X0,X1 Clock Timing



• CAN PLL jitter

Deviation time from the ideal clock is assured per cycle out of 20, 000 cycles.



■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		34	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H"pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

Notes:

- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

I²C Timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		High-Speed Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0, SCK1	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK0, SCK1, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0, SCK1, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		0	3.45*2	0	0.9	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		250*3	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	2t_{CPP}*4	–	2t_{CPP}*4	–	ns	

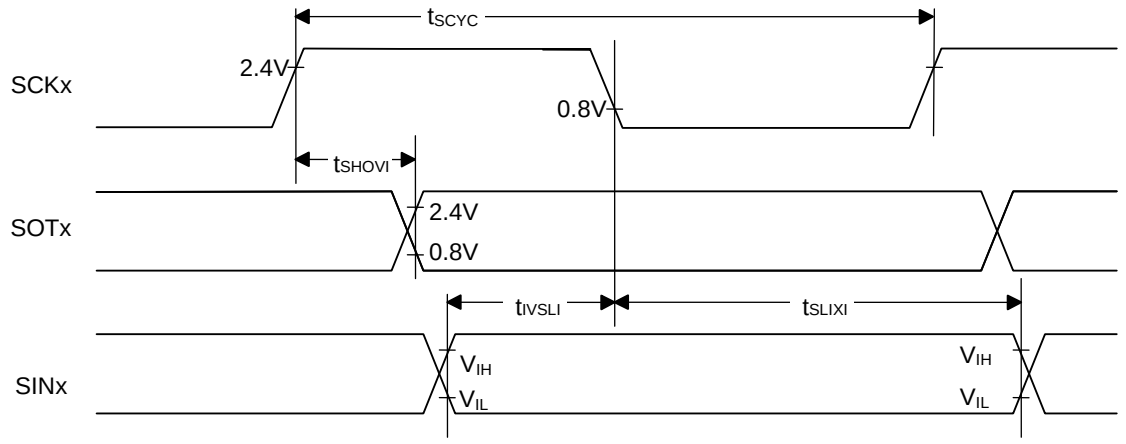
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

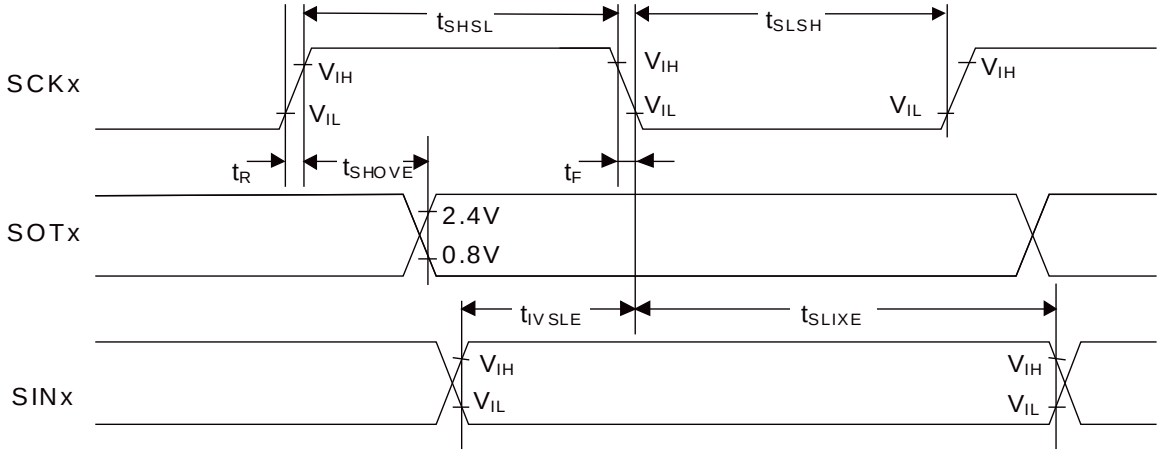
*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the peripheral clock frequency to 8MHz or more when use I²C.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



11.4.1.10 Low voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC	–	–	–	1.3	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		–	–	–	50	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	

*: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.4.1.12 External memory interface

Memory Controller

(T_A: Recommended operating conditions, $V_{CC}3$=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Chip Select delay time	t_{cso}	MEM_XCS0, MEM_XCS1	12pF/10mA	–	18	ns	*1
				–	14	ns	*2
Address delay time	t_{ao}	MEM_EA[24:0]		–	18	ns	*1
				–	14	ns	*2
Data output delay time	t_{do}	MEM_ED[15:0]		–	18	ns	*1
				–	17	ns	*2
Data output → HiZ time	t_{doz}			–	18	ns	*1
				–	17	ns	*2
NOR Flash data setup time	t_{dsr}			20	–	ns	*1
				11	–	ns	*2
NOR Flash data hold time	t_{dhr}			0	–	ns	*1
				0	–	ns	*2
NOR Flash page Read data setup time	t_{dsp}			20	–	ns	*1
				8.5	–	ns	*2
NOR Flash page Read data hold time	t_{dhp}			0	–	ns	*1
				0	–	ns	*2
XRD delay time	t_{rdo}	MEM_XRD		–	18	ns	*1
				–	14	ns	*2
XWR delay time	t_{wro}	MEM_XWR		–	18	ns	*1
				–	14	ns	*2

Output delay is reference clock is an internal clock. The reference clock of MEM_RDY is an internal clock.

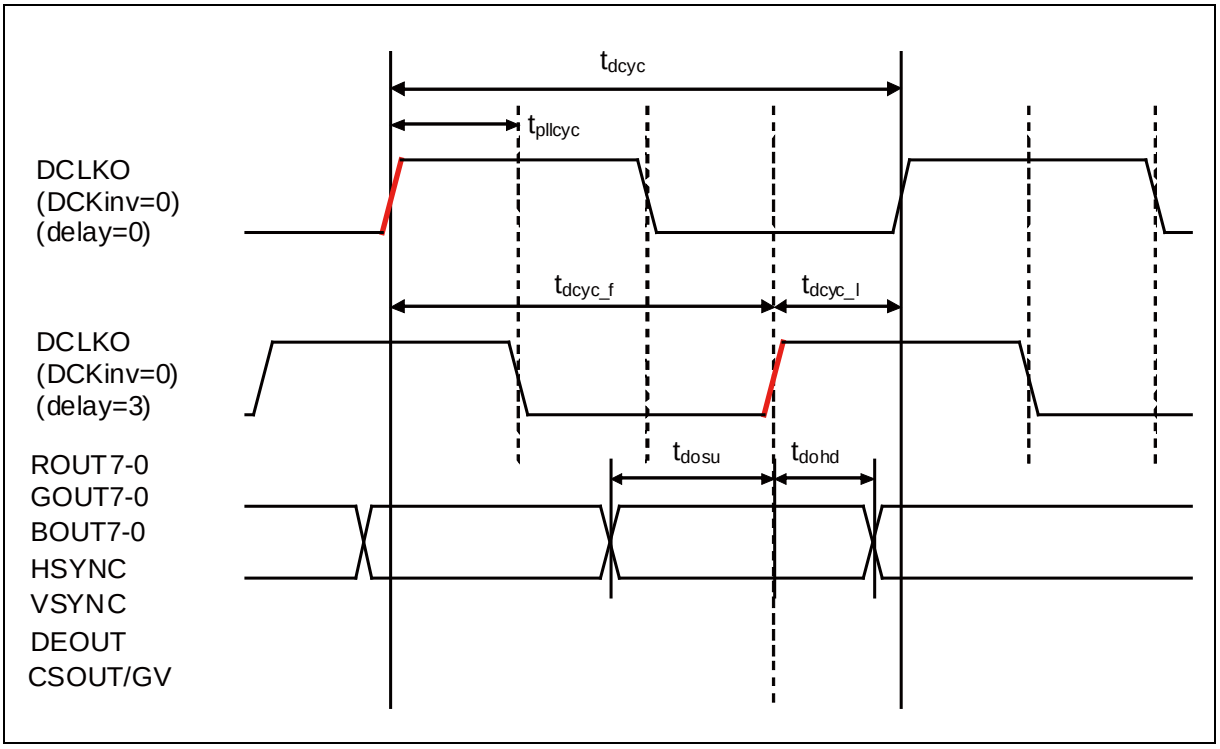
*1: MB91F591/2/4/6/7/9

*2: MB91F59A/B

Built-in PLL delay mode (DCM3.DCKinv=0)

Figure 5 shows the setup/hold definition when the external display device receives the signal at the rising edge of DCLKO. (Example: When frequency division ratio = 4)

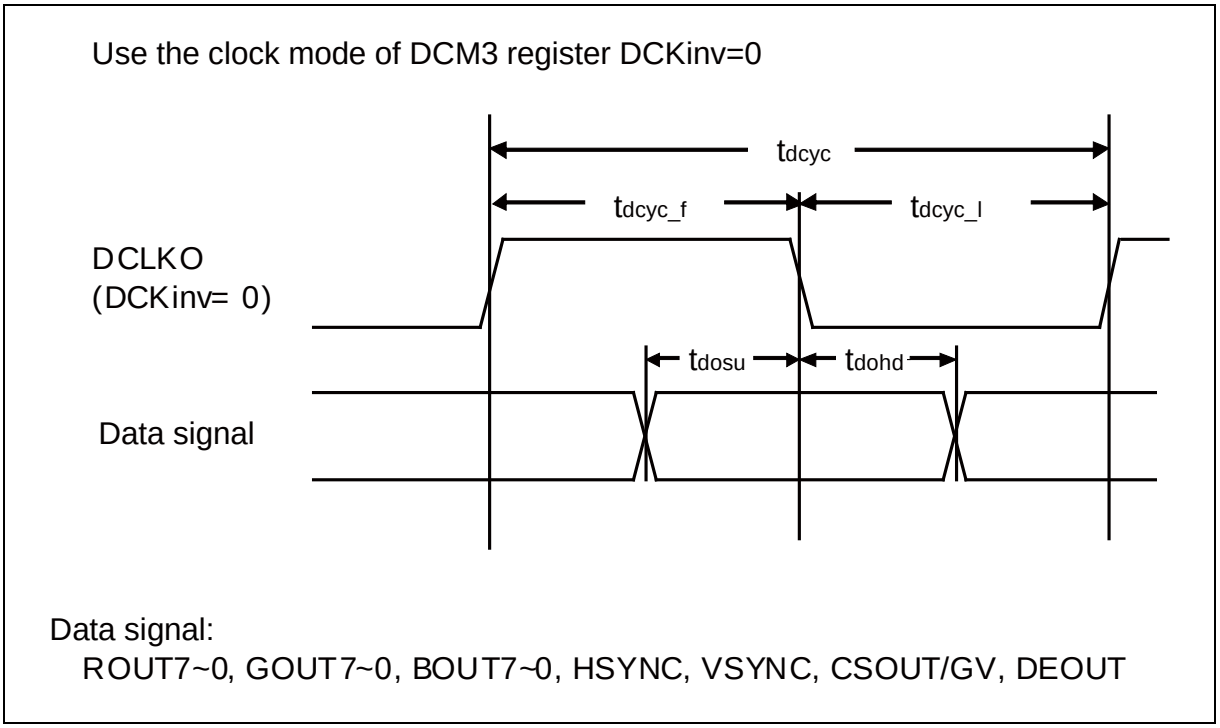
Figure 5. Built-in PLL Delay Mode Setup/Hold Definition



DCLKI Input Standard Mode (DCM3.DCKinv=0)

Figure 8 shows the setup/hold definition when the external display device (TFT) receives the signal at the falling edge of DCLKO.

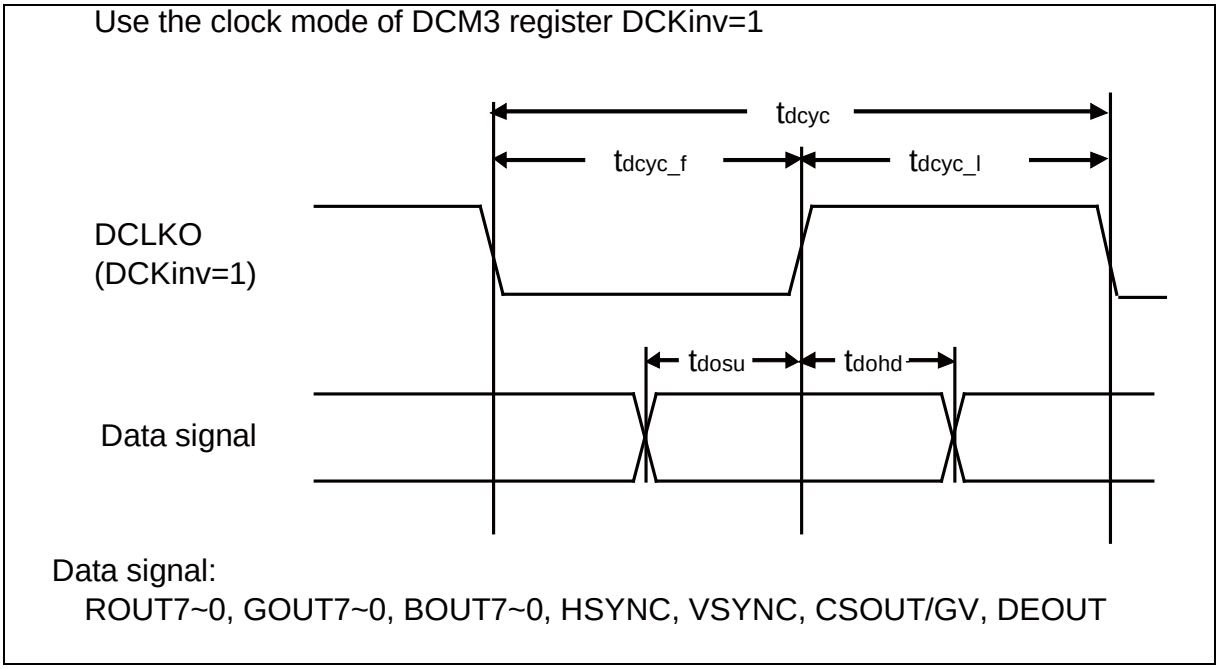
Figure 8. DCLKI Input Standard Mode Setup/Hold Definition



DCLKI Input Reverse Edge Mode (DCM3.DCKinv=1)

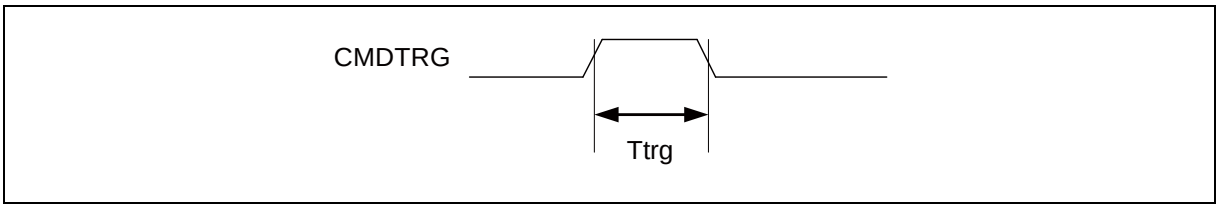
Figure 9 shows the setup/hold definition when the external display device (TFT) receives the signal at the rising edge of DCLKO.

Figure 9. DCLKI Input Reverse Edge Mode Setup/Hold Definition



11.4.1.14 GDC ommand trigger signal

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
Input trigger pulse width	Ttrg	CMDTRG	160	–	ns	



11.5 A/D Converter

11.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, $V_{CC}5$=$AV_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	±3	LSB	
Non linearity error	–	–	–	–	±2.5	LSB	
Differential linearity error	–	–	–	–	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS} - 1.5LSB	–	AV_{SS} + 2.5LSB	V	1LSB = (AV_{CC} - AV_{SS}) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH5 - 3.5LSB	–	AVRH5 + 0.5LSB	V	
Sampling time	t_{SMP}	–	1.2	–	–	µs	*1
Compare time	t_{CMP}	–	1.8	–	–	µs	*1
A/D conversion time	t_{CNV}	–	3.0	–	–	µs	*1
Analog port input current	I_{AIN}	AN0 to AN31	-5	–	+5	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	AV_{SS}	–	AVRH5	V	
Reference voltage	A_{VRH}	AVRH5	4.5	–	5.5	V	AVRH5 ≤ $AV_{CC}5$
	A_{VRL}	AVSS	–	0.0	–	V	
Power supply current	I_A	AVCC	–	–	4.0	mA	
	I_{AH}		–	–	6.0	µA	*2
	I_R	AVRH5	–	600	900	µA	
	I_{RH}		–	–	5	µA	*2
Variation between channels	–	AN0 to AN31	–	–	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

Note:
Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.