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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	872K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f594bhpmc-gsk5e1

2.5 Pin Assignment (BGA Product)

(TOP VIEW)

▲	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	A
B	76	77	78	79	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	21	B
C	75	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	95	22	C
D	74	143	204	205	206	207	208	209	210	211	212	213	214	215	216	217	218	161	96	23	D
E	73	142	203	256													219	162	97	24	E
F	72	141	202	255													220	163	98	25	F
G	71	140	201	254			257	258	259	260	261	262	263	264			221	164	99	26	G
H	70	139	200	253			284	285	286	287	288	289	290	265			222	165	100	27	H
J	69	138	199	252			283	304	305	306	307	308	291	266			223	166	101	28	J
K	68	137	198	251			282	303	316	317	318	309	292	267			224	167	102	29	K
L	67	136	197	250			281	302	315	320	319	310	293	268			225	168	103	30	L
M	66	135	196	249			280	301	314	313	312	311	294	269			226	169	104	31	M
N	65	134	195	248			279	300	299	298	297	296	295	270			227	170	105	32	N
P	64	133	194	247			278	277	276	275	274	273	272	271			228	171	106	33	P
R	63	132	193	246													229	172	107	34	R
T	62	131	192	245													230	173	108	35	T
U	61	130	191	244	243	242	241	240	239	238	237	236	235	234	233	232	231	174	109	36	U
V	60	129	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176	175	110	37	V
W	59	128	127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112	111	38	W
Y	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

3. Pin Description

3.1 Pin Description of LQFP-208/TEQFP-208

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
84	X0	–	L	Main clock oscillation input pin
83	X1	–	L	Main clock oscillation output pin
171 (dual clock product)	X0A	–	N	Sub clock oscillation input pin
172 (dual clock product)	X1A	–	N	Sub clock oscillation output pin
171 (single clock product)	P137	–	A	General-purpose I/O port
172 (single clock product)	P136	–	A	General-purpose I/O port
97	NMIX	N	F1	Non-masking interrupt input pin
87	RSTX	N	F1	External reset input pin
86	MD0	–	P	Mode pin 0
85	MD1	–	P	Mode pin 1
169	MD2	–	F2	Mode pin 2
27	P000	–	O	General-purpose I/O port (3V pin)
	D0	–		External bus · Data bit0 I/O pin
	SIN2_1	–		LIN-UART ch.2 serial data input pin (1)
	TIN0_2	–		Reload timer ch.0 event input pin (2)
	PPG0	–		PPG ch.0 output pin
28	P001	–	O	General-purpose I/O port (3V pin)
	D1	–		External bus · Data bit1 I/O pin
	SOT2_1	–		LIN-UART ch.2 serial data output pin (1)
	TIN1_2	–		Reload timer ch.1 event input pin (2)
	PPG1	–		PPG ch.1 output pin
29	P002	–	O	General-purpose I/O port (3V pin)
	D2	–		External bus · Data bit2 I/O pin
	SCK2_1	–		LIN-UART ch.2 clock I/O pin (1)
	TIN2_2	–		Reload timer ch.2 event input pin (2)
	PPG2	–		PPG ch.2 output pin
30	P003	–	O	General-purpose I/O port (3V pin)
	D3	–		External bus · Data bit3 I/O pin
	SIN3_1	–		LIN-UART ch.3 serial data input pin (1)
	TIN3_2	–		Reload timer ch.3 event input pin (2)
	PPG3	–		PPG ch.3 output pin
31	P004	–	O	General-purpose I/O port (3V pin)
	D4	–		External bus · Data bit4 I/O pin
	SOT3_1	–		LIN-UART ch.3 serial data output pin (1)
	TOT0_2	–		Reload timer ch.0 output pin (2)
	PPG4	–		PPG ch.4 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
121	P107	–	C	General-purpose I/O port
	SGO4_1	–		Sound generator ch.4 SGO output pin
	AN7	–		ADC Analog 7 input pin
	PPG5_1	–		PPG ch.5 output pin (1)
	TOT7_1	–		Reload timer ch.7 output pin (1) (MB91F59A/B only)
	ICU11_1	–		Input capture ch.11 input pin (1) (MB91F59A/B only)
101	P110	–	C	General-purpose I/O port
	TX1	–		CAN transmission data1 output pin
	PPG1_2	–		PPG ch.1 output pin (2)
	FRCK5	–		Free-run timer 5 clock input pin(MB91F59A/B only)
	TOT8_1	–		Reload timer ch.8 output pin (1) (MB91F59A/B only)
102	P111	–	C	General-purpose I/O port
	RX1	–		CAN reception data 1 input pin
	INT10	–		INT10 External interrupt input pin
	PPG2_2	–		PPG ch.2 output pin (2)
	FRCK6	–		Free-run timer 6 clock input pin(MB91F59A/B only)
	TOT9_1	–		Reload timer ch.9 output pin (1) (MB91F59A/B only)
158	P112	–	C	General-purpose I/O port
	TX2	–		CAN transmission data 2 output pin
	PPG3_2	–		PPG ch.3 output pin (2)
	TOT10_1	–		Reload timer ch.10 output pin (1) (MB91F59A/B only)
159	P113	–	C	General-purpose I/O port
	RX2	–		CAN reception data 2 input pin
	INT11	–		INT11 External interrupt input pin
	PPG4_2	–		PPG ch.4 output pin (2)
	TIN7	–		Reload timer ch.7 event input pin(MB91F59A/B only)
162	P114	–	C	General-purpose I/O port
	SGA2	–		Sound generator ch.2 SGA output pin
	SCK3	–		LIN-UART ch.3 clock I/O pin
	TRG3	–		PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1	–		Reload timer ch.1 event input pin
	ICU5_1	–		Input capture ch.5 input pin (1)
	FRCK7	–		Free-run timer 7 clock input pin(MB91F59A/B only)
163	P115	–	C	General-purpose I/O port
	SGO2	–		Sound generator ch.2 SGO output pin
	SIN4	–		LIN-UART ch.4 serial data input pin
	TIN2	–		Reload timer ch.2 event input pin
	FRCK4	–		Free-run timer 4 clock input pin(MB91F59A/B only)
164	P116	–	C	General-purpose I/O port
	SGA3	–		Sound generator ch.3 SGA output pin
	SOT4	–		LIN-UART ch.4 serial data output pin
	TIN3	–		Reload timer ch.3 event input pin
	FRCK3	–		Free-run timer 3 clock input pin(MB91F59A/B only)
165	P117	–	C	General-purpose I/O port
	SGO3	–		Sound generator ch.3 SGO output pin
	SCK4	–		LIN-UART ch.4 clock I/O pin
	TRG4	–		PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0	–		Reload timer ch.0 output pin
	FRCK2	–		Free-run timer 2 clock input pin(MB91F59A/B only)

5. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

5.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

6. Handling Devices

This section explains the latch-up prevention and treatment of a pin.

■For latch-up prevention
If a voltage higher than VCC or a voltage lower than VSS is applied to an I/O pin, or if a voltage exceeding the ratings is applied between VCC pin and VSS pin, a latch-up may occur in CMOS IC. If the latch-up occurs, the power supply current increases excessively and device elements may be damaged by heat. Take care to prevent any voltage from exceeding the maximum ratings in device application.

Also, the analog power supply (AVCC5, AVRH5), the NTSC power supply (AVCC3, AVR3), analog input and power supply to high-current output buffer pins must not be exceed the digital power supply (VCC5 or VCC3) when the power supply to the analog system and high-current output buffer pins is turned on or off.

In the correct power-on sequence of the microcontroller, turn on the digital power supply (VCC5), analog power supplies (AVCC5, AVRH5), and the power supply of high-current output buffer pins (DVCC) simultaneously. Or, turn on the digital power supply (VCC5), and then turn on analog power supplies (AVCC5, AVRH5) and the power supply of high-current output buffer pins (DVCC).

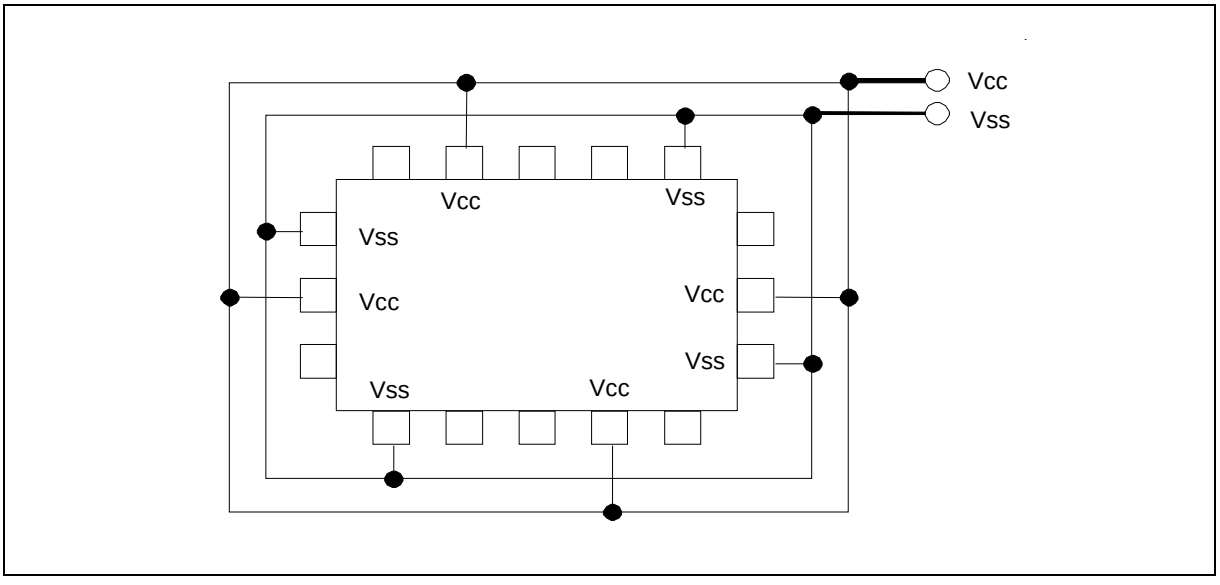
In the correct power-on sequence of GDC, similarly turn on the digital power supply (VCC3) and the NTSC analog power supply (AVCC3) simultaneously. Or, turn on the digital power supply (VCC3), and then turn on the NTSC analog power supply (AVCC3).

■Treatment of unused pins
If unused input pins are left open, they may cause a permanent damage to the device due to malfunction or latch-up. Connect a 2kΩ resistor to each of unused pins for pull-up or pull-down processing.

Also, if I/O pins are not used, they must be set to the output state for opening or they must be set to the input state and treated in the same way as for the input pins.

■Power supply pins
The device is designed to ensure that if the device contains multiple VCC pin or VSS pin, the pins that should be at the same potential are interconnected to prevent latch-up or other malfunctions. Further, connect these pins to an external power supply or ground to reduce unwanted radiation, prevent strobe signals from malfunctioning due to a raised ground level, and fulfill the total output current standard, etc. As shown in Figure 1, all Vss power supply pins must be treated in the similar way. If multiple Vcc or Vss systems are connected, the device cannot operate correctly even within the guaranteed operating range.

Figure 1. Power Supply Input Pins



The power supply pins should be connected to VCC pin and VSS pin of this device at the low impedance from the power supply source.

In the area close to this device, a ceramic capacitor having the capacitance larger than the capacitor of C pin is recommended to use as a bypass capacitor between the VCC pin and the VSS pin.

As for BGA package product, the solder balls of VSS and VCC are placed in the most internal circumference of solder-ball-placement. In order to connect bypass capacitor close to these balls, the capacitors had better be implemented on the back side of a system board surface on which BGA package is implemented.

■Crystal oscillation circuit
An external noise to the X0 pin or X1 pin may cause a device malfunction. The printed circuit board must be designed to lay out the X0 pin and the X1 pin, crystal oscillator (or ceramic resonator), and the bypass capacitor to be grounded to the close position to the device.

The printed circuit board artwork is recommended to surround the X0 pin and X1 pin by ground circuits.

■Mode pins (MD2, MD1, MD0)
Connect the MD2, MD1and MD0 mode pin to the VCC pin or VSS pin directly. To prevent an erroneous selection of test mode caused by the noise, reduce the pattern length between each mode pin and the VCC pin or VSS pin on the printed circuit board. Also, use the low-impedance pin connection.

■During power-on
To prevent a malfunction of the voltage step-down circuit built in the device, set the voltage rising time to have 50µs or longer (between 0.2V and 2.7V) during power-on.

■Notes during PLL clock operation
When the PLL clock is selected and if the oscillator is disconnected or if the input is stopped, this clock may continue to operate at the free running frequency of the self-oscillator circuit built in the PLL clock. This operation is not guaranteed.

■Treatment of A/D converter power supply pins
Connect the pins to have AVCC5=AVRH5=VCC5 and AVSS5/AVRL5=VSS even if the A/D converter is not used.

Also, similarly connect the pins of NTSC A/D converter power supply to have AVCC3=VCC3 and AVSS3=VSS. At this time, open VIN/REFOUT.

■Notes on using external clock
An external clock is not supported. None of the external direct clock input can be used for both main clock and sub clock.

■Power-on sequence of A/D converter analog inputs
Be sure to turn on the digital power supply (Vcc5) first, and then turn on the A/D converter power supplies (AVcc5, AVRH5, AVRL5) and analog inputs (AN0 to AN31). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (Vcc5). When the AVRH5 pin voltage is turned on or off, it must not exceed AVCC5. Even if a common analog input pin is used as an input port, its input voltage must not exceed AVcc5. (However, the analog power supply and digital power supply can be turned on or off simultaneously.)

Be sure to similarly turn on the digital power supply (VCC3) first, and then turn on the A/D converter power supply (AVCC3) for NTSC and NTSC inputs (VIN, AVR). Also, turn off the A/D converter power supplies and analog inputs first, and then turn off the digital power supply (VCC3).

■Treatment of power supplies for high current output buffer pins (DVcc, DVss)
Be sure to turn on the digital power supply (Vcc) first, and then turn on the power supplies for high current output buffer pins (DVcc, DVss). Also, turn off the power supplies for high current output buffer pins first, and then turn off the digital power supply (Vcc).

Even if the high current output buffer pins are used as general-purpose ports, the power supplies of high current output buffer pins (DVcc, DVss) must be powered. (The power supplies of high current output buffer pins and the digital power supplies can be turned on or off simultaneously.)

■Treatment of C pin
This device contains a voltage step-down circuit. A capacitor must always be connected to the C pin to assure the internal stabilization of the device. For the standard values, see the "Recommended Operating Conditions" of the latest data sheet.

■Function switching of a multiplexed port
To switch between the port function and the multiplexed pin function, use the PFR (port function register).

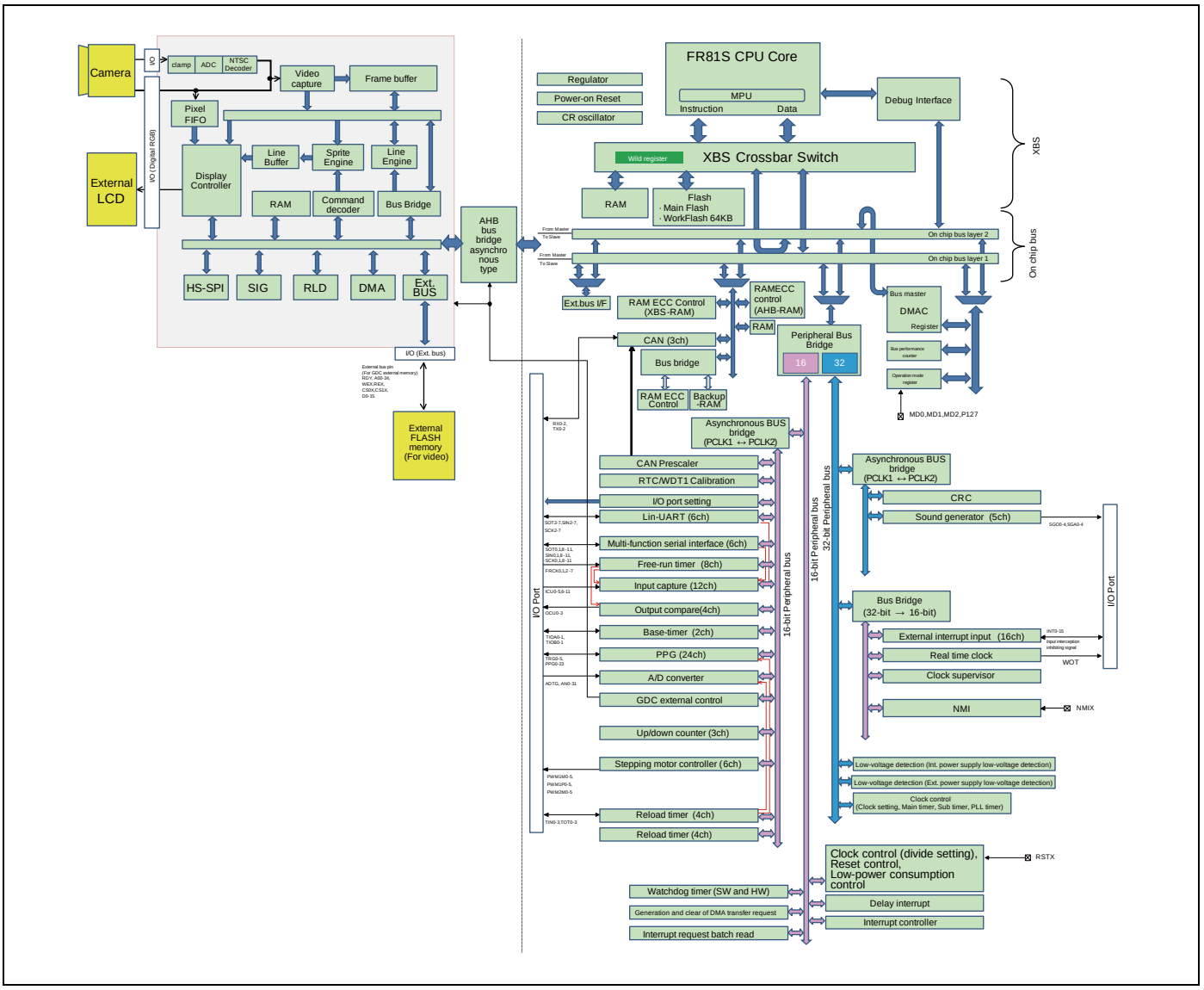
■Low-power consumption mode
To transit to the sleep mode, watch mode, stop mode, watch mode(power-off) or stop mode(power-off), follow the procedure explained in the "Activating the sleep mode, watch mode, or stop mode" or the "Activating the watch mode (power-off) or stop mode(power-off)" of " POWER CONSUMPTION CONTROL".

Power supply for GDC can be turned off separately from the microcontroller.

Take the following notes when using a monitor debugger.

- Do not set a break point for the low-power consumption transition program.
- Do not execute an operation step for the low-power consumption transition program.

■MB91F59A/59B



Note: I/O of peripheral functions can be confirmed at "PIN ASSIGNMENT" and "PIN DESCRIPTION".

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000310_H	—	—	MPUCR [R/W] H 000000-0 ----0100		MPU [S] (Only the CPU can access this area)
000314_H	—	—	—	—	
000318_H	—				
$00031C_H$	—	—	—		
000320_H	DPVAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000324_H	—	—	DPVSR [R/W] H -------- 00000--0		
000328_H	DEAR [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00032C_H$	—	—	DESR [R/W] H -------- 00000--0		
000330_H	PABR0 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000334_H	—	—	PACR0 [R/W] H 000000-0 00000--0		
000338_H	PABR1 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00033C_H$	—	—	PACR1 [R/W] H 000000-0 00000--0		
000340_H	PABR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000344_H	—	—	PACR2 [R/W] H 000000-0 00000--0		
000348_H	PABR3 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00034C_H$	—	—	PACR3 [R/W] H 000000-0 00000--0		
000350_H	PABR4 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				MPU [S] (Only the CPU can access this area)
000354_H	—	—	PACR4 [R/W] H 000000-0 00000--0		
000358_H	PABR5 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00035C_H$	—	—	PACR5 [R/W] H 000000-0 00000--0		
000360_H	PABR6 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
000364_H	—	—	PACR6 [R/W] H 000000-0 00000--0		
000368_H	PABR7 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXX0000				
$00036C_H$	—	—	PACR7 [R/W] H 000000-0 00000--0		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000400_H	ICSEL0[R/W] B, H, W -----000	ICSEL1[R/W] B, H, W -----000	ICSEL2[R/W] B, H, W -------0*1 ------00*2	ICSEL3[R/W] B, H, W -------0*1 ------00*2	Generation and clear of DMA transfer request *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
000404_H	ICSEL4[R/W] B, H, W -------0	ICSEL5[R/W] B, H, W -------0	ICSEL6[R/W] B, H, W -----000	ICSEL7[R/W] B, H, W -----000	
000408_H	ICSEL8[R/W] B, H, W ------00	ICSEL9[R/W] B, H, W ------00*1 -----000*2	ICSEL10[R/W] B, H, W ------00*1 -----000*2	ICSEL11[R/W] B, H, W ------00	
$00040C_H$	ICSEL12[R/W] B, H, W ------00	ICSEL13[R/W] B, H, W -------0	ICSEL14[R/W] B, H, W -------0	ICSEL15[R/W] B, H, W --------*1 -------0*2	
000410_H	ICSEL16[R/W] B, H, W --------*1 -------0*2	ICSEL17[R/W] B, H, W --------*1 -------0*2	ICSEL18[R/W] B, H, W --------*1 -------0*2	ICSEL19[R/W] B, H, W -----000	
000414_H	ICSEL20[R/W] B, H, W -----000	ICSEL21[R/W] B, H, W ------00	ICSEL22[R/W] B, H, W ------00	—	
000418_H	IRPR0H[R] B, H, W 00------*1 0000----*2	IRPR0L[R] B, H, W 00------*1 0000----*2	IRPR1H[R] B, H, W 00------	IRPR1L[R] B, H, W 00------	Interrupt request batch read register *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
$00041C_H$	IRPR2H[R] B, H, W 00------	IRPR2L[R] B, H, W 00------	IRPR3H[R] B, H, W 000000--	IRPR3L[R] B, H, W 000000--	
000420_H	IRPR4H[R] B, H, W 0000----*1 00000---*2	IRPR4L[R] B, H, W 0000----*1 000000--*2	IRPR5H[R] B, H, W 0000----*1 00000---*2	IRPR5L[R] B, H, W 0-------*1 000-----*2	
000424_H	IRPR6H[R] B, H, W 00--0---*1 00000---*2	IRPR6L[R] B, H, W 000-----*1 0000----*2	IRPR7H[R] B, H, W -00-----*1 -0000---*2	IRPR7L[R] B, H, W ------0-*1 ------00*2	
000428_H	IRPR8H[R] B, H, W 00------*1 0000----*2	IRPR8L[R] B, H, W 00------*1 0000----*2	IRPR9H[R] B, H, W 00------	IRPR9L[R] B, H, W 00------	
$00042C_H$	IRPR10H[R] B, H, W 00------	IRPR10L[R] B, H, W 00------	IRPR11H[R] B, H, W 00------	IRPR11L[R] B, H, W 00------	Interrupt request batch read register MB91F59A/B only
000430_H	IRPR12H[R] B, H, W 00------	IRPR12L[R] B, H, W 00------	IRPR13H[R] B, H, W 000-----*1 00000---*2	IRPR13L[R] B, H, W 00000---*1 0000000-*2	Interrupt request batch read register *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
000434_H	IRPR14H[R] B, H, W 00000000	IRPR14L[R] B, H, W 00000000	IRPR15H[R] B, H, W 000-----*1 0000----*2	—	
000438_H, $00043C_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000490_H	IORR0[R/W] B, H, W -0000000	IORR1[R/W] B, H, W -0000000	IORR2[R/W] B, H, W -0000000	IORR3[R/W] B, H, W -0000000	DMA transfer request from a peripheral [S]
000494_H	IORR4[R/W] B, H, W -0000000	IORR5[R/W] B, H, W -0000000	IORR6[R/W] B, H, W -0000000	IORR7[R/W] B, H, W -0000000	
000498_H	IORR8[R/W] B, H, W -0000000	IORR9[R/W] B, H, W -0000000	IORR10[R/W] B, H, W -0000000	IORR11[R/W] B, H, W -0000000	
$00049C_H$	IORR12[R/W] B, H, W -0000000	IORR13[R/W] B, H, W -0000000	IORR14[R/W] B, H, W -0000000	IORR15[R/W] B, H, W -0000000	
$0004A0_H$	—	—	—	—	Reserved
$0004A4_H$	CANPRE [R/W] B,H,W ----0000	—	—	—	CAN prescaler
$0004A8_H$	CPCLR6 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 6 MB91F59A/B only
$0004AC_H$	TCDT6 [R/W] W 00000000 00000000 00000000 00000000				
$0004B0_H$	TCCSH6 [R/W] B, H, W 0-----00	TCCSL6 [R/W] B, H, W -1-00000	—		
$0004B4_H$	—	—	—	—	Reserved
$0004B8_H$	CUCR0 [R/W] B,H,W -------- ---0--00		CUTD0 [R/W] B,H,W 10000000 00000000		RTC/WDT1 calibration (Calibration)
$0004BC_H$	CUTR0 [R] B,H,W -------- 00000000 00000000 00000000				
$0004C0_H$	—	—	—	—	
$0004C4_H$	CUCR1 [R/W] B,H,W -------- ---0--00		CUTD1[R/W] B,H,W 11000011 01010000		
$0004C8_H$	CUTR1 [R] B,H,W -------- 00000000 00000000 00000000				
$0004CC_H$	CRTR [R/W] B,H,W 01111111	—	—	—	RC trimming setting register
$0004D0_H$	CPCLR7 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 7 MB91F59A/B only
$0004D4_H$	TCDT7 [R/W] W 00000000 00000000 00000000 00000000				
$0004D8_H$	TCCSH7 [R/W] B, H, W 0-----00	TCCSL7 [R/W] B, H, W -1-00000	—		
$0004DC_H$	—	—	—	—	Reserved
$0004E0_H$	SCR8 [R/W] B,H,W 0--00000	SMR8 [R/W] B,H,W 000-0000	SSR8 [R/W] B,H,W 0-000011	ESCR8 [R/W] B,H,W -0000000	Multi-function serial 8 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0004E4_H$	RDR8/(TDR8)[R/W] B,H,W *1 -------0 00000000		BGR8 [R/W] H,W 00000000 00000000		
$0004E8_H$	—	—	—	—	
$0004EC_H$	FCR18 [R/W] B,H,W ---00100	FCR08 [R/W] B,H,W -0000000	FBYTE28 [R/W] B,H,W 00000000	FBYTE18 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000CAC$_H$	DDAR10[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMA controller [S]
000CB0$_H$	DCCR11[R/W] W 0----000 --00--00 00000000 0-000000				
000CB4$_H$	DCSR11[R/W] H 0------- -----000		DTCR11[R/W] H 00000000 00000000		
000CB8$_H$	DSAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CBC$_H$	DDAR11[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CC0$_H$	DCCR12[R/W] W 0----000 --00--00 00000000 0-000000				
000CC4$_H$	DCSR12[R/W] H 0------- -----000		DTCR12[R/W] H 00000000 00000000		
000CC8$_H$	DSAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CCC$_H$	DDAR12[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CD0$_H$	DCCR13[R/W] W 0----000 --00--00 00000000 0-000000				
000CD4$_H$	DCSR13[R/W] H 0------- -----000		DTCR13[R/W] H 00000000 00000000		
000CD8$_H$	DSAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CDC$_H$	DDAR13[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CE0$_H$	DCCR14[R/W] W 0----000 --00--00 00000000 0-000000				
000CE4$_H$	DCSR14[R/W] H 0------- -----000		DTCR14[R/W] H 00000000 00000000		
000CE8$_H$	DSAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CEC$_H$	DDAR14[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CF0$_H$	DCCR15[R/W] W 0----000 --00--00 00000000 0-000000				
000CF4$_H$	DCSR15[R/W] H 0------- -----000		DTCR15[R/W] H 00000000 00000000		
000CF8$_H$	DSAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000CFC$_H$	DDAR15[R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000D00$_H$ to 000DF0$_H$	—	—	—	—	Reserved [S]
000DF4$_H$	—	—	DNMIR[R/W] B 0------0	DILVR[R/W] B ---11111	DMA controller [S]
000DF8$_H$	DMACR[R/W] W 0------- -------- 0------- --------				
000DFC$_H$	—	—	—	—	Reserved [S]

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
$000E10_H$	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
$000E14_H$	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
$000E18_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
$000E30_H$	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
$000E34_H$	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	
$000E38_H$ to $000E3C_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002500_H	SEEARH[R] B,H,W --000000 00000000		DEEARH[R] B,H,W --000000 00000000		AHB RAM ECC control register MB91F59A/B only
002504_H	EECSRH[R/W] B,H,W ----0000	—	EFEARH[R/W]B,H,W --000000 00000000		
002508_H	—	EFECRH[R/W]B,H,W -------0 00000000 00000000			
$00250C_H$ to $002FFC_H$	—	—	—	—	Reserved
003000_H	SEEARA[R] B,H,W -----000 00000000		DEEARA[R] B,H,W -----000 00000000		Backup RAM ECC control register
003004_H	EECSRA [R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$ to $003FFC_H$	—	—	—	—	Reserved
004000_H to $005FFC_H$	Backup RAM				Backup RAM area
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—	—	—	—	Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ to $00FFF4_H$	—	—	—	—	Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]:It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

11.3 DC Characteristics

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

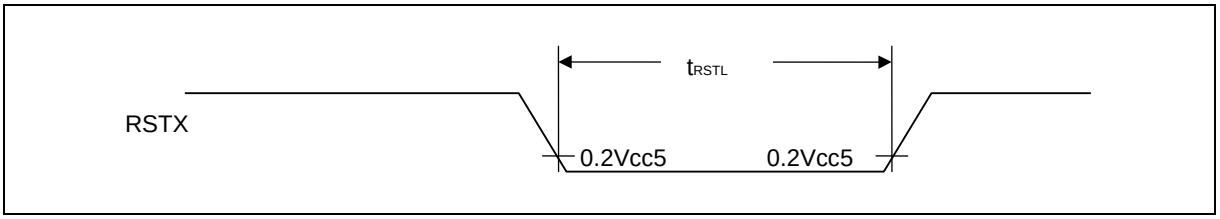
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	CMOS input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH2}		CMOS hysteresis input level is selected	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH3}		Automotive input level is selected	0.8× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH4}		TTL input level is selected	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH5}	RSTX, NMIX, MD2	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH7}	MD0,MD1	–	0.7× $V_{CC}5$	–	$V_{CC}5$+ 0.3	V	
	V_{IH8}	DEBUGIF	–	2.0	–	$V_{CC}5$+ 0.3	V	
	V_{IH10}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	CMOS hysteresis input level is selected	0.7× $V_{CC}3$	–	$V_{CC}3$+ 0.3	V	3.3V dedicated pin
	V_{IH11}		TTL input level is selected	2.0	–	$V_{CC}3$+ 0.3	V	
	V_{IH12}	MD3	-	0.8× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only
	V_{IH13}	TDI, TMS, TRST, TCK	-	0.7× $V_{CC}5$	-	$V_{CC}5$+ 0.3	V	BGA product only

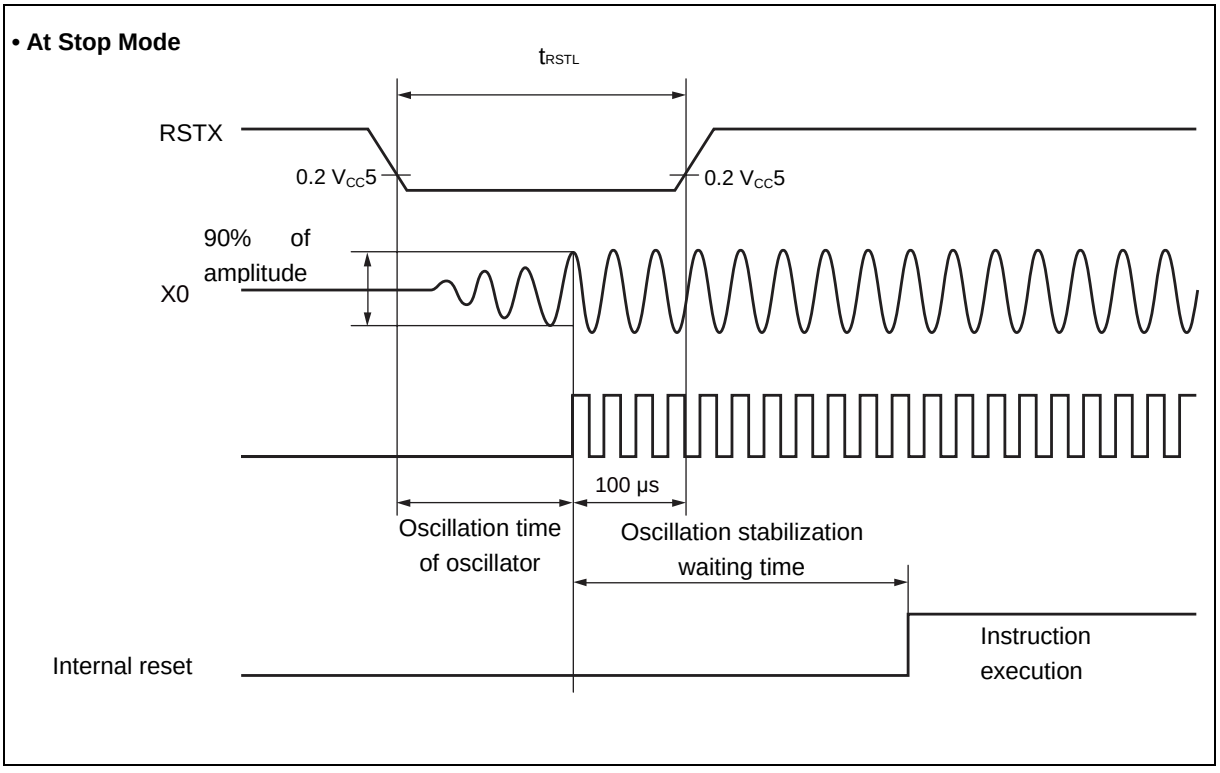
11.4.1.2 Reset Input

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Reset input time	t_{RSTL}	RSTX	–	10	–	µs	When normal operation
				Oscillation time of oscillator* + 100µs	–	ms	At Stop mode
				100µs	–	µs	At RTC mode
Width for reset input removal				1µs	–	µs	

*:The oscillation time of the oscillator is the time it takes for the amplitude of the oscillations to reach 90%. For crystal oscillators, this time is between several ms and several tens of ms, for ceramic oscillators the time is between several hundred µs and several ms, and for an external clock, the time is 0 ms.





■Bit setting: SMR: MD2=0, SMR: MD1=1, SMR: MD0=0, SMR: SCINV=1, SCR: SPI=1

(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock cycle time	t_{SCYC}	SCKx	Internal shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	$4t_{CPP}$	–	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKx, SOTx		-30	+30	ns
Valid SIN → SCK ↑ setup time	t_{IVSHI}	SCKx, SINx		34	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXI}			0	–	ns
SOT → SCK ↑ delay time	t_{SOVHI}	SCKx, SOTx		$2t_{CPP}$-30	–	ns
Serial clock "H"pulse width	t_{SHSL}	SCKx	External shift clock mode C_L=50pF(When drive capability is 2mA or more.) C_L=20pF(When drive capability is 1mA)	t_{CPP}+10	–	ns
Serial clock "L" pulse width	t_{SLSH}			$2t_{CPP}$-10	–	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKx, SOTx		–	33	ns
Valid SIN → SCK ↑ setup time	t_{IVSHE}	SCKx, SINx		10	–	ns
SCK ↑ → Valid SIN hold time	t_{SHIXE}			20	–	ns
SCK fall time	t_F	SCKx		–	5	ns
SCK rise time	t_R	SCKx		–	5	ns

Notes:

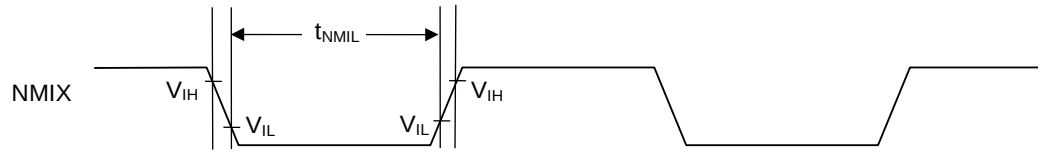
- AC characteristic in CLK synchronized mode.
- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.
- "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.

11.4.1.8 NMI input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{NMIL}	NMIX	–	$4t_{CPP}$	–	ns	

• NMIX Input Timing



■AC Timing Specifications

Parameter	Symbol	min.
Display clock cycle time	t_{dcyc}	18.5 ns

External Load Condition 50 pF

Parameter	Symbol	DCLKO Reference Edge	IO Drive capability Setting		Remark
			10 mA	2 mA	
Setup time	t_{dosu}	neg, pos *1	t_{dcyc}_f - 8.5ns	t_{dcyc}_f - 10.2ns	
Hold time	t_{dohd}	-	t_{dcyc}_l - 1.7ns	t_{dcyc}_l - 3.3ns	*2
		-	t_{dcyc}_l - 3.2ns	t_{dcyc}_l – 5.1ns	*3

*1: DCLKO reference edge: This is the reference clock edge for setup time and hold time.
Pos = The external display device receives the signal at the rising edge of DCLKO.
Neg = The external display device receives the signal at the falling edge of DCLKO.

*2: Should be applied to RGB666.

*3: Should be applied to RGB888.

11.6 Flash Memory

11.6.1 Electrical Characteristics

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	–	200	800	ms	8 Kbyte sector*1, excluding internal preprogramming time
	–	300	1100	ms	8 Kbyte sector*1, including internal preprogramming time
	–	400	2000	ms	64 Kbyte sector*1, excluding internal preprogramming time
	–	700	3700	ms	64 Kbyte sector*1, including internal preprogramming time
8-bit writing time	–	9	288	µs	Exclusive of overhead time at system level*1
16-bit writing time	–	12	384	µs	Exclusive of overhead time at system level*1
ECC writing time	–	9	288	µs	Exclusive of overhead time at system level*1
Erase cycle*2/ Data retain time	1,000 cycles/ 20 years, 10,000 cycles/ 10 years, 100,000 cycles/ 5 years	–	–	–	Average T_A=+85°C*3

*1: The guaranteed value for erasure up to 100,000 cycles.

*2: Number of erase cycles for each sector.

*3: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

11.6.2 Notes

While the Flash memory is written or erased, shutdown of the external power (Vcc5) is prohibited.
In the application system where Vcc5 might be shut down while writing or erasing, be sure to turn the power off by using an external voltage detection function.
To put it concretely, after the external power supply voltage falls below the detection voltage (V_{DL}*), hold Vcc5 at 2.7V or more within the duration calculated by the following expression:

Td*[µs] + (period of PCLK [µs] x 257) + 50 [µs]

*: See " AC Characteristics Low voltage detection (External low-voltage detection) "

12. Ordering Information

Part Number	Package[*1]
MB91F591BPMC-GSE1	208-pin plastic LQFP (LQR208)
MB91F591BSPMC-GSE1	
MB91F591BHPMC-GSE1	
MB91F591BHSPMC-GSE1	
MB91F592BPMC-GSE1	
MB91F592BSPMC-GSE1	
MB91F592BHPMC-GSE1	
MB91F592BHSPMC-GSE1	
MB91F594BPMC-GSE1	
MB91F594BSPMC-GSE1	
MB91F594BHPMC-GSE1	
MB91F594BHSPMC-GSE1	
MB91F59BCEQ-GSE1	208-pin plastic TEQFP (LET208)
MB91F59BCHSEQ-GSE1	
MB91F59ACPB-GSE1	320-Ball Grid Array Package (BYA320)
MB91F59ACSPB-GSE1	
MB91F59ACHPB-GSE1	
MB91F59ACHSPB-GSE1	
MB91F59BCPB-GSE1	
MB91F59BCSPB-GSE1	
MB91F59BCHPB-GSE1	
MB91F59BCHSPB-GSE1	

[*1]: For details of the package, see "Package Dimensions ".