Infineon Technologies - MB91F594BPMC-GSK5E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	872K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f594bpmc-gsk5e1

- Multi-function serial communication (built-in transmission/reception FIFO memory) :
  - 2 channels for MB91F591/2/4/6/7/9
  - 6 channels for MB91F59A/B

  < UART (Asynchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Parity or no parity is selectable.
  - Built-in dedicated baud rate generator
  - An external clock can be used as the transfer clock
  - Parity, frame, and overrun error detect functions provided
  - DMA transfer support

  <CSIO (Synchronous serial interface) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - SPI supported; master and slave systems supported; 5 to 9-bit data length can be set.
  - Built-in dedicated baud rate generator (Master operation)
  - An external clock can be entered. (Slave operation)
  - Overrun error detect function is provided
  - DMA transfer support

  <LIN-UART (Asynchronous Serial Interface for LIN) >
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - LIN protocol Revision 2.1 supported
  - Master and slave systems supported
  - Framing error and overrun error detection
  - LIN synch break generation and detection; LIN synch delimiter generation
  - Built-in dedicated baud rate generator
  - An external clock can be adjusted by the reload counter
  - DMA transfer support

  < I^2C >
  - ch.0 and ch.1 only supported
  - Full-duplex double buffering system, 16-byte transmission FIFO memory, 16-byte reception FIFO memory
  - Standard mode (Max. 100kbps) / high-speed mode (Max. 400kbps) supported
  - DMA transfer supported (for transmission only)
- CAN Controller (C-CAN) : 3 channels
  - Transfer speed : Up to 1Mbps
  - 64-transmission/reception message buffering : 1 channel, 32-transmission/reception message buffering : 2 channels
- Up/down counter: 16-bit × 3 channels for MB91F59A/B
- PPG : 16-bit × 24 channels
- Reload timer :
  - 16-bit × 4 channels for MB91F591/2/4/6/7/9
  - 16-bit × 8 channels for MB91F59A/B
- Free-run timer :
  - 32-bit × 2 channels (Can select each channel for input capture, output compare) for MB91F591/2/4/6/7/9
  - 32-bit × 2 channels (LSYN (LIN synch field detection) for exclusive input capture) for MB91F591/2/4/6/7/9
  - 32-bit × 8 channels (Can select ch.0, 1, 2, and 3 for input capture, output compare) for MB91F59A/B
- Input capture :
  - 32-bit × 6 channels (linked to the free-run timer) for MB91F591/2/4/6/7/9
  - 32-bit × 2 channels (linked to the free-run timer) LSYN (LIN synch field detected) Exclusive for MB91F591/2/4/6/7/9
  - 32-bit × 12 channels (linked to the free-run timer) LSYN (LIN synch field detected) for MB91F59A/B
- Output compare : 32-bit × 4 channels (linked to the free-run timer)
- Sound generator : 5 channels
  - Frequency and amplitude sequencers provided
- Stepping motor controller : 6 channels
  - 8/10-bit PWM
  - High current output supported (4 lines × 6 channels)
  - Can refer back electromotive force using pin-shared A/D converter
- Real-time clock (RTC) (for day, hours, minutes, seconds)
  - Main/sub oscillation frequency can be selected for the operation clock (dual product only)
- Calibration: The hardware watchdog for CR oscillation drive and real-time clock (RTC) for sub clock drive (dual product only)
  - The CR oscillation frequency can be trimmed
  - The main clock to sub clock (dual product only) ratio can be corrected by setting the real-time clock prescaler
- Clock Supervisor
  - Monitoring abnormality (damage of crystal etc.) of sub oscillation (32kHz) (two system clock kinds) of the outside and main oscillation (4 MHz)
  - When abnormality is detected, it switches to the CR clock.
- Base timer : 2 channels
  - 16-bit timer
  - Any of four PWM/PPG/PWC/reload timer functions can be selected and used
  - As for the functions of PWC and reload timer, 2 channels of cascade mode can be used as 32-bit timer.
- CRC generation
- Watchdog timer
  - Hardware watchdog
  - Software watchdog
- NMI
- Interrupt controller
- Interrupt request batch read
  - Multiple interrupts from peripherals can be read by a series of registers.

Item \ Product		MB91F592B /BS	MB91F592BH /BHS	MB91F594B /BS	MB91F594BH /BHS
CPU core		FR81S			
Technology		90nm			
Package		LQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		80MHz			
Maximum GDC operating frequency		81MHz			
Built-in CR oscillator		100kHz			
System clock		On chip PLL			
Flash	Main	576KB		1088KB	
	Work	64KB			
RAM	Main	40KB		64KB	
	Backup	8KB			
VRAM		800KB			
Watchdog timer		1ch Hardware 1ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16ch			
CAN		1ch (64msg) 2ch (32msg)			
LIN-UART		6ch			
Multi-function Serial Interface		2ch			
A/D converter (8bit/10bit)		1unit/32ch			
Reload timer(16bit)		4ch			
Base timer(16bit)		2ch			
Free-run timer(32bit)		2ch			
Input capture(32bit)		6ch			
Output compare(32bit)		4ch			
PPG timer(16bit)		24ch			
Sound generator		5ch			
Real-time clock		Yes			
External interrupt		16ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature		-40°C to +105°C			
Allowable power [mW]		1250			
Others		Flash product			
On chip debugger		Yes			

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
126, 136, 146, 156	DVCC	–	–	SMC large current port power supply pin
125, 135, 145, 155	DVSS	–	–	SMC large current port GND pin
89, 105, 122, 173	VCC5	–	–	+5.0V power supply pin
1, 18, 37, 53, 71, 175, 189	VCC3	–	–	+3.3V power supply pin
19, 36, 52, 72, 82, 88, 104, 123, 170, 174, 188, 208	VSS	–	–	GND pin

[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

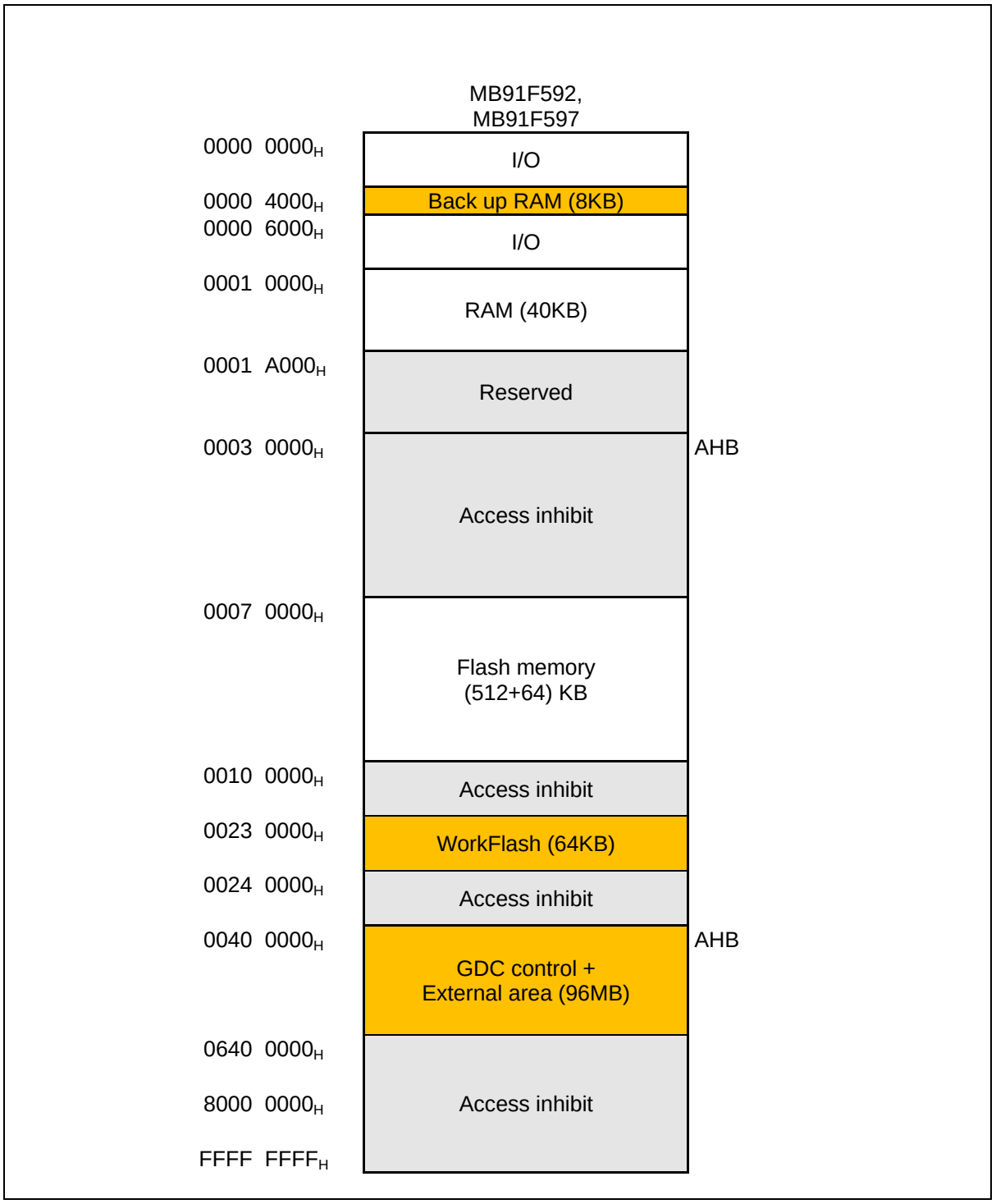
BGA Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
72	GOUT7	–	O	Display digital G7 output pin
	PE7			General-purpose I/O port (3V pin)
73	GOUT4	–	O	Display digital G4 output pin
	PE4			General-purpose I/O port (3V pin)
74	ROUT7	–	O	Display digital R7 output pin
	PD7			General-purpose I/O port (3V pin)
75	ROUT4	–	O	Display digital R4 output pin
	PD4			General-purpose I/O port (3V pin)
76	VSS	–	–	GND pin
77	VSS	–	–	GND pin
78	VSS	–	–	GND pin
79	AVSS3	–	–	NTSC AD convertor GND pin
80	AVR3	–	S	"L" side reference voltage for NTSC A/D converter pin
81	AVSS3	–	–	NTSC AD convertor GND pin
82	BIN6	–	O	Capture B6 input pin (RGB mode)
	PC6			General-purpose I/O port (3V pin)
83	BIN3	–	O	Capture B3 input pin (RGB mode)
	PC3			General-purpose I/O port (3V pin)
84	GIN6	–	O	Capture G6 input pin (RGB mode)
	PB6			General-purpose I/O port (3V pin)
85	GIN3	–	O	Capture G3 input pin (RGB mode)
	VIN7			Capture VIN7 input pin (656 mode)
	PB3			General-purpose I/O port (3V pin)
86	RIN6	–	O	Capture R6 input pin (RGB mode)
	VIN4			Capture VIN4 input pin (656 mode)
	PA6			General-purpose I/O port (3V pin)
87	RIN3	–	O	Capture R3 input pin (RGB mode)
	VIN1			Capture VIN1 input pin (656 mode)
	PA3			General-purpose I/O port (3V pin)
88	P122	–	C	General-purpose I/O port
	SCK5			LIN-UART ch.5 clock I/O pin
	OCU0			Output compare ch.0 output pin
	PPG7_2			PPG ch.7 output pin (2)
	TOT3			Reload timer ch.3 output pin
89	VSS	–	–	GND pin
90	MD2	–	F2	Mode pin 2
91	FRCK7	–	C	Free-run timer 7 clock input pin
	P114			General-purpose I/O port
	ICU5_1			Input capture ch.5 input pin (1)
	SCK3			LIN-UART ch.3 clock I/O pin
	TRG3			PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1			Reload timer ch.1 event input pin
	SGA2			Sound generator ch.2 SGA output pin
92	RX2	–	C	CAN reception data 2 input pin
	P113			General-purpose I/O port
	INT11			INT11 External interrupt input pin
	PPG4_2			PPG ch.4 output pin (2)
	TIN7			Reload timer ch.7 event input pin
93	TDI	–	U	Test Data In (JTAG Boundary Scan Test)

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
94	VSS	–	–	GND pin
95	TRST	–	V	Test Reset (JTAG Boundary Scan Test)
96	AN30	–	E	ADC Analog 30 input pin
	P086			General-purpose I/O port
96	ICU3_2	–	E	Input capture ch.3 input pin (2)
	PPG22			PPG ch.22 output pin
	PWM2P5			SMC ch.5 output pin
97	AN27	–	E	ADC Analog 27 input pin
	P083			General-purpose I/O port
	ICU0_2			Input capture ch.0 input pin (2)
	PPG19			PPG ch.19 output pin
	PWM2M4			SMC ch.4 output pin
	UDCZIN2			Up/down counter ch.2 ZIN input pin
98	AN24	–	E	ADC Analog 24 input pin
	P080			General-purpose I/O port
	SIN6			LIN-UART ch.6 serial data input pin
	PPG16			PPG ch.16 output pin
	PWM1P4			SMC ch.4 output pin
	UDCAIN0_1			Up/down counter ch.0 AIN input pin (1)
99	AN21	–	E	ADC Analog 21 input pin
	P075			General-purpose I/O port
	ICU8			Input capture ch.8 input pin
	SIN7_1			LIN-UART ch.7 serial data input pin
	PPG13_1			PPG ch.13 output pin (1)
	PWM1M3			SMC ch.3 output pin
100	AN18	–	E	ADC Analog 18 input pin
	P072			General-purpose I/O port
	ICU11			Input capture ch.11 input pin
	SIN8			Multi-function serial ch.8 serial data input pin
	PWM2P2			SMC ch.2 output pin
101	AN15	–	E	ADC Analog 15 input pin
	P067			General-purpose I/O port
	SIN9			Multi-function serial ch.9 serial data input pin
	PWM2M1			SMC ch.1 output pin
	UDCAIN0			Up/down counter ch.0 AIN input pin
102	AN12	–	E	ADC Analog 12 input pin
	P064			General-purpose I/O port
	PWM1P1			SMC ch.1 output pin
	UDCAIN1			Up/down counter ch.1 AIN input pin
103	AN9	–	E	ADC Analog 9 input pin
	P061			General-purpose I/O port
	SOT10			Multi-function serial ch.10 serial data output pin
	PWM1M0			SMC ch.0 output pin
104	VSS	–	–	GND pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
251	VSS	–	–	GND pin
252	VCC3	–	–	+3.3V power supply pin
253	VCC3	–	–	+3.3V power supply pin
254	VSS	–	–	GND pin
255	VCC3	–	–	+3.3V power supply pin
256	VCC3	–	–	+3.3V power supply pin
257	GND	–	–	GND pin
:	:	:	:	:
:	:	:	:	:
:	:	:	:	:
320	GND	–	–	GND pin

[*1]: For the I/O circuit types, see "I/O Circuit Type".
[*2]: For switching, see "I/O Port" of Hardware Manual.

■Memory map


MB91F592,
MB91F597
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (40KB)
0001 A000H
Reserved
0003 0000H
AHB
Access inhibit
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
AHB
GDC control +
External area (96MB)
0640 0000H
Access inhibit
8000 0000H
FFFF FFFFH

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000E60H	EPFR00[R/W] B,H,W 00000000	EPFR01[R/W] B,H,W ----0000*1 00000000*2	EPFR02[R/W] B,H,W ---00000	EPFR03[R/W] B,H,W ---00000	Extended port function register *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
000E64H	EPFR04[R/W] B,H,W ---00000	EPFR05[R/W] B,H,W ---00000	EPFR06[R/W] B,H,W ---00000	EPFR07[R/W] B,H,W ---00000	
000E68H	EPFR08[R/W] B,H,W ---00000	EPFR09[R/W] B,H,W ---00000	EPFR10[R/W] B,H,W -0000000	EPFR11[R/W] B,H,W --000000	
000E6CH	EPFR12[R/W] B,H,W --000000	EPFR13[R/W] B,H,W --000000	EPFR14[R/W] B,H,W --000000	EPFR15[R/W] B,H,W -0000000	
000E70H	EPFR16[R/W] B,H,W 00000000	EPFR17[R/W] B,H,W 00000000	EPFR18[R/W] B,H,W 10000000	EPFR19[R/W] B,H,W 11111111	
000E74H	EPFR20[R/W] B,H,W -1111111	EPFR21[R/W] B,H,W 00000000	EPFR22[R/W] B,H,W 00000000	EPFR23[R/W] B,H,W 00000000	
000E78H	EPFR24[R/W] B,H,W -----000	EPFR25[R/W] B,H,W -----000	EPFR26[R/W] B,H,W ----0000	EPFR27[R/W] B,H,W ---00000	
000E7CH	EPFR28[R/W] B,H,W ------00	EPFR29[R/W] B,H,W 00000000	EPFR30[R/W] B,H,W 00000000	EPFR31[R/W] B,H,W 00000000	
000E80H	EPFR32[R/W] B,H,W 00000000	EPFR33[R/W] B,H,W ---00000	EPFR34[R/W] B,H,W ---00000	EPFR35[R/W] B,H,W ---00000	
000E84H	EPFR36[R/W] B,H,W ---00000	EPFR37[R/W] B,H,W 00000000	EPFR38[R/W] B,H,W ---00000	EPFR39[R/W] B,H,W 00000000	
000E88H	EPFR40[R/W] B,H,W --000000	EPFR41[R/W] B,H,W -----000	EPFR42[R/W] B,H,W ------00	EPFR43[R/W] B,H,W 00000000	
000E8CH	EPFR44[R/W] B,H,W 00000000	EPFR45[R/W] B,H,W 00000000	EPFR46[R/W] B,H,W --000000	EPFR47[R/W] B,H,W -------0	
000E90H	EPFR48[R/W] B,H,W 00000000	EPFR49[R/W] B,H,W 00000000	EPFR50[R/W] B,H,W 00000000	EPFR51[R/W] B,H,W ---00000	
000E94H	EPFR52[R/W] B,H,W -----000	EPFR53[R/W] B,H,W ---00000	EPFR54[R/W] B,H,W ----0000	EPFR55[R/W] B,H,W ------01	
000E98H	EPFR56[R/W] B,H,W --000000	EPFR57[R/W] B,H,W --000000	EPFR58[R/W] B,H,W ----0000	—	Extended port function register MB91F59A/B only
000E9CH	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000FAC$_H$	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 3
000FB0$_H$	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000FB4$_H$	TCCSH3 [R/W] B, H, W 0-----00	TCCSL3 [R/W] B, H, W -1-00000	—		
000FB8$_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 4 MB91F59A/B only
000FBC$_H$	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000FC0$_H$	TCCSH4 [R/W] B, H, W 0-----00	TCCSL4 [R/W] B, H, W -1-00000	—		
000FC4$_H$	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 5 MB91F59A/B only
000FC8$_H$	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FCC$_H$	TCCSH5 [R/W] B, H, W 0-----00	TCCSL5 [R/W] B, H, W -1-00000	—		
000FD0$_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 6,7 *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
000FD4$_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8$_H$	ICFS67 [R/W] B, H, W ------00	—	LSYNS1 [R/W] B,H,W ------00*1 --000000*2	ICS67 [R/W] B, H, W 00000000	
000FDC$_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 MB91F59A/B only
000FE0$_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4$_H$	ICFS89 [R/W] B, H, W ------00	—	—	ICS89 [R/W] B, H, W 00000000	
000FE8$_H$	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 10,11 MB91F59A/B only
000FEC$_H$	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0$_H$	ICFS1011 [R/W] B, H, W ------00	—	—	ICS1011 [R/W] B, H, W 00000000	
000FF4$_H$	RCRH2[W] H,W XXXXXXXX	RCRL2[W] B,H,W XXXXXXXX	UDCRH2[R] H,W 00000000	UDCRL2[R] B,H,W 00000000	Up/down counter 2 MB91F59A/B only
000FF8$_H$	CCR2[R/W] B,H 00000000 -0001000		—	CSR2[R/W] B 00000000	
000FFC$_H$	—	—	—	—	Reserved
001000$_H$	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Synchronous/asynchronous switching control
001004$_H$ to 00103C$_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$0010C0_H$	—	SGDER4[R/W] B,H,W 00000000	SGCR4[R/W] B,H,W -0000-0- 000--000		Sound generator 4
$0010C4_H$	SGAR4[R/W] B,H,W 00000000 00000000		SGFR4[R/W] B,H,W 00000000	SGNR4[R/W] B,H,W 00000000	
$0010C8_H$	SGTCR4[R/W] B,H,W 00000000	SGIDR4[R/W] B,H,W 00000000	SGPCR4[R/W] B,H,W 00000000 11111111		
$0010CC_H$	SGDMAR4[W] B,H,W 00000000 00000000 00000000 00000000				
$0010D0_H$ to $00112C_H$	—	—	—	—	Reserved
001130_H	—	—	—	CRCCR[R/W] B,H,W -0000000	CRC arithmetic operation
001134_H	CRCINIT[R/W] B,H,W 1111111 1111111 1111111 1111111				
001138_H	CRCIN[R/W] B,H,W 00000000 00000000 00000000 00000000				
$00113C_H$	CRCR[R] B,H,W 1111111 1111111 1111111 1111111				
001140_H to $0013FC_H$	—	—	—	—	Reserved
001400_H to $001FFC_H$	—	—	—	—	Reserved (3KB)

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002500_H	SEEARH[R] B,H,W --000000 00000000		DEEARH[R] B,H,W --000000 00000000		AHB RAM ECC control register MB91F59A/B only
002504_H	EECSRH[R/W] B,H,W ----0000	—	EFEARH[R/W]B,H,W --000000 00000000		
002508_H	—	EFECRH[R/W]B,H,W -------0 00000000 00000000			
$00250C_H$ to $002FFC_H$	—	—	—	—	Reserved
003000_H	SEEARA[R] B,H,W -----000 00000000		DEEARA[R] B,H,W -----000 00000000		Backup RAM ECC control register
003004_H	EECSRA [R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$ to $003FFC_H$	—	—	—	—	Reserved
004000_H to $005FFC_H$	Backup RAM				Backup RAM area
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—	—	—	—	Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ to $00FFF4_H$	—	—	—	—	Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

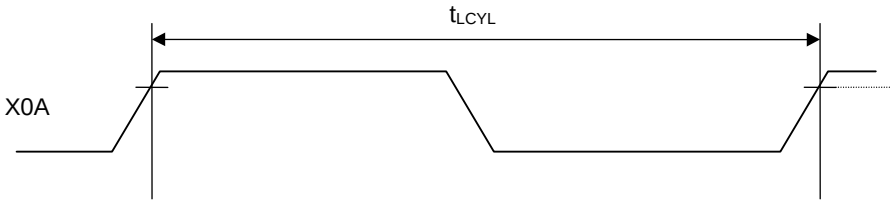
[S]:It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

11.4.1.1 Sub clock timing (products without s-suffix)

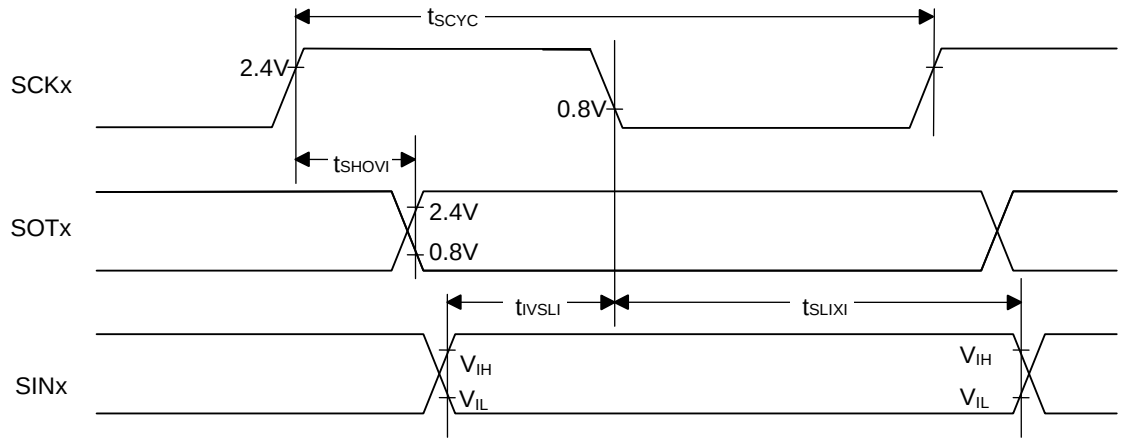
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Source oscillation clock frequency	F_{CL}	X0A, X1A	–	–	32.768	–	kHz	
Source oscillation clock cycle time	t_{LCYL}	X0A, X1A	–	–	30.52	–	µs	

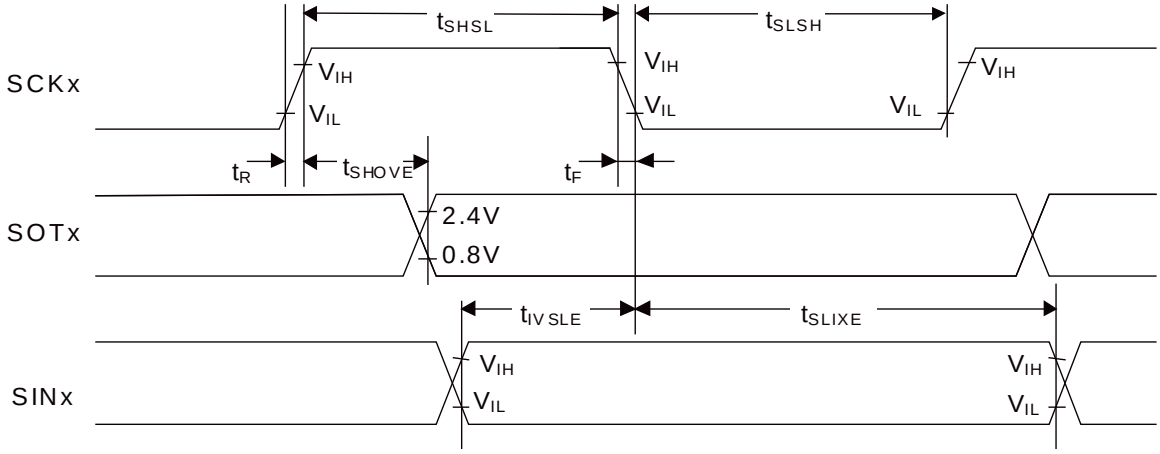
• X0A,X1A Clock Timing



• **Internal Shift Clock Mode**



• **External Shift Clock Mode**

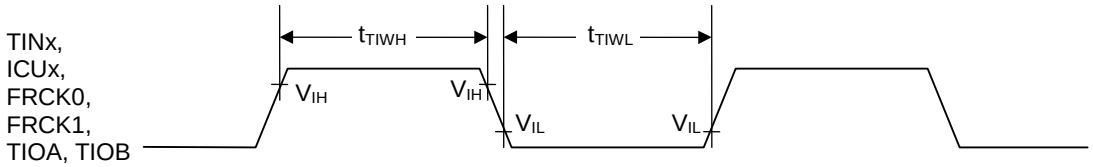


11.4.1.6 Timer input timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TIWH}, t_{TIWL}	TIN0 to TIN3, TIN7 to TIN10, ICU0 to ICU11, FRCK0 to FRCK7, TIOA,TIOB, UDCAIN0 to 2, UDCBIN0 to 2, UDCZIN0 to 2	–	$4t_{CPP}$	–	ns	

• **Timer Input Timing**



Note:

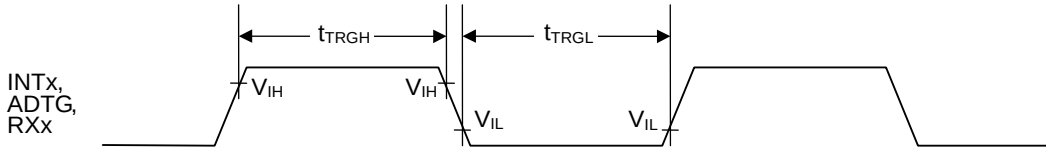
The description can be applied to FRCK2 to 7, UDCAIN0 to 2, UDCBIN0 to 2, and UDCZIN0 to 2 as well.

11.4.1.7 Trigger input timing

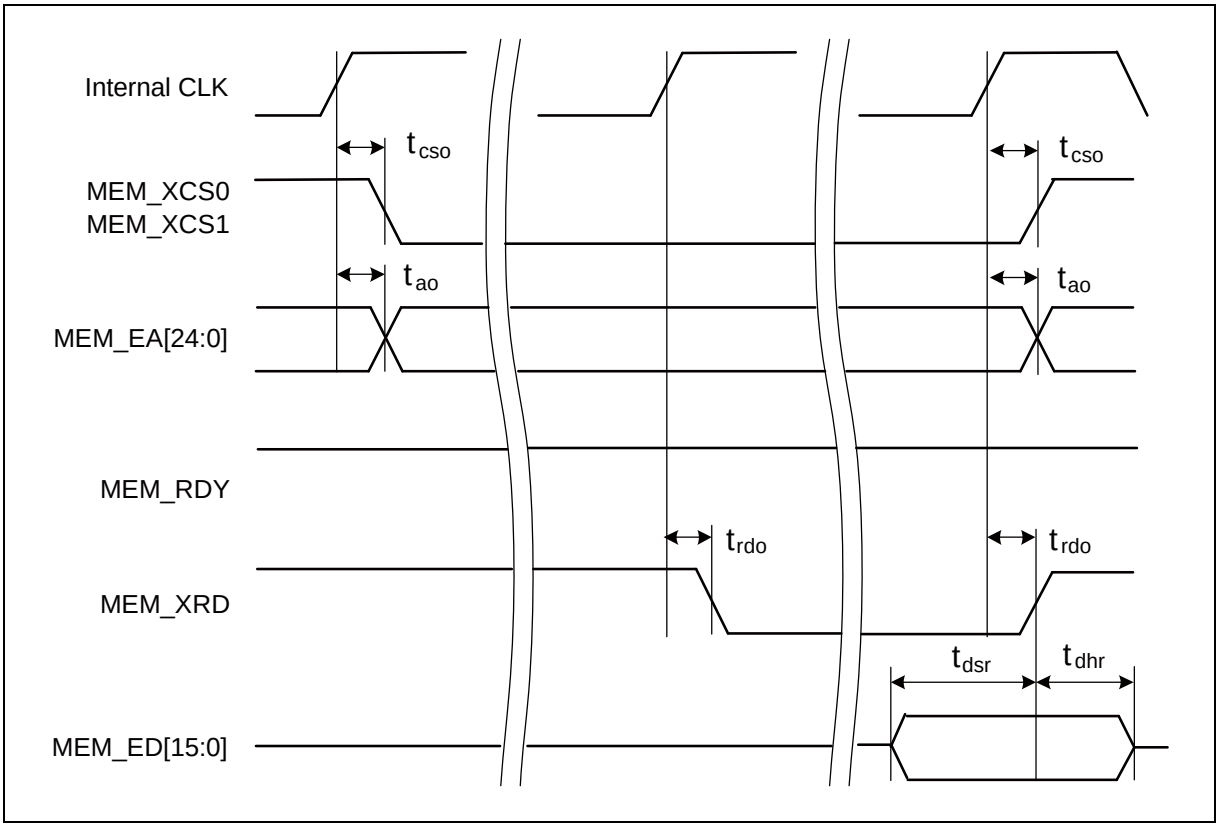
(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Input pulse width	t_{TRGH}, t_{TRGL}	INT0 to INT15, ADTG, RX0, RX1, RX2	–	$5t_{CPP}$	–	ns	
				1	–	µs	At stop mode

• **Trigger Input Timing**



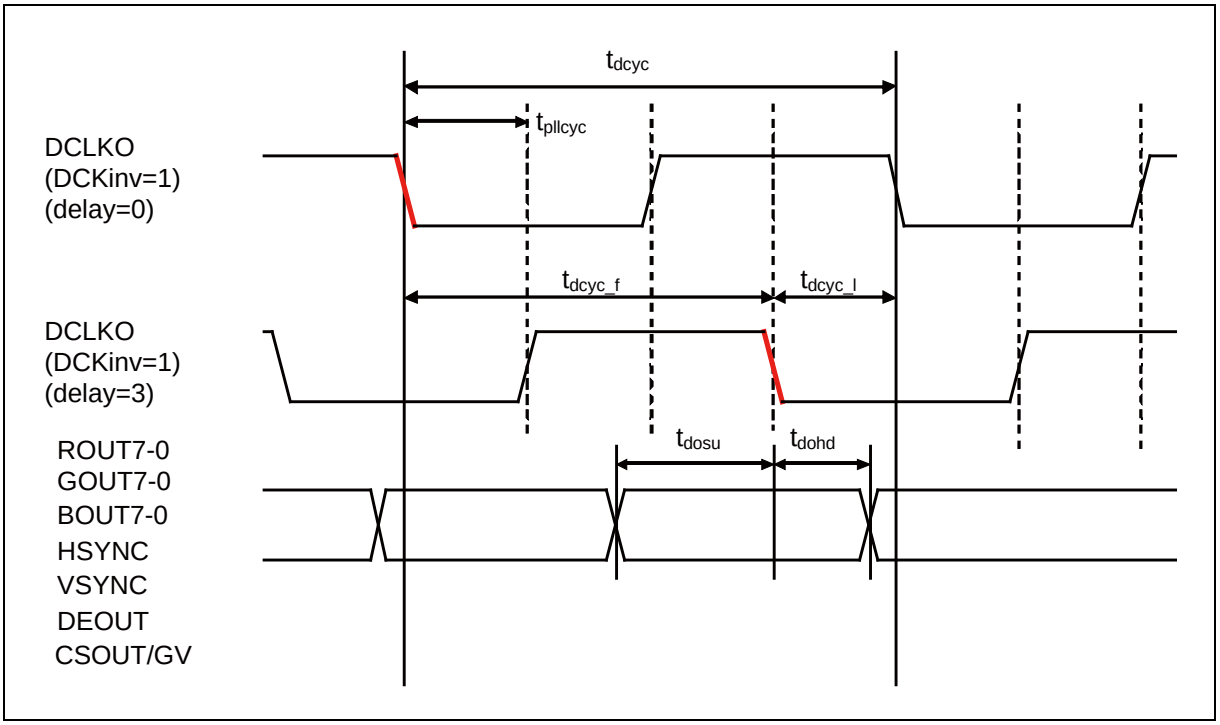
■NOR Flash read timing



Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

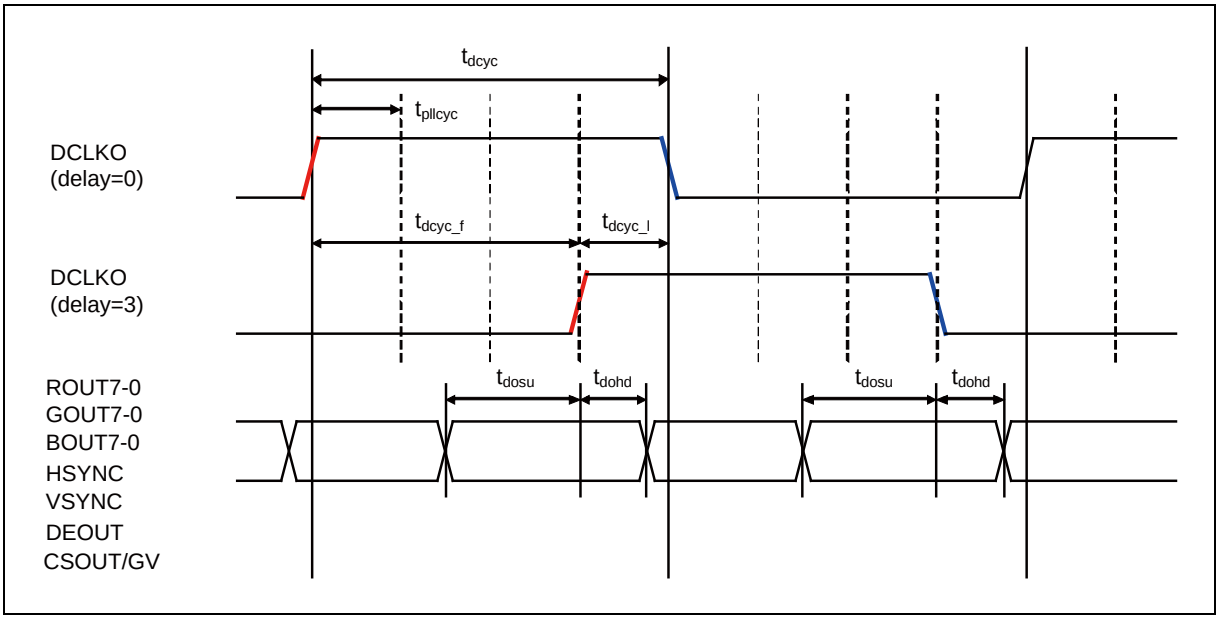
Figure 6. Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



Setup/Hold Definition in Delay Mode

The delay mode is a mode realized with DCLKO delay function, and it can provide delay to DCLKO signal output itself. This can be used when both the following conditions are satisfied.

- The internal PLL is used to generate DCLKO (CKS field of DCM register = 0)
- The frequency division ratio to the internal PLL of DCLKO is 2 or more (SC field of DCM register > 0)

The delay value is set as the unit for internal PLL clock by DCKD field of DCM3 register. The meanings of DCKD setting value are shown below.

When the internal PLL frequency division ratio = 2

DCKD	Delay
000000	No additional delay
000100	+1 PLL clock

When the internal PLL frequency division ratio > 2

DCKD	Delay
000000	No additional delay
000010	+2 PLL clock
000100	+3 PLL clock
000110	+4 PLL clock
:	:
111110	+17 PLL clock

In delay mode, t_{dcyc_f} and t_{dcyc_l} are defined by the delay value above (e.g. "2" of "+2 PLL clock") as shown below.

t_{dcyc_f} = Delay value × t_{pllcyc}

$t_{dcyc\_l} = t_{dcyc} - t_{dcyc\_f}$

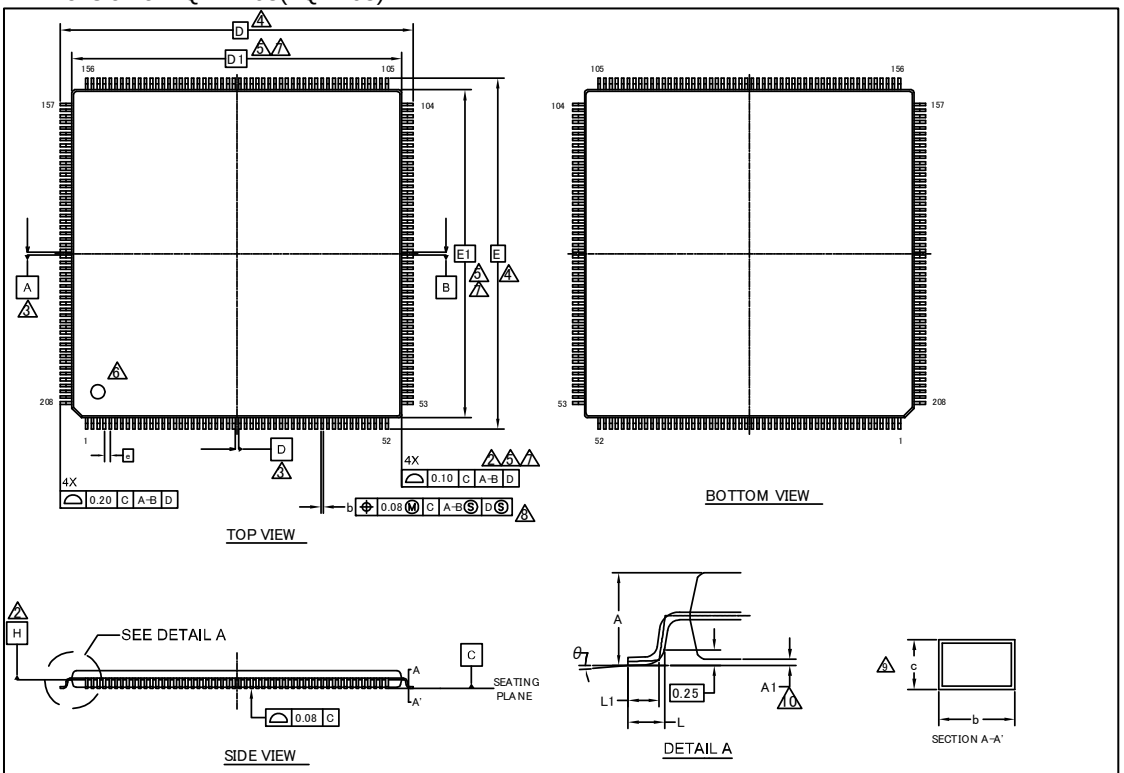
12. Ordering Information

Part Number	Package[*1]
MB91F591BPMC-GSE1	208-pin plastic LQFP (LQR208)
MB91F591BSPMC-GSE1	
MB91F591BHPMC-GSE1	
MB91F591BHSPMC-GSE1	
MB91F592BPMC-GSE1	
MB91F592BSPMC-GSE1	
MB91F592BHPMC-GSE1	
MB91F592BHSPMC-GSE1	
MB91F594BPMC-GSE1	
MB91F594BSPMC-GSE1	
MB91F594BHPMC-GSE1	
MB91F594BHSPMC-GSE1	
MB91F59BCEQ-GSE1	208-pin plastic TEQFP (LET208)
MB91F59BCHSEQ-GSE1	
MB91F59ACPB-GSE1	320-Ball Grid Array Package (BYA320)
MB91F59ACSPB-GSE1	
MB91F59ACHPB-GSE1	
MB91F59ACHSPB-GSE1	
MB91F59BCPB-GSE1	
MB91F59BCSPB-GSE1	
MB91F59BCHPB-GSE1	
MB91F59BCHSPB-GSE1	

[*1]: For details of the package, see "Package Dimensions ".

13. Package Dimensions

■Dimension of LQFP-208(LQR208)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.70
A1	0.05	—	0.15
b	0.17	0.22	0.27
c	0.09	—	0.20
D	30.00 BSC		
D1	28.00 BSC		
e	0.50 BSC		
E	30.00 BSC		
E1	28.00 BSC		
L	0.45	0.60	0.75
L1	0.30	0.50	0.70
θ	0°	—	8°

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DATUM PLANE H IS LOCATED AT THE BOTTOM OF THE MOLD PARTING LINE COINCIDENT WITH WHERE THE LEAD EXITS THE BODY.
3. DATUMS A-B AND D TO BE DETERMINED AT DATUM PLANE H.
4. TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PRE SIDE. DIMENSIONS D1 AND E1 INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
6. DETAILS OF PIN 1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.
7. REGARDLESS OF THE RELATIVE SIZE OF THE UPPER AND LOWER BODY SECTIONS. DIMENSIONS D1 AND E1 ARE DETERMINED AT THE LARGEST FEATURE OF THE BODY EXCLUSIVE OF MOLD FLASH AND GATE BURRS. BUT INCLUDING ANY MISMATCH BETWEEN THE UPPER AND LOWER SECTIONS OF THE MOLDER BODY.
8. DIMENSION b DOES NOT INCLUDE DAMBER PROTRUSION. THE DAMBAR PROTRUSION (S) SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED b MAXIMUM BY MORE THAN 0.08mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE LEAD FOOT.
9. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
10. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.

002-15151 **

PACKAGE OUTLINE, 208 LEAD LQFP
28.0X28.0X1.7 MM LQR208 REV**

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