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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	1.0625MB (1.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	872K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	208-LQFP
Supplier Device Package	208-LQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f594bspmc-gsk5e1

MB91590 Series

FR Family FR81S 32-Bit Microcontroller

This series is Cypress 32-bit microcontroller designed for automotive and industrial control applications. It contains the FR81S CPU that is compatible with the FR family. The FR81S has a high level performance among the Cypress FR family by enhancing CPU instruction pipeline and load store processing, and improving internal bus transfer.
It is best suited for application control for automotive.

Features

FR81S CPU Core

- 32-bit RISC, load/store architecture, pipeline 5-stage structure
- Maximum operating frequency:

  128 MHz (Source oscillation = 4.0 MHz and 32 multiplied (PLL clock multiplication system))

  It shows maximum CPU frequency of series. The specification of each part number can be referred in “Product Lineup” and “Electrical Characteristics.”
- General-purpose register : 32 bits ×16 sets
- 16-bit fixed length instructions (basic instruction), 1 instruction per cycle
- Instructions appropriate to embedded applications
  - Memory-to-memory transfer instruction
  - Bit processing instruction
  - Barrel shift instruction etc.
- High-level language support instructions
  - Function entry/exit instructions
  - Register content multi-load and store instructions
- Bit search instructions
  - Logical 1 detection, 0 detection, and change-point detection
- Branch instructions with delay slot
  - Reduced overhead during branch process
- Register interlock function
  - Easy assembler writing
- The support at the built-in / instruction level of the multiplier
  - Signed 32-bit multiplication : 5 cycles
  - Signed 16-bit multiplication : 3 cycles
- Interrupt (PC/PS saving)
  - 6 cycles (16 priority levels)
- The Harvard architecture allows simultaneous execution of program and data access.
- Instruction compatibility with the FR Family
- Built-in memory protection function (MPU)
  - Eight protection areas can be specified commonly for instructions and the data.
  - Control access privilege in both privilege mode and user mode.
- Built-in FPU (floating point arithmetic)
  - IEEE754 compliant
  - Floating-point register 32-bit × 16 sets

Peripheral Functions

- Clock generation (equipped with SSCG function)
  - Main oscillation (4MHz)
  - Sub oscillation (32kHz) or none sub oscillation
  - PLL multiplication rate : 1 to 32 times
- Built-in Program flash memory capacity 2048 + 64KB (series maximum)
- Built-in Data flash memory capacity(WorkFlash) 64KB
- Built-in RAM capacity
  - Main RAM 192KB (Series maximum)
  - Sub RAM (on AHB) 64KB (Series maximum)
  - Backup RAM 8KB
- General-purpose ports (5V Pin) : 63
  (dual clock products : 61)
  - Included I^2C pseudo open drain support ports : 4
- General-purpose ports (3V Pin) : 93
  - Included 48 combined external bus interface (For GDC external memory I/F)
- External bus interface
  - GDC external memory for I/F use
  - 25-bit address, 16-bit data
  - Power supply voltage fixed to 3.3V
- DMA Controller
  - Up to 16 channels can be started simultaneously.
  - 2 transfer factors (Internal peripheral request and software)
- A/D converter (successive approximation type)
  - 8/10-bit resolution : 32 channels
  - Conversion time : 3µs
- External interrupt input: 16 channels
  - Level ("H" / "L"), or edge detection (rising or falling) enabled
- LIN-UART
  - 6 channels, ch.2 to ch.7
  - UART, synchronous mode, LIN-UART mode is selectable.
  - LIN protocol Revision 2.1 is supported
  - SPI (Serial Peripheral Interface) supported (synchronous mode)
  - Full-duplex double buffering system
  - LIN synch break detection (linked to the input capture)
  - Built-in dedicated baud rate generator
  - DMA transfer support

Item \ Product		MB91F592B /BS	MB91F592BH /BHS	MB91F594B /BS	MB91F594BH /BHS
CPU core		FR81S			
Technology		90nm			
Package		LQFP208			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		80MHz			
Maximum GDC operating frequency		81MHz			
Built-in CR oscillator		100kHz			
System clock		On chip PLL			
Flash	Main	576KB		1088KB	
	Work	64KB			
RAM	Main	40KB		64KB	
	Backup	8KB			
VRAM		800KB			
Watchdog timer		1ch Hardware 1ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16ch			
CAN		1ch (64msg) 2ch (32msg)			
LIN-UART		6ch			
Multi-function Serial Interface		2ch			
A/D converter (8bit/10bit)		1unit/32ch			
Reload timer(16bit)		4ch			
Base timer(16bit)		2ch			
Free-run timer(32bit)		2ch			
Input capture(32bit)		6ch			
Output compare(32bit)		4ch			
PPG timer(16bit)		24ch			
Sound generator		5ch			
Real-time clock		Yes			
External interrupt		16ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature		-40°C to +105°C			
Allowable power [mW]		1250			
Others		Flash product			
On chip debugger		Yes			

Item \ Product		MB91F59AC /F59ACS	MB91F59ACH /F59ACHS	MB91F59BC /F59BCS	MB91F59BCH /F59BCHS
CPU core		FR81S			
Technology		90nm			
Package		BGA320/TEQFP-208*1			
Sub clock		Yes (Non-S series) No (S series)			
Maximum CPU operating frequency		128MHz			
Maximum GDC operating frequency		81MHz			
Built-in CR oscillator		100kHz			
System clock		On chip PLL			
Flash	Main	1600KB		2112KB	
	Work*2	64KB			
RAM	Main	192KB			
	Sub on AHB	64KB			
	Backup	8KB			
VRAM		1792KB			
Watchdog timer		1ch Hardware 1ch Software			
Clock supervisor		Initial value "ON"	Initial value "OFF"	Initial value "ON"	Initial value "OFF"
Low-voltage detection reset (External low-voltage detection)		Yes			
Low-voltage detection reset (Internal low-voltage detection)		Yes			
NMI function		Yes			
DMA Controller		16ch			
CAN		1ch (64msg) 2ch (32msg)			
LIN-UART		6ch			
Multi-function Serial Interface		6ch*3			
High Speed SPI (GDC)		Yes			
A/D converter (8bit/10bit)		1unit/32ch			
Up/down counter(16bit)		3ch			
Reload timer(16bit)		8ch			
Base timer(16bit)		2ch			
Free-run timer(32bit)		8ch			
Input capture(32bit)		12ch			
Output compare(32bit)		4ch			
PPG timer(16bit)		24ch			
Sound generator		5ch			
Real-time clock		Yes			
External interrupt		16ch			
CR/SUB compensation function		Yes			
CRC generation		Yes			
Stepping motor control		6ch			
Stop mode (including power shut-off)		Supported			
Power supply voltage		MICOM:4.5V to 5.5V GDC:3.0V to 3.6V			
Operating temperature		-40°C to +105°C			
Allowable power [mW]		2500			
Others		Flash product			
JTAG Boundary Scan Test		Yes (Only support BGA package products)			
On chip debugger		Yes			

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
121	P107	–	C	General-purpose I/O port
	SGO4_1	–		Sound generator ch.4 SGO output pin
	AN7	–		ADC Analog 7 input pin
	PPG5_1	–		PPG ch.5 output pin (1)
	TOT7_1	–		Reload timer ch.7 output pin (1) (MB91F59A/B only)
	ICU11_1	–		Input capture ch.11 input pin (1) (MB91F59A/B only)
101	P110	–	C	General-purpose I/O port
	TX1	–		CAN transmission data1 output pin
	PPG1_2	–		PPG ch.1 output pin (2)
	FRCK5	–		Free-run timer 5 clock input pin(MB91F59A/B only)
	TOT8_1	–		Reload timer ch.8 output pin (1) (MB91F59A/B only)
102	P111	–	C	General-purpose I/O port
	RX1	–		CAN reception data 1 input pin
	INT10	–		INT10 External interrupt input pin
	PPG2_2	–		PPG ch.2 output pin (2)
	FRCK6	–		Free-run timer 6 clock input pin(MB91F59A/B only)
	TOT9_1	–		Reload timer ch.9 output pin (1) (MB91F59A/B only)
158	P112	–	C	General-purpose I/O port
	TX2	–		CAN transmission data 2 output pin
	PPG3_2	–		PPG ch.3 output pin (2)
	TOT10_1	–		Reload timer ch.10 output pin (1) (MB91F59A/B only)
159	P113	–	C	General-purpose I/O port
	RX2	–		CAN reception data 2 input pin
	INT11	–		INT11 External interrupt input pin
	PPG4_2	–		PPG ch.4 output pin (2)
	TIN7	–		Reload timer ch.7 event input pin(MB91F59A/B only)
162	P114	–	C	General-purpose I/O port
	SGA2	–		Sound generator ch.2 SGA output pin
	SCK3	–		LIN-UART ch.3 clock I/O pin
	TRG3	–		PPG trigger 3 input pin (ch.12 to ch.15)
	TIN1	–		Reload timer ch.1 event input pin
	ICU5_1	–		Input capture ch.5 input pin (1)
	FRCK7	–		Free-run timer 7 clock input pin(MB91F59A/B only)
163	P115	–	C	General-purpose I/O port
	SGO2	–		Sound generator ch.2 SGO output pin
	SIN4	–		LIN-UART ch.4 serial data input pin
	TIN2	–		Reload timer ch.2 event input pin
	FRCK4	–		Free-run timer 4 clock input pin(MB91F59A/B only)
164	P116	–	C	General-purpose I/O port
	SGA3	–		Sound generator ch.3 SGA output pin
	SOT4	–		LIN-UART ch.4 serial data output pin
	TIN3	–		Reload timer ch.3 event input pin
	FRCK3	–		Free-run timer 3 clock input pin(MB91F59A/B only)
165	P117	–	C	General-purpose I/O port
	SGO3	–		Sound generator ch.3 SGO output pin
	SCK4	–		LIN-UART ch.4 clock I/O pin
	TRG4	–		PPG trigger 4 input pin (ch.16 to ch.19)
	TOT0	–		Reload timer ch.0 output pin
	FRCK2	–		Free-run timer 2 clock input pin(MB91F59A/B only)

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
166	P120	–	C	General-purpose I/O port
	FRCK1	–		Free-run timer 1 clock input pin
	SIN5	–		LIN-UART ch.5 serial data input pin
	INT6	–		INT6 External interrupt input pin
	TOT1	–		Reload timer ch.1 output pin
	PPG5_2	–		PPG ch.5 output pin (2)
167	P121	–	C	General-purpose I/O port
	FRCK0	–		Free-run timer 0 clock input pin
	SOT5	–		LIN-UART ch.5 serial data output pin
	INT7	–		INT7 External interrupt input pin
	TOT2	–		Reload timer ch.2 output pin
	PPG6_2	–		PPG ch.6 output pin (2)
168	P122	–	C	General-purpose I/O port
	OCU0	–		Output compare ch.0 output pin
	SCK5	–		LIN-UART ch.5 clock I/O pin
	TOT3	–		Reload timer ch.3 output pin
	PPG7_2	–		PPG ch.7 output pin (2)
108	P123	–	A	General-purpose I/O port
	OCU1	–		Output compare ch.1 output pin
	PPG8_2	–		PPG ch.8 output pin (2)
	TIN8	–		Reload timer ch.8 event input pin(MB91F59A/B only)
	SIN11	–		Multi-function serial ch.11 serial data input pin(MB91F59A/B only)
109	P124	–	A	General-purpose I/O port
	OCU2	–		Output compare ch.2 output pin
	ICU5_2	–		Input capture ch.5 input pin (2)
	PPG9_2	–		PPG ch.9 output pin (2)
	TIN9	–		Reload timer ch.9 event input pin(MB91F59A/B only)
	SOT11	–		Multi-function serial ch.11 serial data output pin(MB91F59A/B only)
110	P125	–	A	General-purpose I/O port
	OCU3	–		Output compare ch.3 output pin
	ICU0	–		Input capture ch.0 input pin
	PPG10_2	–		PPG ch.10 output pin (2)
	TIN10	–		Reload timer ch.10 event input pin(MB91F59A/B only)
	SCK11	–		Multi-function serial ch.11 clock I/O pin(MB91F59A/B only)
90	P126	–	A	General-purpose I/O port
	TRG0	–		PPG trigger 0 input pin (ch.0 to ch.3)
	SIN0	–		Multi-function serial ch.0 serial data input pin
	INT1	–		INT1 External interrupt input pin
91	P127	–	K	General-purpose I/O port
	SOT0	–		Multi-function serial ch.0 serial data output pin / I^2C ch.0 serial data I/O pin
92	P130	–	K	General-purpose I/O port
	SCK0	–		Multi-function serial ch.0 clock I/O pin / I^2C ch.0 clock I/O pin
	INT0	–		INT0 External interrupt input pin
	ICU1	–		Input capture ch.1 input pin
	TIOA0	–		Base timer TIOA0 output pin

BGA Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
136	D0	–	O	External bus · Data bit0 I/O pin
136	P000	–	O	General-purpose I/O port (3V pin)
	SIN2_1			LIN-UART ch.2 serial data input pin (1)
	PPG0			PPG ch.0 output pin
	TIN0_2			Reload timer ch.0 event input pin (2)
137	VSYNC	–	O	Display vertical sync signal output pin (for Internal sync)/ Display vertical sync signal input pin (for External sync)
	PG5			General-purpose I/O port (3V pin)
138	BOUT7	–	O	Display digital B7 output pin
	PF7			General-purpose I/O port(3V pin)
139	BOUT5	–	O	Display digital B5 output pin
	PF5			General-purpose I/O port (3V pin)
140	BOUT3	–	O	Display digital B3 output pin
	PF3			General-purpose I/O port (3V pin)
141	GOUT6	–	O	Display digital G6 output pin
	PE6			General-purpose I/O port (3V pin)
142	GOUT3	–	O	Display digital G3 output pin
	PE3			General-purpose I/O port (3V pin)
143	ROUT6	–	O	Display digital R6 output pin
	PD6			General-purpose I/O port (3V pin)
144	ROUT3	–	O	Display digital R3 output pin
	PD3			General-purpose I/O port (3V pin)
145	VSS	–	–	GND pin
146	DCKIN	–	O	Display reference clock input pin (for External sync)
	CMDTRG			GDC command trigger input pin
	PG0			General-purpose I/O port (3V pin)
147	CSOUT	–	O	Display composite sync signal output pin, Graphics / Video switch (for External sync) output pin
	PG3			General-purpose I/O port (3V pin)
148	HSIN	P	O	Capture horizontal sync signal input pin
	PG2	–		General-purpose I/O port (3V pin)
149	BIN7	–	O	Capture B7 input pin (RGB mode)
	PC7			General-purpose I/O port (3V pin)
150	BIN4	–	O	Capture B4 input pin (RGB mode)
	PC4			General-purpose I/O port (3V pin)
151	GIN7	–	O	Capture G7 input pin (RGB mode)
	PB7			General-purpose I/O port (3V pin)
152	GIN4	–	O	Capture G4 input pin (RGB mode)
	PB4			General-purpose I/O port (3V pin)
153	RIN7	–	O	Capture R7 input pin (RGB mode)
	VIN5			Capture VIN5 input pin (656 mode)
	PA7			General-purpose I/O port (3V pin)
154	RIN4	–	O	Capture R4 input pin (RGB mode)
	VIN2			Capture VIN2 input pin (656 mode)
	PA4			General-purpose I/O port (3V pin)
155	FRCK0	–	C	Free-run timer 0 clock input pin
	P121			General-purpose I/O port
	INT7			INT7 External interrupt input pin

■Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:

1. Maintain relative humidity in the working environment between 40% and 70%. Use of an apparatus for ion generation may be needed to remove electricity.
2. Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
3. Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of 1 MΩ).
   Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
4. Ground all fixtures and instruments, or protect with anti-static measures.
5. Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

5.3 Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above.

For reliable performance, do the following:

1. Humidity

   Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
2. Discharge of Static Electricity

   When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
3. Corrosive Gases, Dust, or Oil

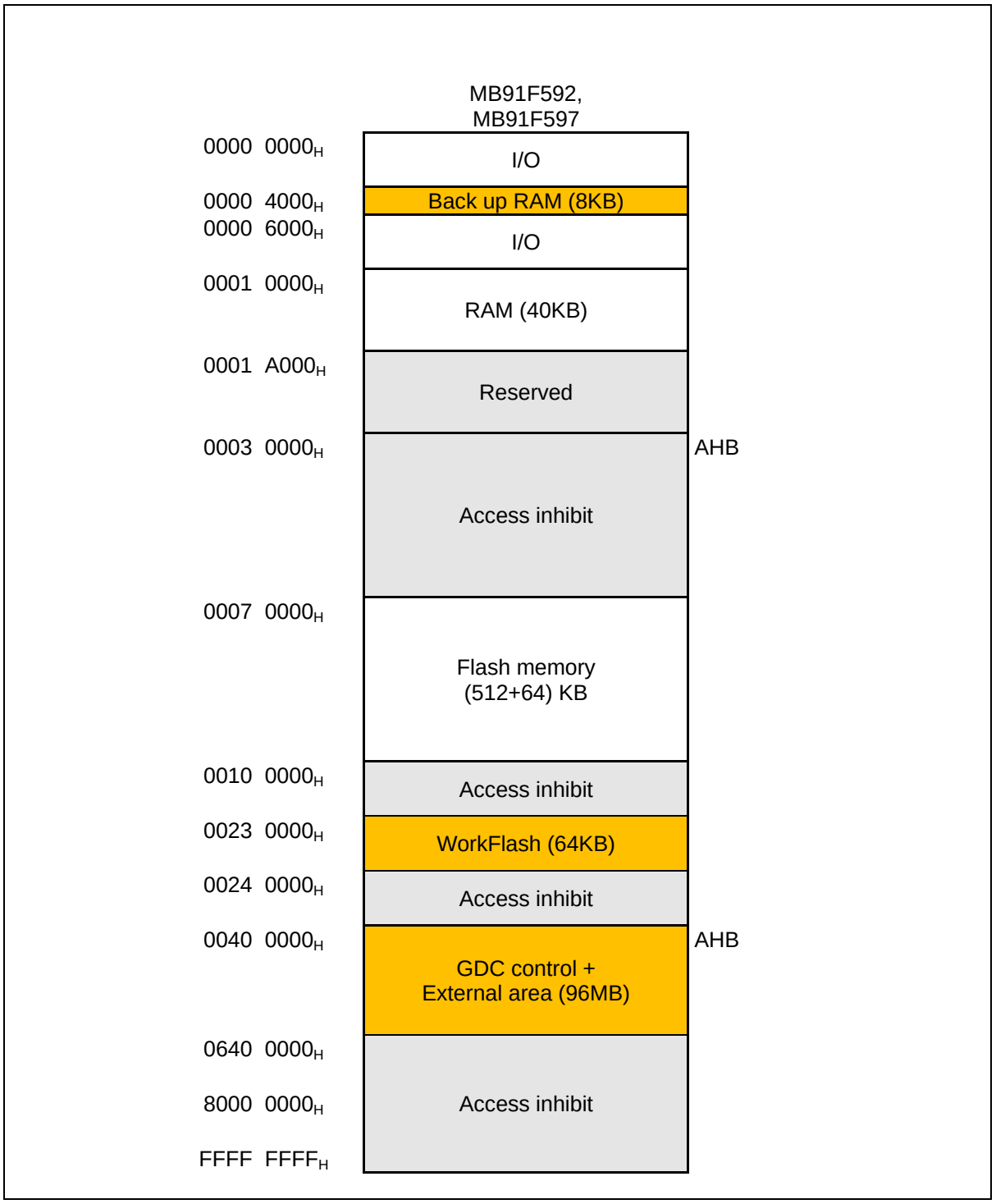
   Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
4. Radiation, Including Cosmic Radiation

   Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
5. Smoke, Flame

CAUTION: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.

Customers considering the use of Cypress products in other special environmental conditions should consult with sales representatives.

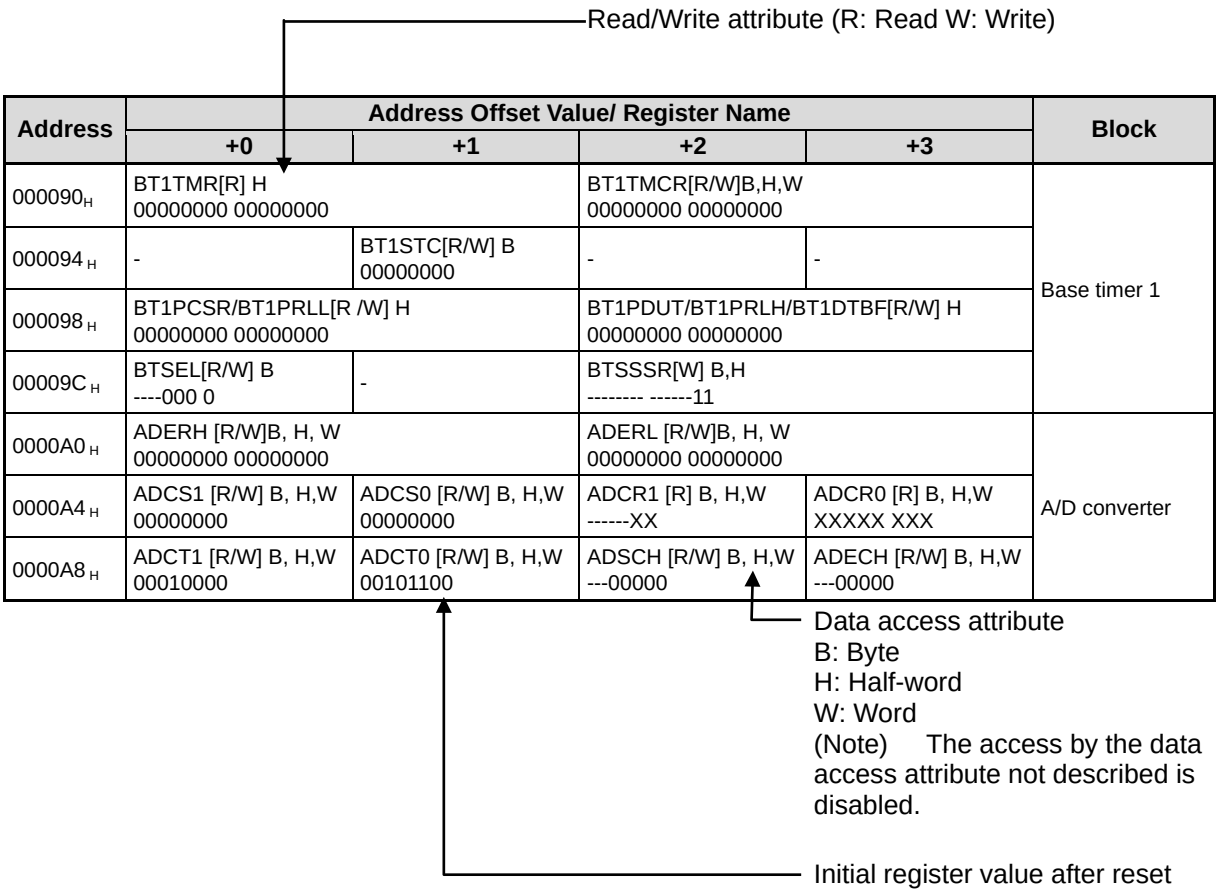
■Memory map


MB91F592,
MB91F597
0000 0000H
I/O
0000 4000H
Back up RAM (8KB)
0000 6000H
I/O
0001 0000H
RAM (40KB)
0001 A000H
Reserved
0003 0000H
AHB
Access inhibit
0007 0000H
Flash memory
(512+64) KB
0010 0000H
Access inhibit
0023 0000H
WorkFlash (64KB)
0024 0000H
Access inhibit
0040 0000H
AHB
GDC control +
External area (96MB)
0640 0000H
Access inhibit
8000 0000H
FFFF FFFFH

9. I/O Map

The following I/O map shows the relationship between memory space and registers for peripheral resources.

■Legend of I/O Map



Address	Address Offset Value/ Register Name				Block
	+0	+1	+2	+3	
000090 H	BT1TMR[R] H 00000000 00000000		BT1TMCR[R/W]B,H,W 00000000 00000000		Base timer 1
000094 H	-	BT1STC[R/W] B 00000000	-	-	
000098 H	BT1PCSR/BT1PRLL[R /W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF[R/W] H 00000000 00000000		
00009C H	BTSEL[R/W] B ----000 0	-	BTSSSR[W] B,H -------- ------11		
0000A0 H	ADERH [R/W]B, H, W 00000000 00000000		ADERL [R/W]B, H, W 00000000 00000000		A/D converter
0000A4 H	ADCS1 [R/W] B, H,W 00000000	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXX XXX	
0000A8 H	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	

The initial register value after reset indicates as follows:

- "1": Initial value "1"
- "0": Initial value "0"
- "X": Initial value undefined
- "-": Reserved bit/Undefined bit
- "*": Initial value "0" or "1" according to the setting

Note: The access by the data access attribute not described is disabled.

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000E00_H$	DDR00[R/W] B,H,W 00000000	DDR01[R/W] B,H,W 00000000	DDR02[R/W] B,H,W 00000000	DDR03[R/W] B,H,W 00000000	Data direction register
$000E04_H$	DDR04[R/W] B,H,W 00000000	DDR05[R/W] B,H,W 00000000	DDR06[R/W] B,H,W 00000000	DDR07[R/W] B,H,W 00000000	
$000E08_H$	DDR08[R/W] B,H,W 00000000	DDR09[R/W] B,H,W 00000000	DDR10[R/W] B,H,W 00000000	DDR11[R/W] B,H,W 00000000	
$000E0C_H$	DDR12[R/W] B,H,W 00000000	DDR13[R/W] B,H,W 00-00000	—	—	
$000E10_H$	DDRA[R/W] B,H,W 000000--	DDRB[R/W] B,H,W 000000--	DDRC[R/W] B,H,W 000000--	DDRD[R/W] B,H,W 000000--	
$000E14_H$	DDRE[R/W] B,H,W 000000--	DDRF[R/W] B,H,W 000000--	DDRG[R/W] B,H,W 00000000	DDRH[R/W] B,H,W ----0---	
$000E18_H$ to $000E1C_H$	—	—	—	—	Reserved
$000E20_H$	PFR00[R/W] B,H,W 00000000	PFR01[R/W] B,H,W 00000000	PFR02[R/W] B,H,W 00000000	PFR03[R/W] B,H,W 00000000	Port function register
$000E24_H$	PFR04[R/W] B,H,W 00000000	PFR05[R/W] B,H,W -0000000	PFR06[R/W] B,H,W 00000000	PFR07[R/W] B,H,W 00000000	
$000E28_H$	PFR08[R/W] B,H,W 00000000	PFR09[R/W] B,H,W 0-000000	PFR10[R/W] B,H,W 00000000	PFR11[R/W] B,H,W 00000000	
$000E2C_H$	PFR12[R/W] B,H,W 0-000000	PFR13[R/W] B,H,W ---00000	—	—	
$000E30_H$	PFRA[R/W] B,H,W --------	PFRB[R/W] B,H,W --------	PFRC[R/W] B,H,W --------	PFRD[R/W] B,H,W 000000--	
$000E34_H$	PFRE[R/W] B,H,W 000000--	PFRF[R/W] B,H,W 000000--	PFRG[R/W] B,H,W 00000---	PFRH[R/W] B,H,W --------	
$000E38_H$ to $000E3C_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
002500_H	SEEARH[R] B,H,W --000000 00000000		DEEARH[R] B,H,W --000000 00000000		AHB RAM ECC control register MB91F59A/B only
002504_H	EECSRH[R/W] B,H,W ----0000	—	EFEARH[R/W]B,H,W --000000 00000000		
002508_H	—	EFECRH[R/W]B,H,W -------0 00000000 00000000			
$00250C_H$ to $002FFC_H$	—	—	—	—	Reserved
003000_H	SEEARA[R] B,H,W -----000 00000000		DEEARA[R] B,H,W -----000 00000000		Backup RAM ECC control register
003004_H	EECSRA [R/W] B,H,W ----0000	—	EFEARA[R/W] B,H,W -----000 00000000		
003008_H	—	EFECRA[R/W] B,H,W -------0 00000000 00000000			
$00300C_H$ to $003FFC_H$	—	—	—	—	Reserved
004000_H to $005FFC_H$	Backup RAM				Backup RAM area
006000_H to $00EFFC_H$	—	—	—	—	Reserved
$00F000_H$ to $00FEFC_H$	—	—	—	—	Reserved [S]
$00FF00_H$	DSUCR [R/W] B,H,W -------- -------0		—	—	OCDU [S]
$00FF04_H$ to $00FF0C_H$	—	—	—	—	Reserved [S]
$00FF10_H$	PCSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FF14_H$	PSSR [R/W] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
$00FF18_H$ to $00FFF4_H$	—	—	—	—	Reserved [S]
$00FFF8_H$	EDIR1 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				OCDU [S]
$00FFFC_H$	EDIR0 [R] B,H,W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

[S]:It is a system register. The illegal instruction exception (data access error) is generated in these registers in the user mode when reading and writing to it.

11. Electrical Characteristics

11.1 Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit	Remarks
		Min	Max		
Power supply voltage[*1,*2]	$V_{CC}5$	Vss-0.3	Vss+6.0	V	
	$V_{CC}3$	Vss-0.3	Vss+4.0	V	Vcc3 ≤ Vcc5
	DV_{CC}	Vss-0.3	Vss+6.0	V	DVcc ≤ Vcc5
Analog power supply voltage[*1,*2]	$AV_{CC}5$	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5 ≤ Vcc5
	$AV_{CC}3$	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3 ≤ Vcc3
Analog reference voltage[*1]	AVRH5	Vss-0.3	Vss+6.0	V	AVRH5 ≤ AVcc5
	AVR3	Vss-0.3	Vss+4.0	V	AVR3 ≤ AVcc3
Input voltage[*1]	V_{I1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{I2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{I3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Analog pin input voltage[*1]	$V_{IA}5$	Vss-0.3	Vcc5+0.3	V	
	$V_{IA}3$	Vss-0.3	Vcc3+0.3	V	
Output voltage[*1]	V_{O1}	Vss-0.3	Vcc5+0.3	V	5V pins other than SMC multiplied pins
	V_{O2}	Vss-0.3	Vcc3+0.3	V	3.3V dedicated pin
	V_{O3}	Vss-0.3	Vcc5+0.3	V	SMC shared pin
Maximum clamp current	I_{CLAMP}	-4	4	mA	*9
Total maximum clamp current	$\Sigma\lvert I_{CLAMP}\rvert$	–	20	mA	*9
"L" level maximum output current [*3]	I_{OL1}	–	7	mA	When setting to 2mA[*6]
	I_{OL2}	–	40	mA	When setting to 30mA[*7]
	I_{OL3}	–	30	mA	When setting to 20mA[*8]
"L" level average output current [*4]	I_{OLAV1}	–	2	mA	When setting to 2mA[*6]
	I_{OLAV2}	–	30	mA	When setting to 30mA[*7]
	I_{OLAV3}	–	20	mA	When setting to 20mA[*8]
"L" level total output current [*5]	ΣI_{OL1}	–	50	mA	*6
	ΣI_{OL2}	–	250	mA	*7
	ΣI_{OL3}	–	50	mA	*8
"H" level maximum output current [*3]	I_{OH1}	–	-7	mA	When setting to 2mA[*6]
	I_{OH2}	–	-40	mA	When setting to 30mA[*7]
	I_{OH3}	–	-30	mA	When setting to 20mA[*8]
"H" level average output current [*4]	I_{OHAV1}	–	-2	mA	When setting to 2mA[*6]
	I_{OHAV2}	–	-30	mA	When setting to 30mA[*7]
	I_{OHAV3}	–	-20	mA	When setting to 20mA[*8]
"H" level total output current [*5]	ΣI_{OH1}	–	-50	mA	*6
	ΣI_{OH2}	–	-250	mA	*7
	ΣI_{OH3}	–	-50	mA	*8
Power consumption	P_D	–	1250	mW	LQFP product
		–	2500	mW	BGA product TEQFP product HQFP product
Operating temperature	T_A	-40	+105	°C	*10
Storage temperature	Tstg	-55	+150	°C	

[*1]: These parameters are based on the condition that V_{SS}=AV_{SS}=DV_{SS}=0.0V

[*2]: Caution must be taken that $AV_{CC}5$ and DV_{CC} do not exceed $V_{CC}5$.Similarly,$AV_{CC}3$ must not exceed $V_{CC}3$.

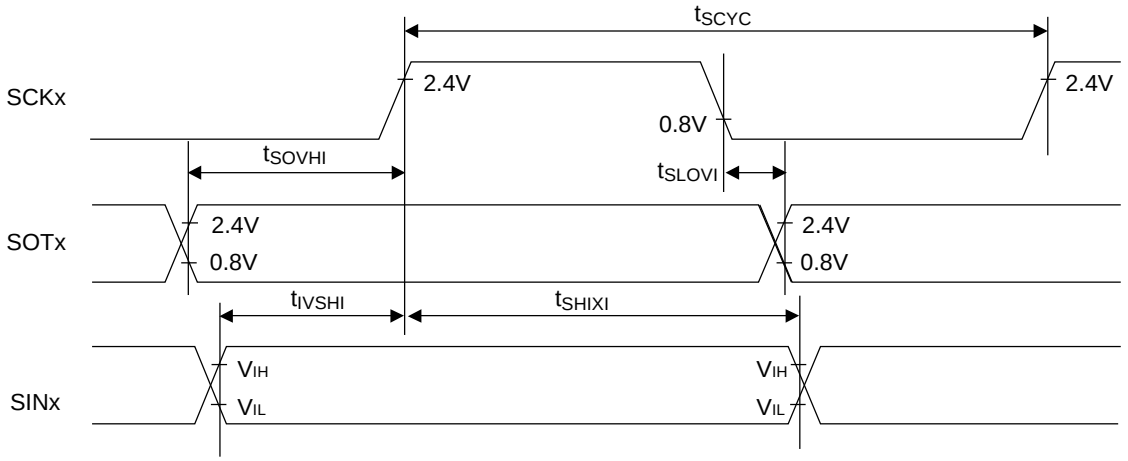
[*3]: The maximum output current is defined as the value of the peak current flowing through any one of the corresponding pins.

[*4]: The average output current is defined as the value of the average current flowing through any one of the corresponding pins for a 10 ms period. The average value is the operation current × the operation ratio.

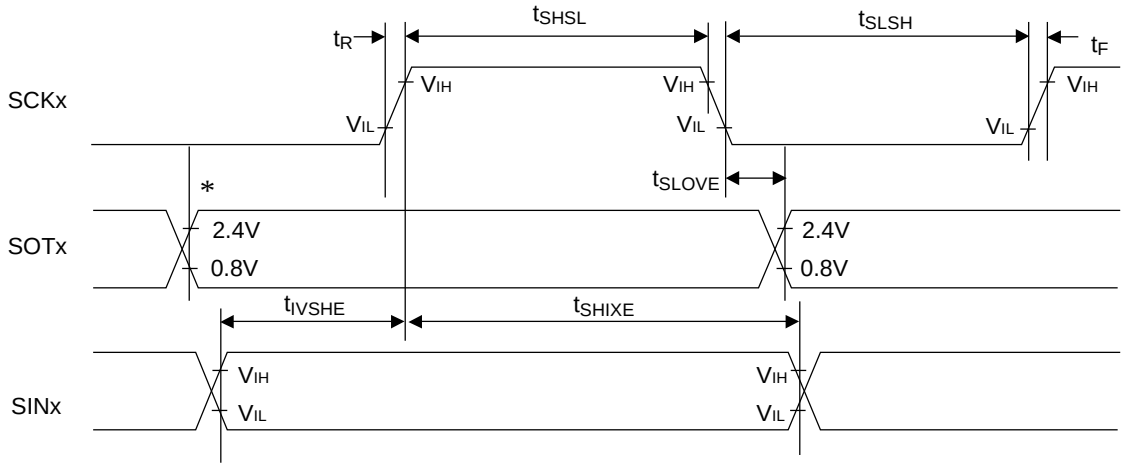
[*5]: The total output current is defined as the maximum current value flowing through all of corresponding pins.

[*6]: Outputs other than P60-P87 and 3V pin.

• **Internal Shift Clock Mode**



• **External Shift Clock Mode**



***: Changes when Writing to TDR Register**

I²C Timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		High-Speed Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0, SCK1	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK0, SCK1, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0, SCK1, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		0	3.45*2	0	0.9	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		250*3	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	2t_{CPP}*4	–	2t_{CPP}*4	–	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the peripheral clock frequency to 8MHz or more when use I²C.

11.4.1.10 Low voltage detection (Internal low-voltage detection)

(T_A: Recommended operating conditions, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply voltage range	V_{RDP5}	VCC	–	–	–	1.3	V	
Detection voltage	V_{RDL}		*	0.8	0.9	1.0	V	When power-supply voltage falls
Hysteresis width	V_{RHYS}		–	–	–	50	mV	When power-supply voltage rises
Low voltage detection time	Td	–	–	–	–	30	µs	

*: If the fluctuation of the power supply is faster than the low voltage detection time(Td), there is a possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

11.4.1.13 GDC display signal

Clock

AC timing of video interface clock signal

(T_A: Recommended operating conditions, V_{CC}3=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value		Unit	Remarks
			Min	Max		
DCLKI frequency	Fdclki0	DCLKI	–	54	MHz	
DCLKI "H"width	Thdclki0		18	–	ns	
DCLKI "L"width	Tldclki0		18	–	ns	
DCLK frequency	Tldclk0	DCLK (internal)	–	54	MHz	*1
DCLKO frequency	Fdclko0	DCLKO	–	54	MHz	*2

*1: The internal display clock of PLL synchronous mode is generated with internal PLL of display clock prescaler.

*2: DCLKI or PLL internal display clock is output.

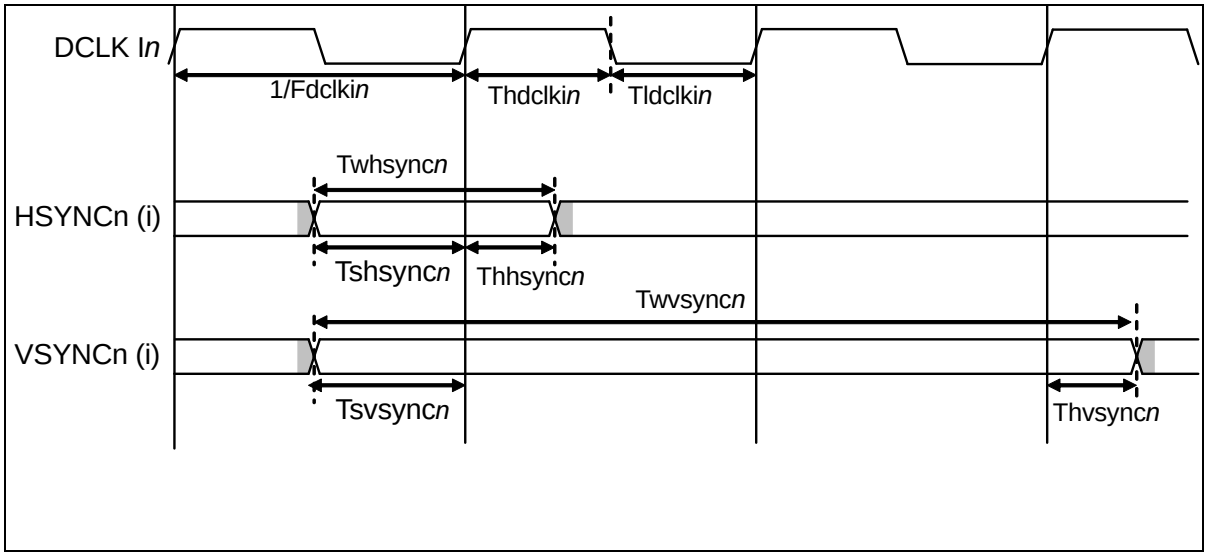
Apply only DCLKI synchronous mode. (reference clock= DCLKI)

- AC timing of video interface input signal

(T_A: Recommended operating conditions, V_{CC}3=3.3V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
HSYNC input setup time	Tshsync0	HSYNC(i)	4	–	–	ns	
HSYNC input hold time	Thhsync0		1	–	–	ns	
VSYNC input pulse width	Twvsync0	VSYNC(i)	1	–	–	HSYNC	

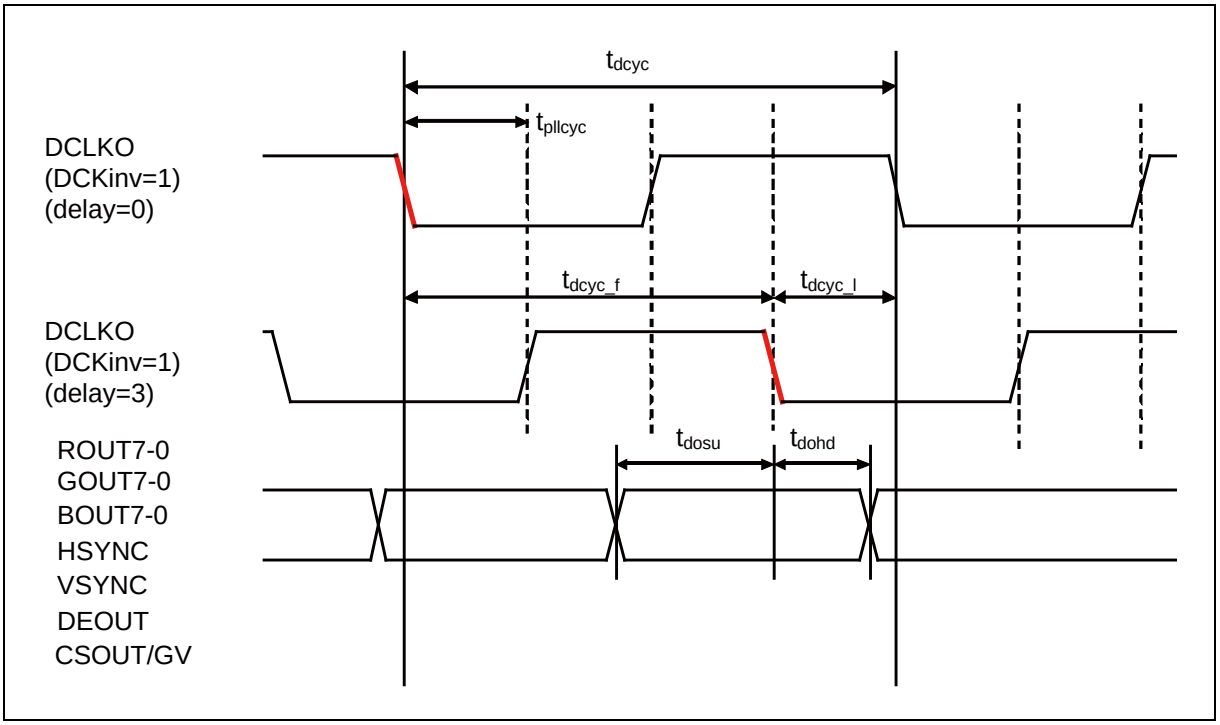
■Display input signal timing



Built-in PLL reverse edge and delay mode (DCM3.DCKinv=1)

Figure 6 shows the setup/hold definition when the external display device receives the signal at the falling edge of DCLKO. (Example: When frequency division ratio = 4)

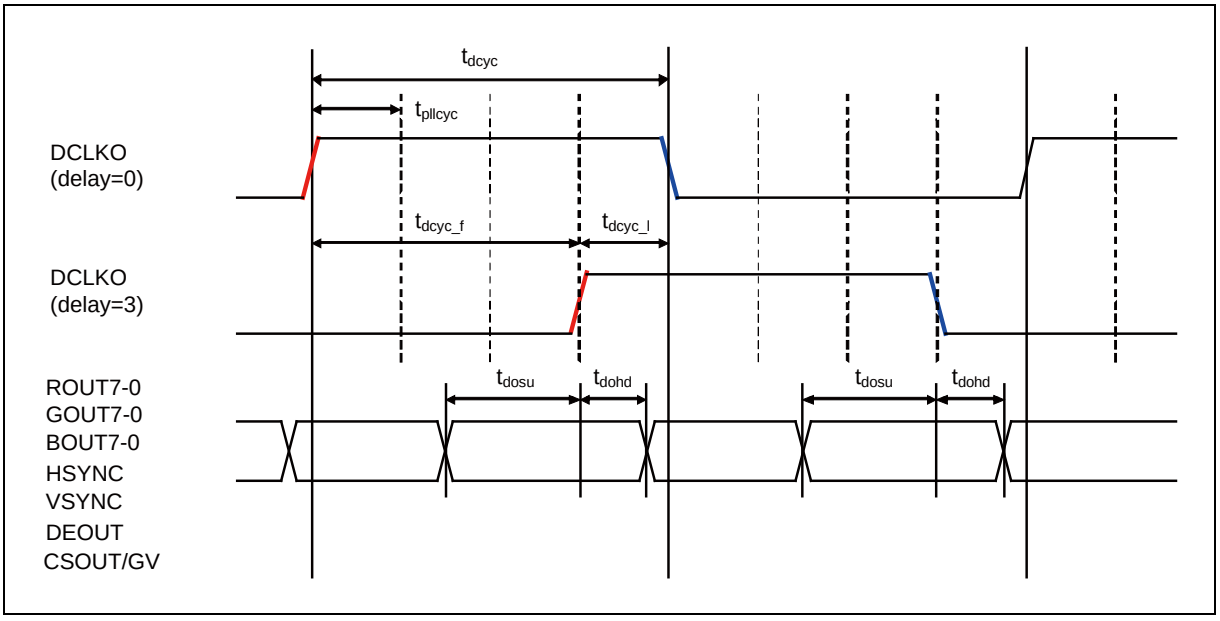
Figure 6. Built-in PLL Reverse Edge and Delay Mode Setup/Hold Definition



Built-in PLL both edge and delay mode (DCM3.DCKinv=0)

Figure 7 shows the setup/hold definition when the external display device (TFT) receives the signal both at the rising edge and the falling edge of DCLKO. (Example: When frequency division ratio = 4) Although there are two sampling locations in both edge mode; one at the rising edge and the other at the falling edge, the values of setup/hold definition are same.

Figure 7. Built-in PLL Both Edge and Delay Mode Setup/Hold Definition



11.5 A/D Converter

11.5.1 Electrical Characteristics

(T_A: Recommended operating conditions, $V_{CC}5$=$AV_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	–	–	–	–	10	bit	
Total error	–	–	–	–	±3	LSB	
Non linearity error	–	–	–	–	±2.5	LSB	
Differential linearity error	–	–	–	–	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN31	AV_{SS} - 1.5LSB	–	AV_{SS} + 2.5LSB	V	1LSB = (AV_{CC} - AV_{SS}) /1024
Full-scale transition voltage	V_{FST}	AN0 to AN31	AVRH5 - 3.5LSB	–	AVRH5 + 0.5LSB	V	
Sampling time	t_{SMP}	–	1.2	–	–	µs	*1
Compare time	t_{CMP}	–	1.8	–	–	µs	*1
A/D conversion time	t_{CNV}	–	3.0	–	–	µs	*1
Analog port input current	I_{AIN}	AN0 to AN31	-5	–	+5	µA	$V_{AVSS} \le V_{AIN} \le V_{AVCC}$
Analog input voltage	V_{AIN}	AN0 to AN31	AV_{SS}	–	AVRH5	V	
Reference voltage	A_{VRH}	AVRH5	4.5	–	5.5	V	AVRH5 ≤ $AV_{CC}5$
	A_{VRL}	AVSS	–	0.0	–	V	
Power supply current	I_A	AVCC	–	–	4.0	mA	
	I_{AH}		–	–	6.0	µA	*2
	I_R	AVRH5	–	600	900	µA	
	I_{RH}		–	–	5	µA	*2
Variation between channels	–	AN0 to AN31	–	–	4	LSB	

*1: Time for each channel.

*2: Power supply current (V_{CC} = AV_{CC} = 5.0 V) is specified if A/D converter is not operating and CPU is stopped.

Note:
Be sure to use the clock with a frequency between 8MHz and 17MHz for the ADC compare clock in order to ensure its accuracy.

12. Ordering Information

Part Number	Package[*1]
MB91F591BPMC-GSE1	208-pin plastic LQFP (LQR208)
MB91F591BSPMC-GSE1	
MB91F591BHPMC-GSE1	
MB91F591BHSPMC-GSE1	
MB91F592BPMC-GSE1	
MB91F592BSPMC-GSE1	
MB91F592BHPMC-GSE1	
MB91F592BHSPMC-GSE1	
MB91F594BPMC-GSE1	
MB91F594BSPMC-GSE1	
MB91F594BHPMC-GSE1	
MB91F594BHSPMC-GSE1	
MB91F59BCEQ-GSE1	208-pin plastic TEQFP (LET208)
MB91F59BCHSEQ-GSE1	
MB91F59ACPB-GSE1	320-Ball Grid Array Package (BYA320)
MB91F59ACSPB-GSE1	
MB91F59ACHPB-GSE1	
MB91F59ACHSPB-GSE1	
MB91F59BCPB-GSE1	
MB91F59BCSPB-GSE1	
MB91F59BCHPB-GSE1	
MB91F59BCHSPB-GSE1	

[*1]: For details of the package, see "Package Dimensions ".

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