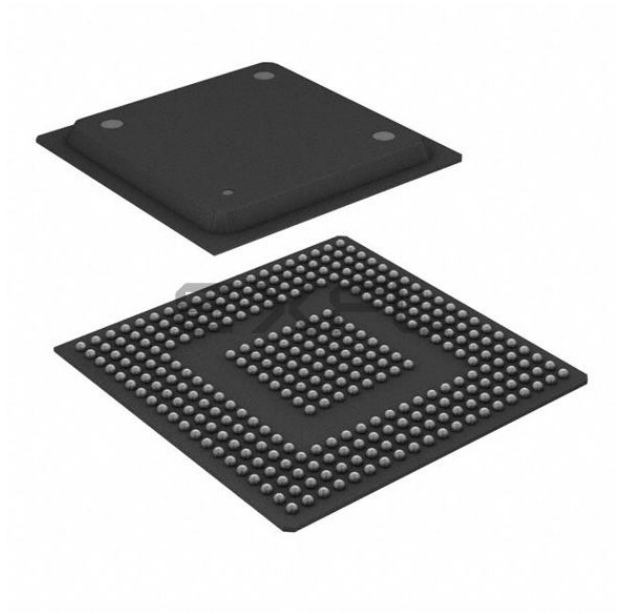


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	FR81S
Core Size	32-Bit Single-Core
Speed	128MHz
Connectivity	CANbus, CSIO, EBI/EMI, LINbus, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	156
Program Memory Size	2.0625MB (2.0625M x 8)
Program Memory Type	FLASH
EEPROM Size	64K x 8
RAM Size	2.008M x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 32x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	320-BBGA
Supplier Device Package	320-PBGA (27x27)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb91f59bcpb-gsk5e1

3. Pin Description

3.1 Pin Description of LQFP-208/TEQFP-208

Pin No.	Pin Name	Polarity	I/O Circuit Types*1	Function*2
84	X0	–	L	Main clock oscillation input pin
83	X1	–	L	Main clock oscillation output pin
171 (dual clock product)	X0A	–	N	Sub clock oscillation input pin
172 (dual clock product)	X1A	–	N	Sub clock oscillation output pin
171 (single clock product)	P137	–	A	General-purpose I/O port
172 (single clock product)	P136	–	A	General-purpose I/O port
97	NMIX	N	F1	Non-masking interrupt input pin
87	RSTX	N	F1	External reset input pin
86	MD0	–	P	Mode pin 0
85	MD1	–	P	Mode pin 1
169	MD2	–	F2	Mode pin 2
27	P000	–	O	General-purpose I/O port (3V pin)
	D0	–		External bus · Data bit0 I/O pin
	SIN2_1	–		LIN-UART ch.2 serial data input pin (1)
	TIN0_2	–		Reload timer ch.0 event input pin (2)
	PPG0	–		PPG ch.0 output pin
28	P001	–	O	General-purpose I/O port (3V pin)
	D1	–		External bus · Data bit1 I/O pin
	SOT2_1	–		LIN-UART ch.2 serial data output pin (1)
	TIN1_2	–		Reload timer ch.1 event input pin (2)
	PPG1	–		PPG ch.1 output pin
29	P002	–	O	General-purpose I/O port (3V pin)
	D2	–		External bus · Data bit2 I/O pin
	SCK2_1	–		LIN-UART ch.2 clock I/O pin (1)
	TIN2_2	–		Reload timer ch.2 event input pin (2)
	PPG2	–		PPG ch.2 output pin
30	P003	–	O	General-purpose I/O port (3V pin)
	D3	–		External bus · Data bit3 I/O pin
	SIN3_1	–		LIN-UART ch.3 serial data input pin (1)
	TIN3_2	–		Reload timer ch.3 event input pin (2)
	PPG3	–		PPG ch.3 output pin
31	P004	–	O	General-purpose I/O port (3V pin)
	D4	–		External bus · Data bit4 I/O pin
	SOT3_1	–		LIN-UART ch.3 serial data output pin (1)
	TOT0_2	–		Reload timer ch.0 output pin (2)
	PPG4	–		PPG ch.4 output pin

Pin No.	Pin Name	Polarity	I/O Circuit Types[*1]	Function[*2]
55	P030	–	O	General-purpose I/O port (3V pin)
	A02	–		External bus · Address bit2 output pin
56	P031	–	O	General-purpose I/O port (3V pin)
	A03	–		External bus · Address bit3 output pin
57	P032	–	O	General-purpose I/O port (3V pin)
	A04	–		External bus · Address bit4 output pin
58	P033	–	O	General-purpose I/O port (3V pin)
	A05	–		External bus · Address bit5 output pin
59	P034	–	O	General-purpose I/O port (3V pin)
	A06	–		External bus · Address bit6 output pin
60	P035	–	O	General-purpose I/O port (3V pin)
	A07	–		External bus · Address bit7 output pin
61	P036	–	O	General-purpose I/O port (3V pin)
	A08	–		External bus · Address bit8 output pin
62	P037	–	O	General-purpose I/O port (3V pin)
	A09	–		External bus · Address bit9 output pin
	QSPI_SIO0	–		HS_SPI SDATA0 I/O pin(MB91F59A/B only)
63	P040	–	O	General-purpose I/O port (3V pin)
	A10	–		External bus · Address bit10 output pin
	QSPI_SIO1	–		HS_SPI SDATA1 I/O pin(MB91F59A/B only)
64	P041	–	O	General-purpose I/O port (3V pin)
	A11	–		External bus · Address bit11 output pin
	QSPI_SIO2	–		HS_SPI SDATA2 I/O pin(MB91F59A/B only)
65	P042	–	O	General-purpose I/O port (3V pin)
	A12	–		External bus · Address bit12 output pin
	QSPI_SIO3	–		HS_SPI SDATA3 I/O pin(MB91F59A/B only)
66	P043	–	O	General-purpose I/O port (3V pin)
	A13	–		External bus · Address bit13 output pin
	QSPI_CS0	–		HS_SPI SSEL0 Output pin(MB91F59A/B only)
67	P044	–	O	General-purpose I/O port (3V pin)
	A14	–		External bus · Address bit14 output pin
	QSPI_CS1	–		HS_SPI SSEL1 Output pin(MB91F59A/B only)
68	P045	–	O	General-purpose I/O port (3V pin)
	A15	–		External bus · Address bit15 output pin
	QSPI_CS2	–		HS_SPI SSEL2 Output pin(MB91F59A/B only)
69	P046	–	O	General-purpose I/O port (3V pin)
	A16	–		External bus · Address bit16 output pin
	QSPI_CS3	–		HS_SPI SSEL3 Output pin(MB91F59A/B only)
70	P047	–	O	General-purpose I/O port (3V pin)
	A17	–		External bus · Address bit17 output pin
	QSPI_CLK	–		HS_SPI SCLK Output pin(MB91F59A/B only)
74	P050	–	O	General-purpose I/O port (3V pin)
	A18	–		External bus · Address bit18 output pin
75	P051	–	O	General-purpose I/O port(3V pin)
	A19	–		External bus · Address bit19 output pin
76	P052	–	O	General-purpose I/O port(3V pin)
	A20	–		External bus · Address bit20 output pin

■Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

5.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■Lead-Free Packaging
CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

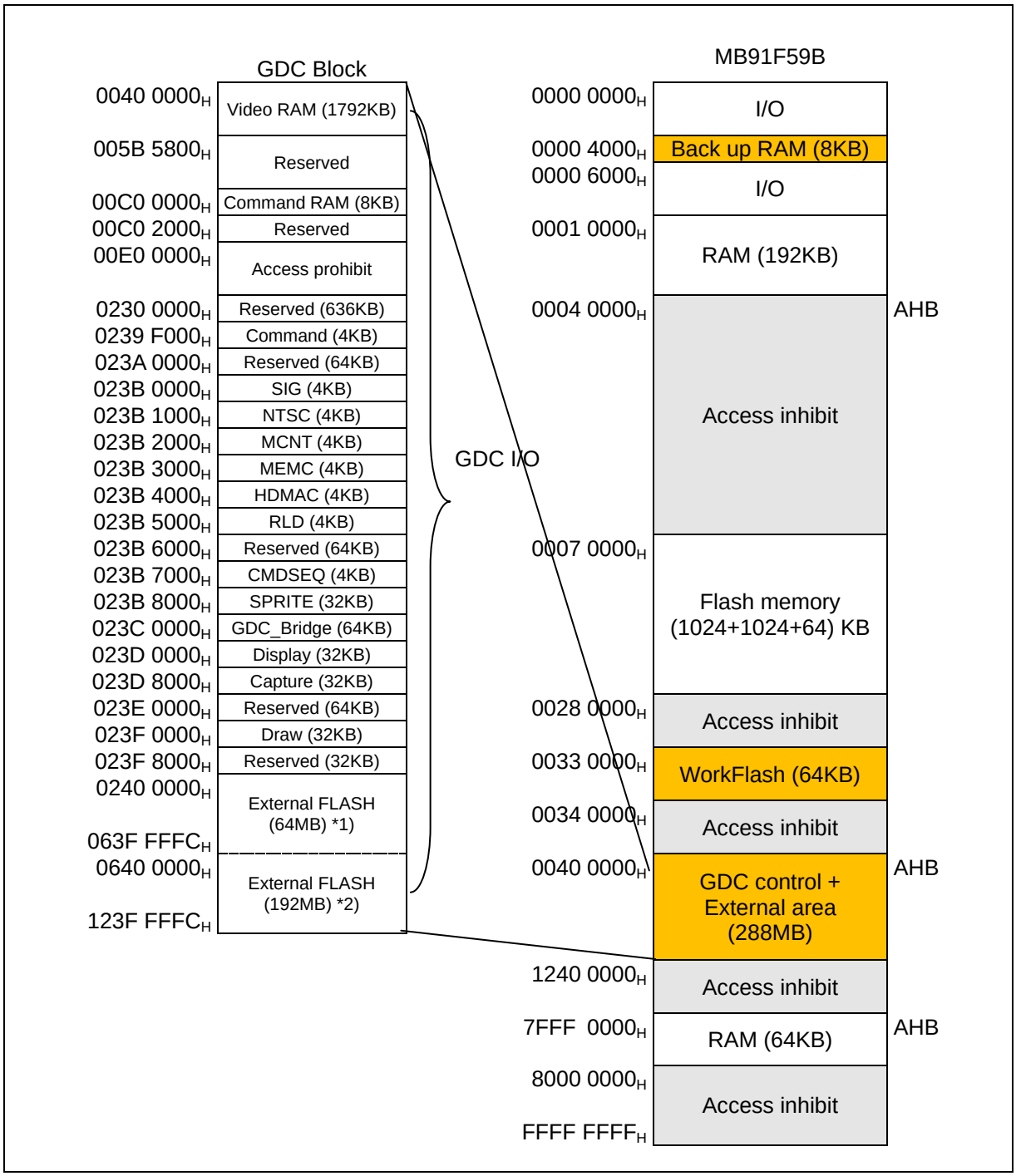
■Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress. packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking
Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

■GDC memory map

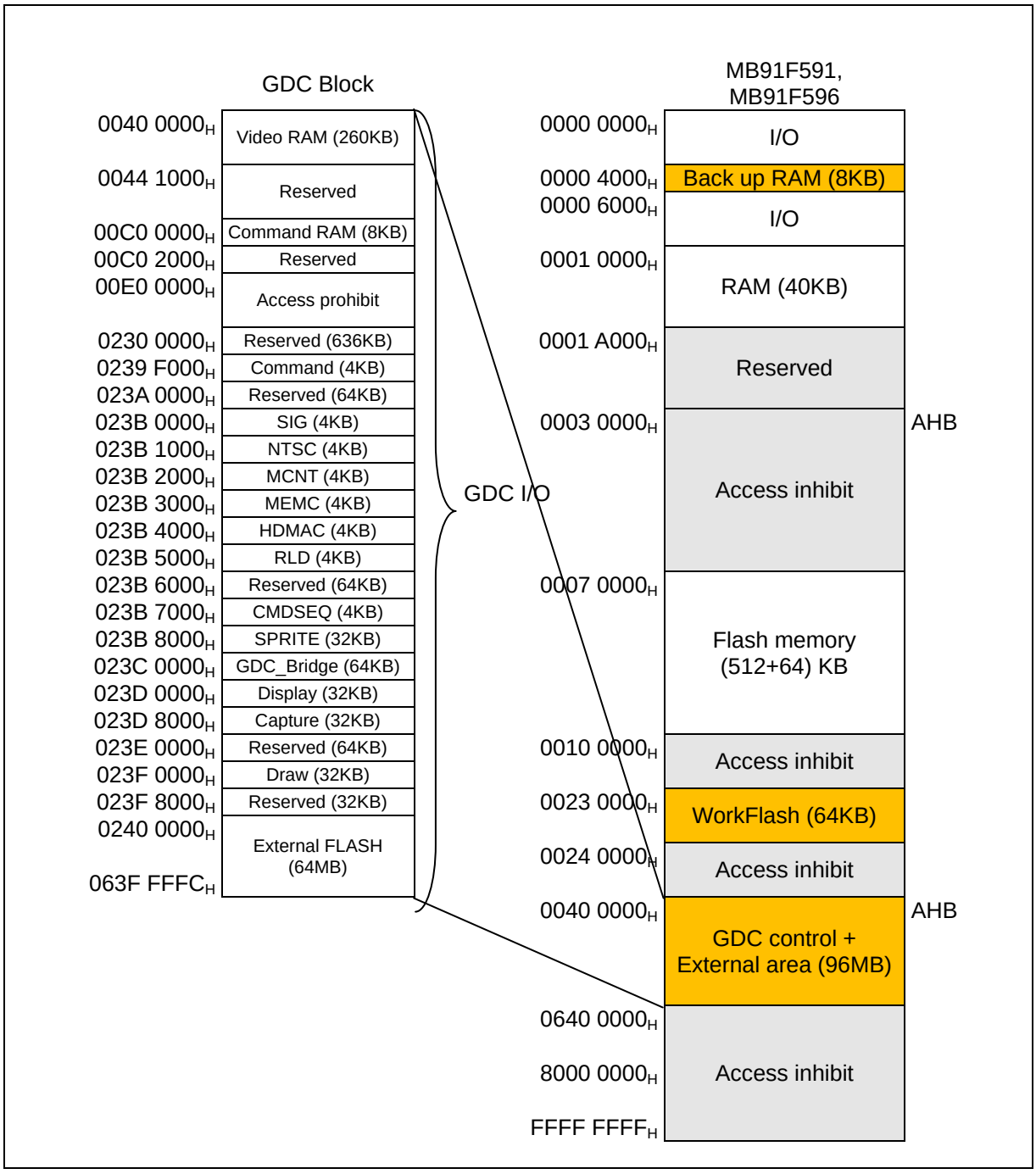


Note: The GDC area is executed mapping with the little endian.

*1) Parallel interface supports 64MB of memory space from 0240_0000H to 063F_FFFCH for External FLASH.

*2) HS-SPI supports additional 192MB of memory space from 0640_0000H to 123F_FFFFH.
(HS-SPI totally supports 256MB of memory space from 0240_0000H to 123F_FFFFH for External FLASH)

■GDC memory map



Note: The GDC area is executed mapping with the little endian.

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000090_H	BT1TMR [R] H 00000000 00000000		BT1TMCR [R/W] H -0000000 00000000		Base timer 1
000094_H	—	BT1STC [R/W] B 0000-000	—	—	
000098_H	BT1PCSR/BT1PRLL [R/W] H 00000000 00000000		BT1PDUT/BT1PRLH/BT1DTBF [R/W] H 00000000 00000000		
$00009C_H$	BTSEL01 [R/W] B ----0000	—	BTSSSR [W] B,H -------- ------11		Base timer 0,1
$0000A0_H$	ADERH [R/W] B, H, W 00000000 00000000		ADERL [R/W] B, H, W 00000000 00000000		A/D converter
$0000A4_H$	ADCS1 [R/W] B, H,W 0000000-	ADCS0 [R/W] B, H,W 00000000	ADCR1 [R] B, H,W ------XX	ADCR0 [R] B, H,W XXXXXXXX	
$0000A8_H$	ADCT1 [R/W] B, H,W 00010000	ADCT0 [R/W] B, H,W 00101100	ADSCH [R/W] B, H,W ---00000	ADECH [R/W] B, H,W ---00000	
$0000AC_H$	—	—	—	—	Reserved
$0000B0_H$	SCR0/(IBCR0) [R/W] B,H,W 0--00000	SMR0 [R/W] B,H,W 000-0000	SSR0 [R/W] B,H,W 0-000011	ESCR0/(IBSR0) [R/W] B,H,W -0000000	Multi-function serial 0 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000B4_H$	RDR0/(TDR0)[R/W] B,H,W *1 -------0 00000000		BGR0 [R/W] H,W 00000000 00000000		
$0000B8_H$	— / (ISMK0) [R/W] B,H,W -------- *2	— / (ISBA0) [R/W] B,H,W -------- *2	—	—	
$0000BC_H$	FCR10 [R/W] B,H,W ---00100	FCR00 [R/W] B,H,W -0000000	FBYTE20 [R/W] B,H,W 00000000	FBYTE10 [R/W] B,H,W 00000000	
$0000C0_H$	SCR1/(IBCR1) [R/W] B,H,W 0--00000	SMR1 [R/W] B,H,W 000-0000	SSR1 [R/W] B,H,W 0-000011	ESCR1/(IBSR1) [R/W] B,H,W -0000000	Multi-function serial 1 *1: Byte access is possible only for access to lower 8 bits *2: Reserved because I^2C mode is not set immediately after reset.
$0000C4_H$	RDR1/(TDR1)[R/W] B,H,W *1 -------0 00000000		BGR1 [R/W] H,W 00000000 00000000		
$0000C8_H$	— / (ISMK1) [R/W] B,H,W -------- *2	— /(ISBA1) [R/W] B,H,W -------- *2	—	—	
$0000CC_H$	FCR11 [R/W] B, H, W ---00100	FCR01[R/W] B, H, W -0000000	FBYTE21 [R/W] B,H,W 00000000	FBYTE11[R/W] B,H,W 00000000	
$0000D0_H$	SCR2 [R/W] B, H, W 00000000	SMR2 [R/W] B, H, W 00000000	SSR2 [R/W] B, H, W 00001000	RDR2 /TDR2 [R/W] B, H, W 00000000	LIN-UART2
$0000D4_H$	ESCR2 [R/W] B, H, W 00000X00	ECCR2 [R/W] B, H, W -0000-XX	BGR2 [R/W] B, H, W -0000000 00000000		
$0000D8_H$	SCR3 [R/W] B, H, W 00000000	SMR3 [R/W] B, H, W 00000000	SSR3 [R/W] B, H, W 00001000	RDR3 /TDR3 [R/W] B, H, W 00000000	LIN-UART3
$0000DC_H$	ESCR3 [R/W] B, H, W 00000X00	ECCR3 [R/W] B, H, W -0000-XX	BGR3 [R/W] B, H, W -0000000 00000000		

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$0001C0_H$	TMRLRA8 [R/W] H XXXXXXXX XXXXXXXX		TMR8 [R] H XXXXXXXX XXXXXXXX		Reload timer 8 MB91F59A/B only
$0001C4_H$	TMRLRB8 [R/W] H XXXXXXXX XXXXXXXX		TMCSR8 [R/W] B, H,W 00000000 0-000000		
$0001C8_H$	TMRLRA9 [R/W] H XXXXXXXX XXXXXXXX		TMR9 [R] H XXXXXXXX XXXXXXXX		Reload timer 9 MB91F59A/B only
$0001CC_H$	TMRLRB9 [R/W] H XXXXXXXX XXXXXXXX		TMCSR9 [R/W] B, H,W 00000000 0-000000		
$0001D0_H$	TMRLRA10 [R/W] H XXXXXXXX XXXXXXXX		TMR10 [R] H XXXXXXXX XXXXXXXX		Reload timer 10 MB91F59A/B only
$0001D4_H$	TMRLRB10 [R/W] H XXXXXXXX XXXXXXXX		TMCSR10 [R/W] B, H,W 00000000 0-000000		
$0001D8_H$ to $0001DC_H$	—	—	—	—	Reserved
$0001E0_H$	SCR10 [R/W] B,H,W 0--00000	SMR10 [R/W] B,H,W 000-0000	SSR10 [R/W] B,H,W 0-000011	ESCR10 [R/W] B,H,W -0000000	Multi-function serial 10 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001E4_H$	RDR10/(TDR10)[R/W] B,H,W *1 -------0 00000000		BGR10 [R/W] H,W 00000000 00000000		
$0001E8_H$	—	—	—	—	
$0001EC_H$	FCR110 [R/W] B,H,W ---00100	FCR010 [R/W] B,H,W -0000000	FBYTE210 [R/W] B,H,W 00000000	FBYTE110 [R/W] B,H,W 00000000	
$0001F0_H$	SCR11 [R/W] B,H,W 0--00000	SMR11 [R/W] B,H,W 000-0000	SSR11 [R/W] B,H,W 0-000011	ESCR11 [R/W] B,H,W -0000000	Multi-function serial 11 *1: Byte access is possible only for access to lower 8 bits. MB91F59A/B only
$0001F4_H$	RDR11/(TDR11)[R/W] B,H,W *1 -------0 00000000		BGR11 [R/W] H,W 00000000 00000000		
$0001F8_H$	—	—	—	—	
$0001FC_H$	FCR111 [R/W] B,H,W ---00100	FCR011 [R/W] B,H,W -0000000	FBYTE211 [R/W] B,H,W 00000000	FBYTE111 [R/W] B,H,W 00000000	

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
$000EA0_H$	PPCR00[R/W] B,H,W 11111111	PPCR01[R/W] B,H,W 11111111	PPCR02[R/W] B,H,W 11111111	PPCR03[R/W] B,H,W 11111111	Port pull-up/down control register
$000EA4_H$	PPCR04[R/W] B,H,W 11111111	PPCR05[R/W] B,H,W 11111111	PPCR06[R/W] B,H,W 11111111	PPCR07[R/W] B,H,W 11111111	
$000EA8_H$	PPCR08[R/W] B,H,W 11111111	PPCR09[R/W] B,H,W 11111111	PPCR10[R/W] B,H,W 11111111	PPCR11[R/W] B,H,W 11111111	
$000EAC_H$	PPCR12[R/W] B,H,W 11111111	PPCR13[R/W] B,H,W 11-11111	—	—	
$000EB0_H$	PPCRA[R/W] B,H,W 111111--	PPCRB[R/W] B,H,W 111111--	PPCRC[R/W] B,H,W 111111--	PPCRD[R/W] B,H,W 111111--	
$000EB4_H$	PPCRE[R/W] B,H,W 111111--	PPCRF[R/W] B,H,W 111111--	PPCRG[R/W] B,H,W 11111111	PPCRH[R/W] B,H,W ----1---	
$000EB8_H$ to $000EBC_H$	—	—	—	—	Reserved
$000EC0_H$	PPER00[R/W] B,H,W 00000000	PPER01[R/W] B,H,W 00000000	PPER02[R/W] B,H,W 00000000	PPER03[R/W] B,H,W 00000000	Port pull-up/down enable register
$000EC4_H$	PPER04[R/W] B,H,W 00000000	PPER05[R/W] B,H,W 00000000	PPER06[R/W] B,H,W 00000000	PPER07[R/W] B,H,W 00000000	
$000EC8_H$	PPER08[R/W] B,H,W 00000000	PPER09[R/W] B,H,W 00000000	PPER10[R/W] B,H,W 00000000	PPER11[R/W] B,H,W 00000000	
$000ECC_H$	PPER12[R/W] B,H,W 00000000	PPER13[R/W] B,H,W 00-00000	—	—	
$000ED0_H$	PPERA[R/W] B,H,W 000000--	PPERB[R/W] B,H,W 000000--	PPERC[R/W] B,H,W 000000--	PPERD[R/W] B,H,W 000000--	
$000ED4_H$	PPERE[R/W] B,H,W 000000--	PPERF[R/W] B,H,W 000000--	PPERG[R/W] B,H,W 00000000	PPERH[R/W] B,H,W ----0---	
$000ED8_H$ to $000EDC_H$	—	—	—	—	Reserved

Address	Address Offset Value / Register Name				Block
	+0	+1	+2	+3	
000FAC$_H$	CPCLR3 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 3
000FB0$_H$	TCDT3 [R/W] W 00000000 00000000 00000000 00000000				
000FB4$_H$	TCCSH3 [R/W] B, H, W 0-----00	TCCSL3 [R/W] B, H, W -1-00000	—		
000FB8$_H$	CPCLR4 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 4 MB91F59A/B only
000FBC$_H$	TCDT4 [R/W] W 00000000 00000000 00000000 00000000				
000FC0$_H$	TCCSH4 [R/W] B, H, W 0-----00	TCCSL4 [R/W] B, H, W -1-00000	—		
000FC4$_H$	CPCLR5 [R/W] W 11111111 11111111 11111111 11111111				Free-run timer 5 MB91F59A/B only
000FC8$_H$	TCDT5 [R/W] W 00000000 00000000 00000000 00000000				
000FCC$_H$	TCCSH5 [R/W] B, H, W 0-----00	TCCSL5 [R/W] B, H, W -1-00000	—		
000FD0$_H$	IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input capture 6,7 *1:MB91F591/2/4/6/7/9 *2:MB91F59A/B
000FD4$_H$	IPCP7 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FD8$_H$	ICFS67 [R/W] B, H, W ------00	—	LSYNS1 [R/W] B,H,W ------00*1 --000000*2	ICS67 [R/W] B, H, W 00000000	
000FDC$_H$	IPCP8 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 8,9 MB91F59A/B only
000FE0$_H$	IPCP9 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FE4$_H$	ICFS89 [R/W] B, H, W ------00	—	—	ICS89 [R/W] B, H, W 00000000	
000FE8$_H$	IPCP10 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Input Capture 10,11 MB91F59A/B only
000FEC$_H$	IPCP11 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000FF0$_H$	ICFS1011 [R/W] B, H, W ------00	—	—	ICS1011 [R/W] B, H, W 00000000	
000FF4$_H$	RCRH2[W] H,W XXXXXXXX	RCRL2[W] B,H,W XXXXXXXX	UDCRH2[R] H,W 00000000	UDCRL2[R] B,H,W 00000000	Up/down counter 2 MB91F59A/B only
000FF8$_H$	CCR2[R/W] B,H 00000000 -0001000		—	CSR2[R/W] B 00000000	
000FFC$_H$	—	—	—	—	Reserved
001000$_H$	SACR [R/W] B,H,W -------0	PICD [R/W] B,H,W ----0011	—	—	Synchronous/asynchronous switching control
001004$_H$ to 00103C$_H$	—	—	—	—	Reserved

*1: Does not support a DMA transfer request caused by an interrupt generated from a peripheral to which no RN (Resource Number) is assigned.

*2: The status of the multi-function serial interface does not support a DMA transfer caused by I^2C reception.

*3: The clock calibration unit does not support a DMA transfer caused by an interrupt.

*4: RAM ECC bit error does not support a DMA transfer caused by an interrupt.

*5: REALOS is a trademark of Cypress

*6: An interrupt of Up/down counter ch.2 does not support a DMA transfer.

*7: An interrupt related GDC does not support a DMA transfer.

**: Only supported by MB91F59A/B

UDCn: Up/down counter ch.n

ICUn: Input capture unit.n

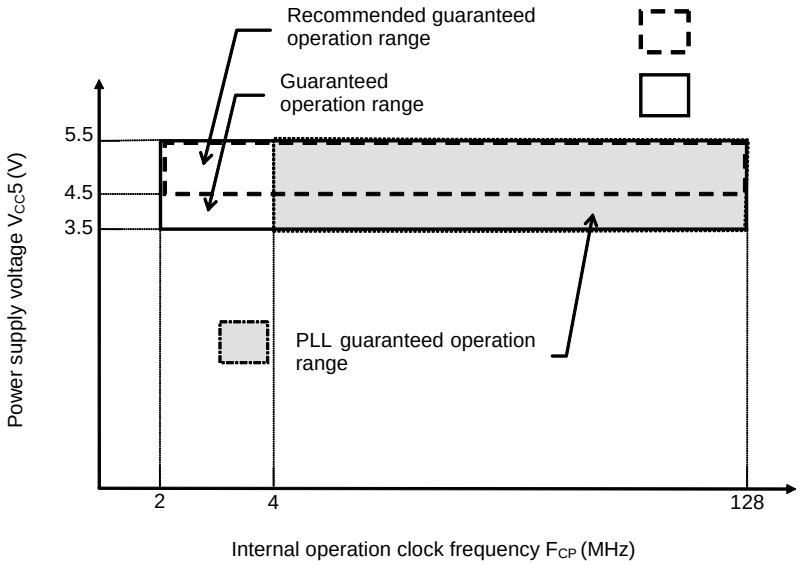
OCUn: Output compare unit.n

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, $V_{CC}3$=3.3V ± 10%, V_{SS}=DV_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V_{OH1}	P060 to P067, P070 to P077, P080 to P087, P090 to P097, P100 to P107, P110 to P117, P120 to P127, P130 to P137	$V_{CC}5$ = 4.5V I_{OH} = -1.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH2}		$V_{CC}5$ = 4.5V I_{OH} = -2.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	
	V_{OH3}	P060 to P067, P070 to P077, P080 to P087	DV_{CC} = 4.5V I_{OH} = -30.0mA	DV_{CC}-0.5	–	DV_{CC}	V	SMC shared pin
	V_{OH4}	P000 to P007, P010 to P017, P020 to P027, P030 to P037, P040 to P047, P050 to P057, PA2 to PA7, PB2 to PB7, PC2 to PC7, PD2 to PD7, PE2 to PE7, PF2 to PF7, PG0 to PG7, PH3	$V_{CC}3$ = 3.0V I_{OH} = -2.0mA	$V_{CC}3$-0.5	–	$V_{CC}3$	V	3.3V dedicated pin
	V_{OH5}		$V_{CC}3$ = 3.0V I_{OH} = -5.0mA					
	V_{OH6}		$V_{CC}3$ = 3.0V I_{OH} = -10.0mA					
	V_{OH7}		$V_{CC}3$ = 3.0V I_{OH} = -20.0mA					
	V_{OH8}	TDO	$V_{CC}5$ = 4.5V I_{OH} = -5.0mA	$V_{CC}5$-0.5	–	$V_{CC}5$	V	BGA product only

Guaranteed Operation Range (5V Operating microcontroller Section)

Internal operation clock frequency vs. Power supply voltage

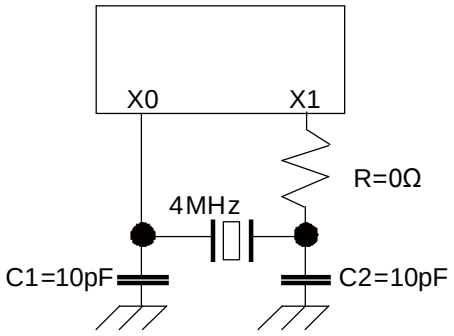


Note: The CPU will be reset at the power supply voltage 4V±0.3V or less.

Oscillation Clock Frequency vs. Internal Operation Clock Frequency

		Internal Operation Clock Frequency							
		Main Clock	PLL Clock						
			Multiplied by 1	Multiplied by 2	Multiplied by 3	Multiplied by 4	...	Multiplied by 20	Multiplied by 32
Oscillation clock frequency	4MHz	2MHz	4MHz	8MHz	12MHz	16MHz	...	80MHz	128MHz

• Example of Oscillation Circuit



Note: As to the product with its clock supervisor's initial value is "ON", when the oscillator is unable to start within 20ms from the stop state the clock supervisor will detect the oscillation stop. As a result, the CPU moves to the fail safe operation.
Design your printed circuit board so that the oscillator can start oscillation within 20ms.

11.4.1.3 Power-on Conditions

(T_A: Recommended operating conditions, V_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Level detection voltage	–	$V_{CC}5$	–	2.1	2.3	2.5	V	When turning on power for microcontroller
Level detection hysteresis width	–	$V_{CC}5$	–	–	–	125	mV	During voltage drop
Level detection time	–	–	–	–	–	30	us	*1
Specification for voltage slope detection	–	$V_{CC}5$	$V_{CC}5$ = at level detection release level time	–	–	4	mV/µs	*2
Power off time	t_{OFF}	$V_{CC}5$	–	50	–	–	ms	*3

*1: If the fluctuation of the power supply is faster than the low voltage detection time, there is the possibility to generate or release after the power supply voltage has exceeded the detection voltage range.

*2: When setting the power supply fluctuation to this specification or less, it is possible to suppress the voltage slope detection. This is the specification when the power supply fluctuation is stable.

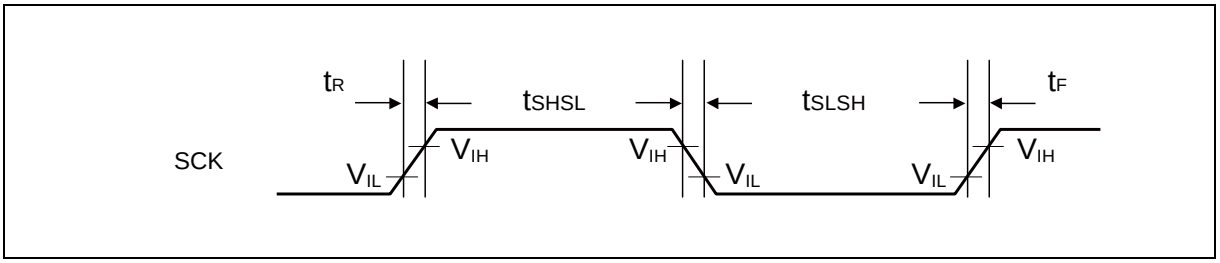
*3: This time is to start the voltage slope detection at next power on after power down and internal charge loss.

External Clock (EXT = 1): Asynchronous Only

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V±10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit
				Min	Max	
Serial clock "H" pulse width	t_{SHSL}	SCKx	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA)	t_{CPP}+10	-	ns
Serial clock "L" pulse width	t_{SLSH}			t_{CPP}+10	-	ns
SCK fall time	t_F			-	5	ns
SCK rise time	t_R			-	5	ns

Note: "x" means channel number of 0, 1, 8, 9, 10, and 11 for SCKx, SINx and SOTx.



I²C Timing

(T_A: Recommended operating conditions, $V_{CC}5$=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Standard Mode		High-Speed Mode		Unit	Remarks
				Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	SCK0, SCK1	C_L=50pF (When drive capability is 2mA or more.) C_L=20pF (When drive capability is 1mA) R = (V_P/I_{OL}) *1	0	100	0	400	kHz	
Repeat "start" condition hold time SDA ↓ → SCL ↓	t_{HDSTA}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Period of "L" for SCL clock	t_{LOW}	SCK0, SCK1, (SCL)		4.7	–	1.3	–	µs	
Period of "H" for SCL clock	t_{HIGH}	SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Repeat "start" condition setup time SCL ↑ → SDA ↓	t_{SUSTA}	SCK0, SCK1, (SCL)		4.7	–	0.6	–	µs	
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		0	3.45*2	0	0.9	µs	
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		250*3	–	100	–	ns	
"Stop" condition setup time SCL ↑ → SDA ↑	t_{SUSTO}	SOT0, SOT1, (SDA) SCK0, SCK1, (SCL)		4.0	–	0.6	–	µs	
Bus-free time between "stop" condition and "start" condition	t_{BUF}	–		4.7	–	1.3	–	µs	
Noise filter	t_{SP}	–	–	2t_{CPP}*4	–	2t_{CPP}*4	–	ns	

*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA output lines, respectively. Vp shows that the power-supply voltage of the pull-up resistor and I_{OL} shows the V_{OL} guarantee current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I²C bus device can be used on a standard mode I²C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250 ns".

*4: t_{CPP} is the peripheral clock cycle time. Adjust the peripheral clock frequency to 8MHz or more when use I²C.

■Bit setting: ESCR: SCES=0, ECCR: SCDE=1

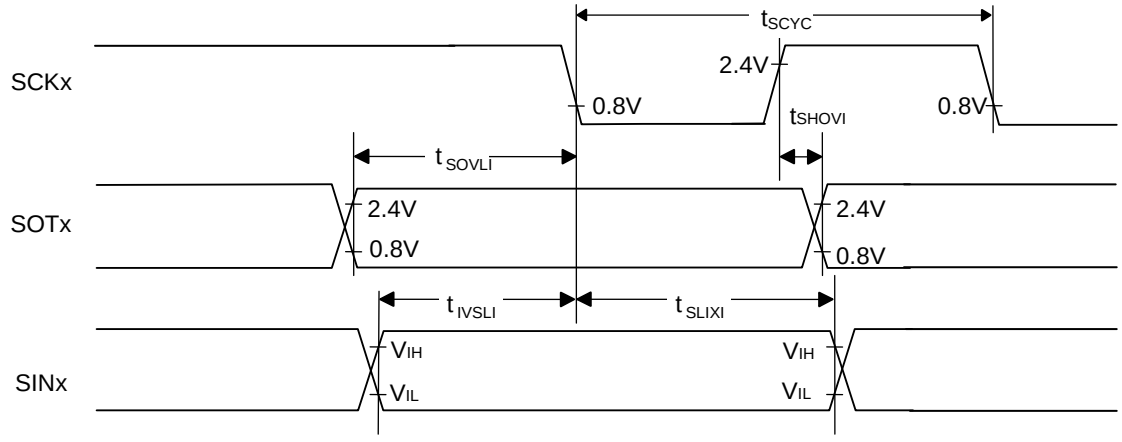
(T_A: Recommended operating conditions, V_{CC}5=5.0V ± 10%, V_{SS}=AV_{SS}=0.0V)

Parameter	Symbol	Pin Name	Conditions	Value		Unit	Remarks
				Min	Max		
Serial clock cycle time	t_{SCYC}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7		$5t_{CPP}$	–	ns	
SCK ↑ → SOT delay time	t_{SHOVI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		-50	+50	ns	
Valid SIN → SCK ↓ setup time	t_{IVSLI}	SCK2,SCK3, SCK4,SCK5,	–	t_{CPP}+80	–	ns	Internal shift clock Mode: C_L=80pF + 1 • TTL
SCK ↓ → Valid SIN hold time	t_{SLIXI}	SCK6,SCK7, SIN2,SIN3, SIN4,SIN5, SIN6,SIN7		0	–	ns	
SOT → SCK ↓ delay time	t_{SOVLI}	SCK2,SCK3, SCK4,SCK5, SCK6,SCK7, SOT2,SOT3, SOT4,SOT5, SOT6,SOT7		$3t_{CPP}$-70	–	ns	

Notes:

- C_L is the load capacitance applied to pins during testing.
- The maximum baud rate is limited by internal operation clock used and other parameters.
- See Hardware Manual for details.

• Internal Shift Clock Mode

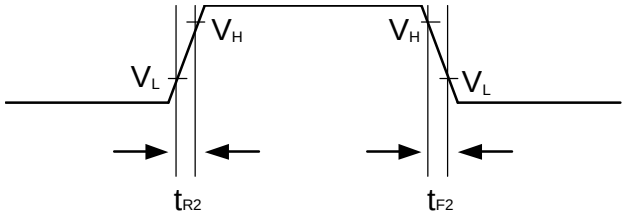


11.4.1.11 High current output slew rate

(T_A: Recommended operating conditions, $V_{CC}5=AV_{CC}5=5.0V \pm 10\%$, $V_{SS}=AV_{SS}=0.0V$)

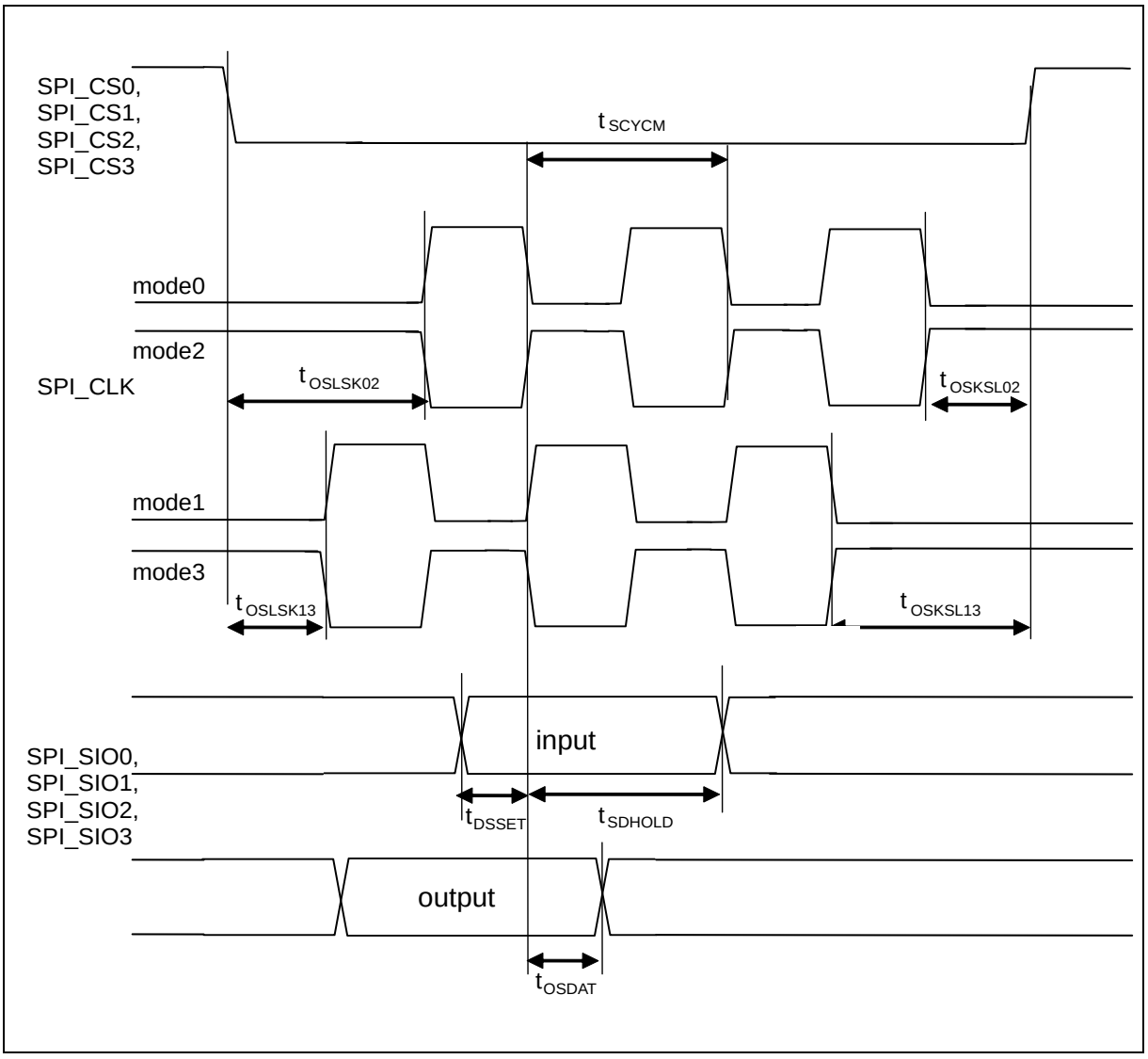
Parameter	Symbol	Pin Name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Output rise /fall time	t_{R2}, t_{F2}	P060 to P067, P070 to P077, P080 to P087	–	15	–	100	ns	load capacitance 85pF

• **Slew Rate Output Timing**



$V_H=V_{OL2}+0.9\times(V_{OH2}-V_{OL2})$

$V_L=V_{OL2}+0.1\times(V_{OH2}-V_{OL2})$


SPI_CS0,
SPI_CS1,
SPI_CS2,
SPI_CS3
tSCYCM
mode0
mode2
SPI_CLK
tOSLSK02
tOSKSL02
mode1
mode3
tOSLSK13
tOSKSL13
SPI_SIO0,
SPI_SIO1,
SPI_SIO2,
SPI_SIO3
input
tDSSET
tSDHOLD
output
tOSDAT

■AC Timing Specifications

Parameter	Symbol	min.
Display clock cycle time	t_{dcyc}	18.5 ns

External Load Condition 50 pF

Parameter	Symbol	DCLKO Reference Edge	IO Drive capability Setting		Remark
			10 mA	2 mA	
Setup time	t_{dosu}	neg, pos *1	t_{dcyc}_f - 8.5ns	t_{dcyc}_f - 10.2ns	
Hold time	t_{dohd}	-	t_{dcyc}_l - 1.7ns	t_{dcyc}_l - 3.3ns	*2
		-	t_{dcyc}_l - 3.2ns	t_{dcyc}_l – 5.1ns	*3

*1: DCLKO reference edge: This is the reference clock edge for setup time and hold time.
Pos = The external display device receives the signal at the rising edge of DCLKO.
Neg = The external display device receives the signal at the falling edge of DCLKO.

*2: Should be applied to RGB666.

*3: Should be applied to RGB888.

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