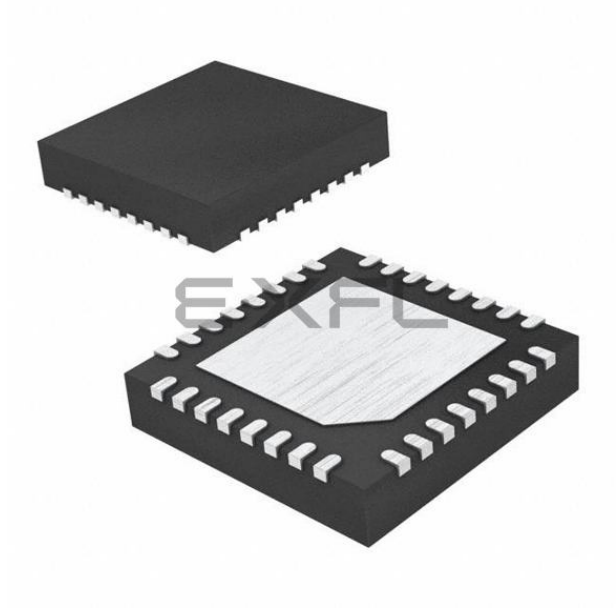
Microchip Technology - DSPIC33EP128GS702-I/MM Datasheet



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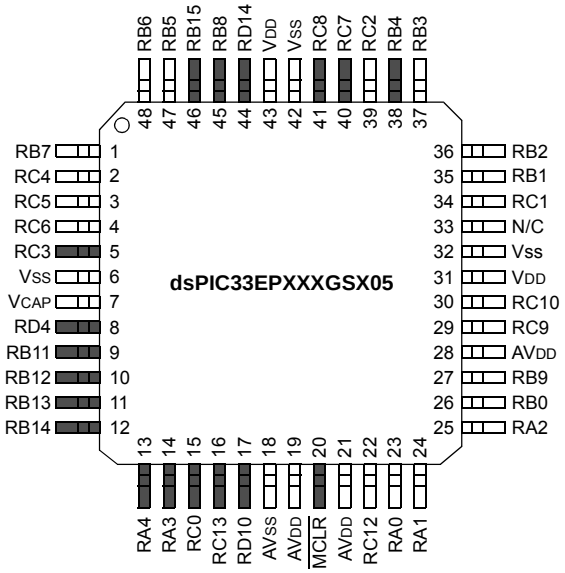
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	20
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN-S (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs702-i-mm

Pin Diagrams (Continued)

48-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PGEC1/AN21/SDA1/**RP39**/RB7	25	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/**RP18**/RA2
2	AN1ALT/**RP52**/RC4	26	AN3/CMP1D/CMP2B/PGA2P3/**RP32**/RB0
3	AN0ALT/**RP53**/RC5	27	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9
4	AN17/**RP54**/RC6	28	AVDD
5	**RP51**/RC3	29	AN11/PGA1N3/**RP57**/RC9
6	VSS	30	EXTREF2/AN10/PGA1P4/**RP58**/RC10
7	VCAP	31	VDD
8	**RP68**/RD4	32	VSS
9	TMS/PWM3H/**RP43**/RB11	33	N/C
10	TCK/PWM3L/**RP44**/RB12	34	AN8/CMP4C/PGA2P4/**RP49**/RC1
11	PWM2H/**RP45**/RB13	35	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1
12	PWM2L/**RP46**/RB14	36	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/**RP34**/RB2
13	PWM1H/**RP20**/RA4	37	PGED2/DACOUT1/AN18/INT0/**RP35**/RB3
14	PWM1L/**RP19**/RA3	38	PGEC2/ADTRG31/**RP36**/RB4
15	FLT12/**RP48**/RC0	39	EXTREF1/AN9/CMP4D/**RP50**/RC2
16	FLT11/**RP61**/RC13	40	ASDA1/**RP55**/RC7
17	CLC4OUT/FLT10/**RP74**/RD10	41	ASCL1/**RP56**/RC8
18	AVSS	42	VSS
19	AVDD	43	VDD
20	$\overline{\text{MCLR}}$	44	CLC3OUT/RD14
21	AVDD	45	PGED3/SDA2/FLT31/**RP40**/RB8
22	AN14/PGA2N3/**RP60**/RC12	46	PGEC3/SCL2/**RP47**/RB15
23	AN0/CMP1A/PGA1P1/**RP16**/RA0	47	TDO/AN19/PGA2N2/**RP37**/RB5
24	AN1/CMP1B/PGA1P2/PGA2P1/**RP17**/RA1	48	PGED1/TDI/AN20/SCL1/**RP38**/RB6

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 11-12 and Table 11-13 for the complete list of remappable sources.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	Yes	UART2 IrDA baud clock output.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes(3)	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
FLT1-FLT8	I	ST	Yes	PWM Fault Inputs 1 through 8.
FLT9-FLT12	I	ST	No	PWM Fault Inputs 9 through 12.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 through 3.
PWM4L-PWM8L(2)	O	—	Yes	PWM Low Outputs 4 through 8.
PWM4H-PWM8H(2)	O	—	Yes	PWM High Outputs 4 through 8.
SYNCI1, SYNCI2	I	ST	Yes	PWM Synchronization Inputs 1 and 2.
SYNCO1, SYNCO2	O	—	Yes	PWM Synchronization Outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4H/L through PWM8H/L are fixed on dsPIC33EPXXXGS708/808 devices. PWM4H/L through PWM6H/L are fixed on dsPIC33EPXXXGS706/806 devices.

3: The SCK3 pin is fixed on dsPIC33EPXXXGS706/806 and dsPIC33EPXXXGS708/808 devices.

4: PPS is available on dsPIC33EPXXXGS702 devices only.

FIGURE 2-6: OFF-LINE UPS

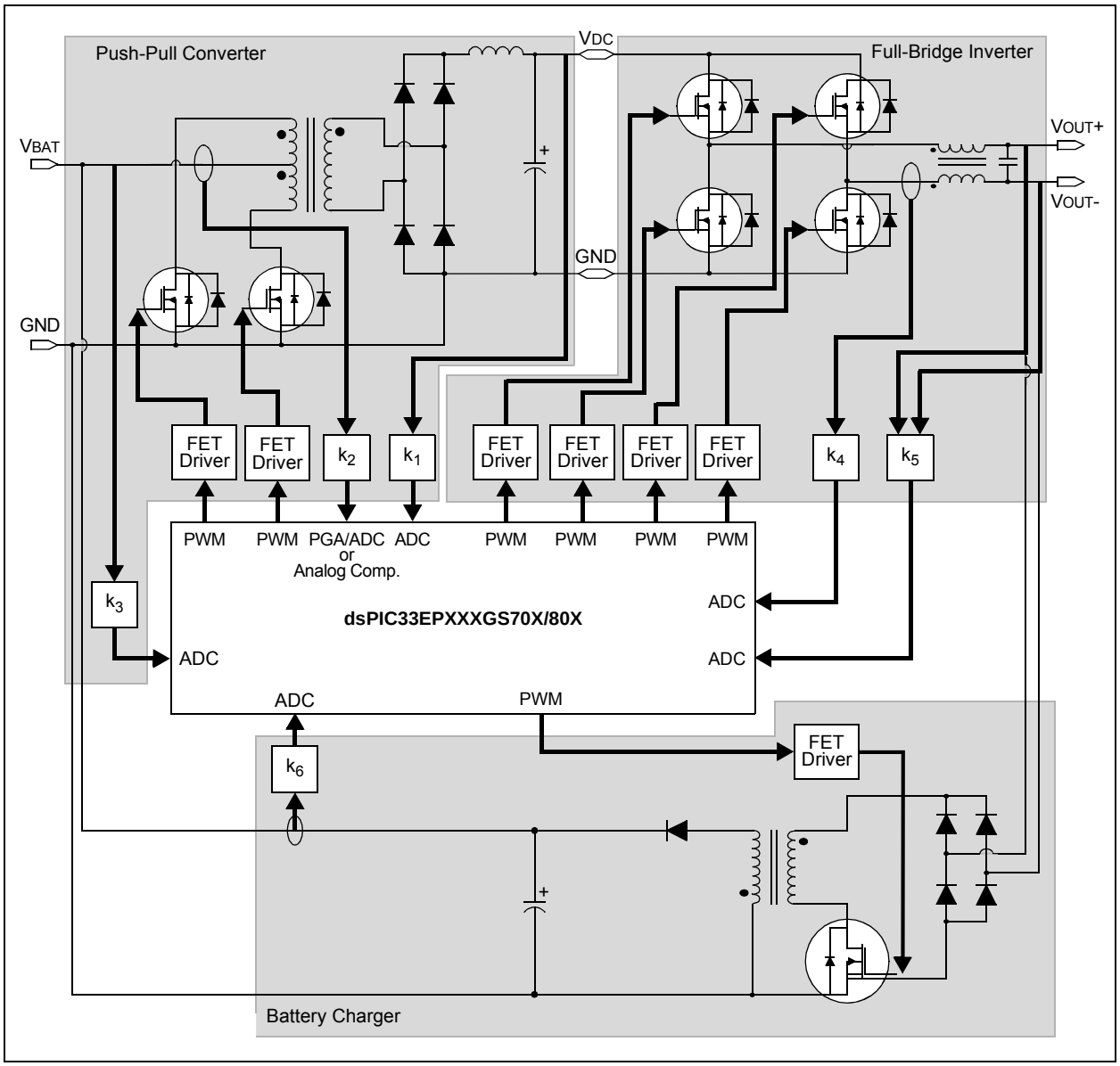


TABLE 4-4: SFR BLOCK 200h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I2C1 and I2C2			U1STA	222	0000000010010000	SPI1BRGH	252	0000000000000000
I2C1CONL	200	0001000000000000	U1TXREG	224	0000000xxxxxxxxx	SPI1IMSKL	254	0000000000000000
I2C1CONH	202	0000000000000000	U1RXREG	226	0000000000000000	SPI1IMSKH	256	0000000000000000
I2C1STAT	204	0000000000000000	U1BRG	228	0000000000000000	SPI1URDTL	258	0000000000000000
I2C1ADD	206	0000000000000000	U2MODE	230	0000000000000000	SPI1URDTH	25A	0000000000000000
I2C1MSK	208	0000000000000000	U2STA	232	0000000010010000	SPI2CON1L	260	0000000000000000
I2C1BRG	20A	0000000000000000	U2TXREG	234	0000000xxxxxxxxx	SPI2CON1H	262	0000000000000000
I2C1TRN	20C	0000000011111111	U2RXREG	236	0000000000000000	SPI2CON2L	264	0000000000000000
I2C1RCV	20E	0000000000000000	U2BRG	238	0000000000000000	SPI2CON2H	266	0000000000000000
I2C2CON1	210	0001000000000000	**SPI**			SPI2STATL	268	0000000000101000
I2C2CON2	212	0000000000000000	SPI1CON1L	240	0000000000000000	SPI2STATH	26A	0000000000000000
I2C2STAT	214	0000000000000000	SPI1CON1H	242	0000000000000000	SPI2BUFL	26C	0000000000000000
I2C2ADD	216	0000000000000000	SPI1CON2L	244	0000000000000000	SPI2BUFH	26E	0000000000000000
I2C2MSK	218	0000000000000000	SPI1CON2H	246	0000000000000000	SPI3STAT	270	000xxxxxxxxxxxx
I2C2BRG	21A	0000000000000000	SPI1STATL	248	0000000000101000	SPI2BRGH	272	0000000000000000
I2C2TRN	21C	0000000011111111	SPI1STATH	24A	0000000000000000	SPI2IMSKL	274	0000000000000000
I2C2RCV	21E	0000000000000000	SPI1BUFL	24C	0000000000000000	SPI2IMSKH	276	0000000000000000
UART1 and UART2			SPI1BUFH	24E	0000000000000000	SPI2URDTL	278	0000000000000000
U1MODE	220	0000000000000000	SPI1BRGL	250	000xxxxxxxxxxxx	SPI2URDTH	27A	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-5: SFR BLOCK 300h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
ADC			ADCMP0ENH	33A	0000000000000000	ADTRIG4L	390	0000000000000000
ADCON1L	300	0000000000000000	ADCMP0LO	33C	0000000000000000	ADTRIG4H	392	0000000000000000
ADCON1H	302	0000000001100000	ADCMP0HI	33E	0000000000000000	ADCMP0CON	3A0	0000000000000000
ADCON2L	304	0000000000000000	ADCMP1ENL	340	0000000000000000	ADCMP1CON	3A4	0000000000000000
ADCON2H	306	0000000000000000	ADCMP1ENH	342	0000000000000000	ADBASE	3C0	0000000000000000
ADCON3L	308	0000000000000000	ADCMP1LO	344	0000000000000000	ADLVLTRGL	3D0	0000000000000000
ADCON3H	30A	0000000000000000	ADCMP1HI	346	0000000000000000	ADLVLTRGH	3D2	0000000000000000
ADCON4L	30C	0000000000000000	ADFL0DAT	368	0000000000000000	ADCORE0L	3D4	0000000000000000
ADCON4H	30E	0000000000000000	ADFL0CON	36A	0000000000000000	ADCORE0H	3D6	0000001100000000
ADMOD0L	310	0000000000000000	ADFL1DAT	36C	0000000000000000	ADCORE1L	3D8	0000000000000000
ADMOD0H	312	0000000000000000	ADFL1CON	36E	0000000000000000	ADCORE1H	3DA	0000001100000000
ADMOD1L	314	0000000000000000	ADTRIG0L	380	0000000000000000	ADCORE2L	3DC	0000000000000000
ADIEL	320	0000000000000000	ADTRIG0H	382	0000000000000000	ADCORE2H	3DE	0000001100000000
ADIEH	322	0000000000000000	ADTRIG1L	384	0000000000000000	ADCORE3L	3E0	0000000000000000
ADCSS1L	328	0000000000000000	ADTRIG1H	386	0000000000000000	ADCORE3H	3E2	0000001100000000
ADCSS1H	32A	0000000000000000	ADTRIG2L	388	0000000000000000	ADEIEL	3F0	0000000000000000
ADSTATL	330	0000000000000000	ADTRIG2H	38A	0000000000000000	ADEIEH	3F2	0000000000000000
ADSTATH	332	0000000000000000	ADTRIG3L	38C	0000000000000000	ADEISTATL	3F8	0000000000000000
ADCMP0ENL	338	0000000000000000	ADTRIG3H	38E	0000000000000000	ADEISTATH	3FA	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-15: SFR BLOCK E00h-F00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
PORTA			ANSELB	E1E	0000001011101111	CNPDD	E3C	0000000000000000
TRISA	E00	0000000000011111	**PORTC**			ANSELD	E3E	0110000110100000
PORTA	E02	0000000000000000	TRISC	E20	0111011111111111	**PORTE**		
LATA	E04	0000000000000000	PORTC	E22	0000000000000000	TRISE	E40	1111111111111111
ODCA	E06	0000000000000000	LATC	E24	0000000000000000	PORTE	E42	0000000000000000
CNENA	E08	0000000000000000	ODCC	E26	0000000000000000	LATE	E44	0000000000000000
CNPUA	E0A	0000000000000000	CNENC	E28	0000000000000000	ODCE	E46	0000000000000000
CNPDA	E0C	0000000000000000	CNPUC	E2A	0000000000000000	CNENE	E48	0000000000000000
ANSELA	E0E	0000000000000111	CNPDC	E2C	0000000000000000	CNPUE	E4A	0000000000000000
PORTB			ANSELC	E2E	0001011001110111	CNPDE	E4C	0000000000000000
TRISB	E10	0111101111111111	**PORTD**			ANSELE	E4E	1100000100000000
PORTB	E12	0000000000000000	TRISD	E30	1111111111111111	**CPU**		
LATB	E14	0000000000000000	PORTD	E32	0000000000000000	VISI	F88	0000000000000000
ODCB	E16	0000000000000000	LATD	E34	0000000000000000	**JTAG**		
CNENB	E18	0000000000000000	ODCD	E36	0000000000000000	JDATAH	FF0	0000000000000000
CNPUB	E1A	0000000000000000	CNEND	E38	0000000000000000	JDATAL	FF2	0000000000000000
CNPDB	E1C	0000000000000000	CNPUD	E3A	0000000000000000			

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

FIGURE 4-11: BIT-REVERSED ADDRESSING EXAMPLE

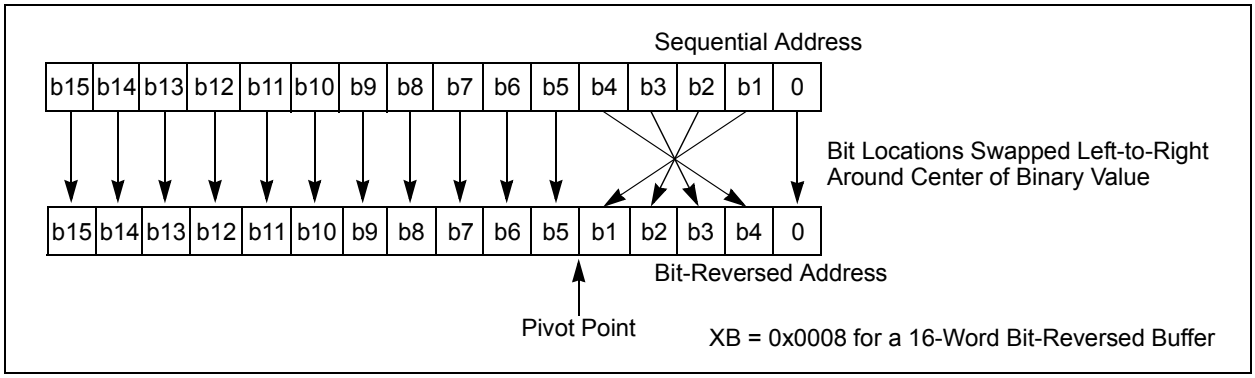


TABLE 4-18: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	**A2**	**A1**	**A0**	**Decimal**	**A3**	**A2**	**A1**	**A0**	**Decimal**
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

REGISTER 7-7: INTTREG: INTERRUPT CONTROL AND STATUS REGISTER

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	ILR3	ILR2	ILR1	ILR0
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-8 **ILR<3:0>:** New CPU Interrupt Priority Level bits
1111 = CPU Interrupt Priority Level is 15
•
•
•
0001 = CPU Interrupt Priority Level is 1
0000 = CPU Interrupt Priority Level is 0

bit 7-0 **VECNUM<7:0>:** Vector Number of Pending Interrupt bits
11111111 = 255, Reserved; do not use
•
•
•
00001001 = 9, IC1 – Input Capture 1
00001000 = 8, INT0 – External Interrupt 0
00000111 = 7, Reserved; do not use
00000110 = 6, Generic soft error trap
00000101 = 5, Reserved; do not use
00000100 = 4, Math error trap
00000011 = 3, Stack error trap
00000010 = 2, Generic hard trap
00000001 = 1, Address error trap
00000000 = 0, Oscillator fail trap

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

- Four DMA Channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM Start addresses after each block transfer complete)
- DMA Request for each Channel can be Selected from any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
CAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
CAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
CAN2 – RX Data Ready	00110111	0X0540(C2RXD)	—
CAN2 – TX Data Request	01000111	—	0X0542(C2TXD)

REGISTER 11-45: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP53R6	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP52R6	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP53R<6:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP52R<6:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-46: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP55R6	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP54R6	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP55R<6:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP54R<6:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 16-16: SPHASEx: PWMx SECONDARY PHASE-SHIFT REGISTER (x = 1 to 8)(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **SPHASEx<15:0>:** Secondary Phase Offset for PWMxL Output Pin bits (used in Independent PWM mode only)

Note 1: If PWMCONx<9> = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); SPHASEx<15:0> = Not used
- True Independent Output mode (IOCONx<11:10> = 11), PHASEx<15:0> = Phase-shift value for PWMxL only

2: If PWMCONx<9> = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); SPHASEx<15:0> = Not used
- True Independent Output mode (IOCONx<11:10> = 11); PHASEx<15:0> = Independent time base period value for PWMxL only
- When the PHASEx/SPHASEx registers provide the local period, the valid range of values is 0x0010-0xFFF8

REGISTER 17-6: PTGSDLIM: PTG STEP DELAY LIMIT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGSDLIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGSDLIM<15:0>:** PTG Step Delay Limit Register bits
Holds a PTG Step delay value, representing the number of additional PTG clocks, between the start of a Step command and the completion of a Step command.

Note 1: A base Step delay of one PTG clock is added to any value written to the PTGSDLIM register (Step Delay = (PTGSDLIM) + 1).

2: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 17-7: PTGC0LIM: PTG COUNTER 0 LIMIT REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGC0LIM<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PTGC0LIM<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PTGC0LIM<15:0>:** PTG Counter 0 Limit Register bits
May be used to specify the loop count for the PTGJMPC0 Step command or as a limit register for the General Purpose Counter 0.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 18-4: SPIxSTATL: SPIx STATUS REGISTER LOW (CONTINUED)

bit 3 **SPITBE:** SPIx Transmit Buffer Empty Status bit
1 = SPIxTXB is empty
0 = SPIxTXB is not empty
Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR. Automatically cleared in hardware when SPIxBUF is written, loading SPIxTXB.
Enhanced Buffer mode:
Indicates TXELM<5:0> = 000000.

bit 2 **Unimplemented:** Read as '0'

bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = SPIxTXB is full
0 = SPIxTXB not full
Standard Buffer mode:
Automatically set in hardware when SPIxBUF is written, loading SPIxTXB. Automatically cleared in hardware when SPIx transfers data from SPIxTXB to SPIxTXSR.
Enhanced Buffer mode:
Indicates TXELM<5:0> = 111111.

bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = SPIxRXB is full
0 = SPIxRXB is not full
Standard Buffer mode:
Automatically set in hardware when SPIx transfers data from SPIxRXSR to SPIxRXB. Automatically cleared in hardware when SPIxBUF is read from, reading SPIxRXB.
Enhanced Buffer mode:
Indicates RXELM<5:0> = 111111.

Note 1: SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

22.0 HIGH-SPEED, 12-BIT ANALOG-TO-DIGITAL CONVERTER (ADC)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"12-Bit High-Speed, Multiple SARs A/D Converter (ADC)**" (DS70005213) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

dsPIC33EPXXXGS70X/80X devices have a high-speed, 12-bit Analog-to-Digital Converter (ADC) that features a low conversion latency, high resolution and oversampling capabilities to improve performance in AC/DC, DC/DC power converters.

22.1 Features Overview

The high-speed, 12-bit multiple SARs Analog-to-Digital Converter (ADC) includes the following features:

- Five ADC Cores: Four Dedicated Cores and One Shared (common) Core
- User-Configurable Resolution of up to 12 Bits for each Core
- Up to 3.25 Msps Conversion Rate per Channel at 12-Bit Resolution
- Low Latency Conversion
- Up to 22 Analog Input Channels, with a Separate 16-Bit Conversion Result Register for each Input
- Conversion Result can be Formatted as Unsigned or Signed Data, on a per Channel Basis, for All Channels
- Single-Ended and Pseudodifferential Conversions are available on All ADC Cores
- Simultaneous Sampling of up to 5 Analog Inputs
- Channel Scan Capability
- Multiple Conversion Trigger Options for each Core, including:
  - PWM1 through PWM6 (primary and secondary triggers, and current-limit event trigger)
  - PWM Special Event Trigger
  - Timer1/Timer2 period match
  - Output Compare 1 and event trigger
  - External pin trigger event (ADTRG31)
  - Software trigger
- Two Integrated Digital Comparators with Dedicated Interrupts:
  - Multiple comparison options
  - Assignable to specific analog inputs
- Two Oversampling Filters with Dedicated Interrupts:
  - Provide increased resolution
  - Assignable to a specific analog input

The module consists of five independent SAR ADC cores. Simplified block diagrams of the multiple SARs 12-bit ADC are shown in Figure 22-1, Figure 22-2 and Figure 22-3.

The analog inputs (channels) are connected through multiplexers and switches to the Sample-and-Hold (S&H) circuit of each ADC core. The core uses the channel information (the output format, the Measurement mode and the input number) to process the analog sample. When conversion is complete, the result is stored in the result buffer for the specific analog input, and passed to the digital filter and digital comparator if they were configured to use data from this particular channel.

The ADC module can sample up to five inputs at a time (four inputs from the dedicated SAR cores and one from the shared SAR core). If multiple ADC inputs request conversion on the shared core, the module will convert them in a sequential manner, starting with the lowest order input.

The ADC provides each analog input the ability to specify its own trigger source. This capability allows the ADC to sample and convert analog inputs that are associated with PWM generators operating on independent time bases.

REGISTER 22-6: ADCON3H: ADC CONTROL REGISTER 3 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLKSEL1	CLKSEL0	CLKDIV5	CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	CLKDIV0
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SHREN	—	—	—	C3EN	C2EN	C1EN	C0EN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **CLKSEL<1:0>:** ADC Module Clock Source Selection bits
11 = APLL
10 = FRC
01 = FOSC (System Clock x 2)
00 = FSYS (System Clock)

bit 13-8 **CLKDIV<5:0>:** ADC Module Clock Source Divider bits
The divider forms a TCORESRC clock used by all ADC cores (shared and dedicated) from the TSRC ADC module clock source selected by the CLKSEL<1:0> bits. Then, each ADC core individually divides the TCORESRC clock to get a core-specific TADCORE clock using the ADCS<6:0> bits in the ADCOREXH register or the SHRADCS<6:0> bits in the ADCON2L register.
111111 = 64 Source Clock Periods
•
•
•
000011 = 4 Source Clock Periods
000010 = 3 Source Clock Periods
000001 = 2 Source Clock Periods
000000 = 1 Source Clock Period

bit 7 **SHREN:** Shared ADC Core Enable bit
1 = Shared ADC core is enabled
0 = Shared ADC core is disabled

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **C3EN:** Dedicated ADC Core 3 Enable bits
1 = Dedicated ADC Core 3 is enabled
0 = Dedicated ADC Core 3 is disabled

bit 2 **C2EN:** Dedicated ADC Core 2 Enable bits
1 = Dedicated ADC Core 2 is enabled
0 = Dedicated ADC Core 2 is disabled

bit 1 **C1EN:** Dedicated ADC Core 1 Enable bits
1 = Dedicated ADC Core 1 is enabled
0 = Dedicated ADC Core 1 is disabled

bit 0 **C0EN:** Dedicated ADC Core 0 Enable bits
1 = Dedicated ADC Core 0 is enabled
0 = Dedicated ADC Core 0 is disabled

REGISTER 22-30: ADCAL1H: ADC CALIBRATION REGISTER 1 HIGH

R/W-0, HS	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CSHRRDY	—	—	—	CSHRSKIP	CSHRDIFF	CSHREN	CSHRRUN
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSHRRDY:** Shared ADC Core Calibration Status Flag bit
1 = Shared ADC core calibration is finished
0 = Shared ADC core calibration is in progress

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CSHRSKIP:** Shared ADC Core Calibration Bypass bit
1 = After power-up, the shared ADC core will not be calibrated
0 = After power-up, the shared ADC core will be calibrated

bit 10 **CSHRDIFF:** Shared ADC Core Differential-Mode Calibration bit
1 = Shared ADC core will be calibrated in Differential Input mode
0 = Shared ADC core will be calibrated in Single-Ended Input mode

bit 9 **CSHREN:** Shared ADC Core Calibration Enable bit
1 = Shared ADC core calibration bits (CSHRRDY, CSHRSKIP, CSHRDIFF and CSHRRUN) can be accessed by software
0 = Shared ADC core calibration bits are disabled

bit 8 **CSHRRUN:** Shared ADC Core Calibration Start bit
1 = If this bit is set by software, the shared ADC core calibration cycle is started; this bit is cleared automatically by hardware
0 = Software can start the next calibration cycle

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 22-34: ADFLxCON: ADC DIGITAL FILTER x CONTROL REGISTER (x = 0 or 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0, HSC
FLEN	MODE1	MODE0	OVRSAM2	OVRSAM1	OVRSAM0	IE	RDY
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	FLCHSEL4	FLCHSEL3	FLCHSEL2	FLCHSEL1	FLCHSEL0
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLEN:** Filter Enable bit
1 = Filter is enabled
0 = Filter is disabled and the RDY bit is cleared

bit 14-13 **MODE<1:0>:** Filter Mode bits
11 = Averaging mode
10 = Reserved
01 = Reserved
00 = Oversampling mode

bit 12-10 **OVRSAM<2:0>:** Filter Averaging/Oversampling Ratio bits
If MODE<1:0> = 00:
111 = 128x (16-bit result in the ADFLxDAT register is in 12.4 format)
110 = 32x (15-bit result in the ADFLxDAT register is in 12.3 format)
101 = 8x (14-bit result in the ADFLxDAT register is in 12.2 format)
100 = 2x (13-bit result in the ADFLxDAT register is in 12.1 format)
011 = 256x (16-bit result in the ADFLxDAT register is in 12.4 format)
010 = 64x (15-bit result in the ADFLxDAT register is in 12.3 format)
001 = 16x (14-bit result in the ADFLxDAT register is in 12.2 format)
000 = 4x (13-bit result in the ADFLxDAT register is in 12.1 format)
If MODE<1:0> = 11 (12-bit result in the ADFLxDAT register in all instances):
111 = 256x
110 = 128x
101 = 64x
100 = 32x
011 = 16x
010 = 8x
001 = 4x
000 = 2x

bit 9 **IE:** Filter Common ADC Interrupt Enable bit
1 = Common ADC interrupt will be generated when the filter result will be ready
0 = Common ADC interrupt will not be generated for the filter

bit 8 **RDY:** Oversampling Filter Data Ready Flag bit
This bit is cleared by hardware when the result is read from the ADFLxDAT register.
1 = Data in the ADFLxDAT register is ready
0 = The ADFLxDAT register has been read and new data in the ADFLxDAT register is not ready

bit 7-5 **Unimplemented:** Read as '0'

NOTES:

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
	IIL	**Input Leakage Current(2,3)**					
DI50		I/O Pins 5V Tolerant(4)	-1	—	+1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance
DI51		I/O Pins Not 5V Tolerant(4)	-1	—	+1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance, -40°C ≤ TA ≤ +85°C
DI51a		I/O Pins Not 5V Tolerant(4)	-1	—	+1	µA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +85°C
DI51b		I/O Pins Not 5V Tolerant(4)	-1	—	+1	µA	VSS ≤ VPIN ≤ VDD, pin at high-impedance, -40°C ≤ TA ≤ +125°C
DI51c		I/O Pins Not 5V Tolerant(4)	-1	—	+1	µA	Analog pins shared with external reference pins, -40°C ≤ TA ≤ +125°C
DI55		$\overline{\text{MCLR}}$	-5	—	+5	µA	VSS ≤ VPIN ≤ VDD
DI56		OSC1	-5	—	+5	µA	VSS ≤ VPIN ≤ VDD, XT and HS modes

Note 1: Data in “Typ.” column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **“Pin Diagrams”** section for the 5V tolerant I/O pins.

5: VIL Source < (VSS – 0.3). Characterized but not tested.

6: VIH Source > (VDD + 0.3) for pins that are not 5V tolerant only.

7: Digital 5V tolerant pins do not have internal high-side diodes to VDD and cannot tolerate any “positive” input injection current.

8: Injection Currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

TABLE 30-52: ADC MODULE SPECIFICATIONS (CONTINUED)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[5] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typical**	**Max.**	**Units**	**Conditions**
ADC Accuracy: Single-Ended Input							
AD20b	Nr	Resolution	12			bits	
AD21b	INL	Integral Nonlinearity	> 5	—	< 5	LSb	AVSS = 0V, AVDD = 3.3V
AD22b	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	AVSS = 0V, AVDD = 3.3V **(Note 2)**
AD23b	GERR	Gain Error (Dedicated Core)	> 0	8	< 15	LSb	AVSS = 0V, AVDD = 3.3V
		Gain Error (Shared Core)	> 5	15	< 22	LSb	
AD24b	EOFF	Offset Error (Dedicated Core)	> 2	9	< 15	LSb	AVSS = 0V, AVDD = 3.3V
		Offset Error (Shared Core)	> 5	17	< 22	LSb	
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance							
AD31b	SINAD	Signal-to-Noise and Distortion	63	—	> 65	dB	**(Notes 3, 4)**
AD34b	ENOB	Effective Number of Bits	10.3	—	—	bits	**(Notes 3, 4)**

Note 1: These parameters are not characterized or tested in manufacturing.

2: No missing codes, limits based on characterization results.

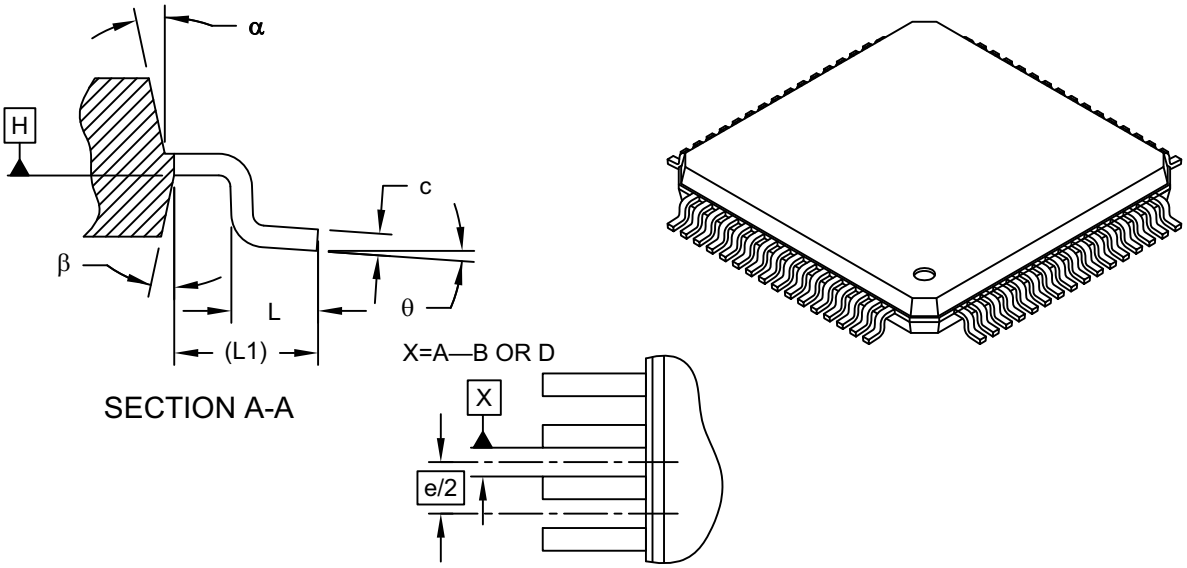
3: These parameters are characterized but not tested in manufacturing.

4: Characterized with a 15 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		64	
Lead Pitch	e		0.50 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	-	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-085C Sheet 2 of 2