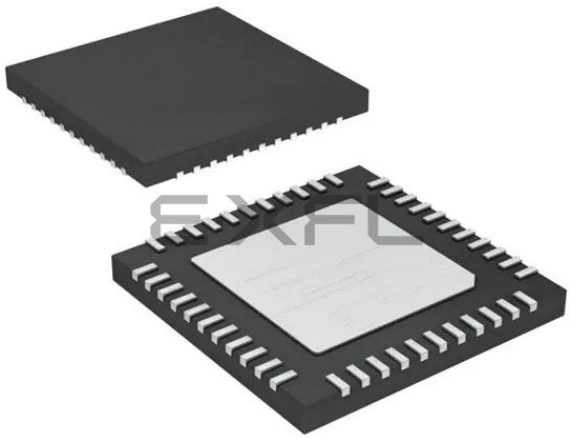
Microchip Technology - DSPIC33EP128GS704-E/ML Datasheet



Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

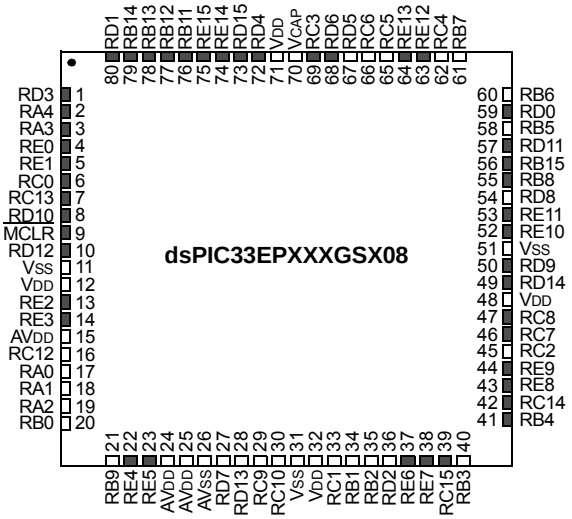
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs704-e-ml

Pin Diagrams (Continued)

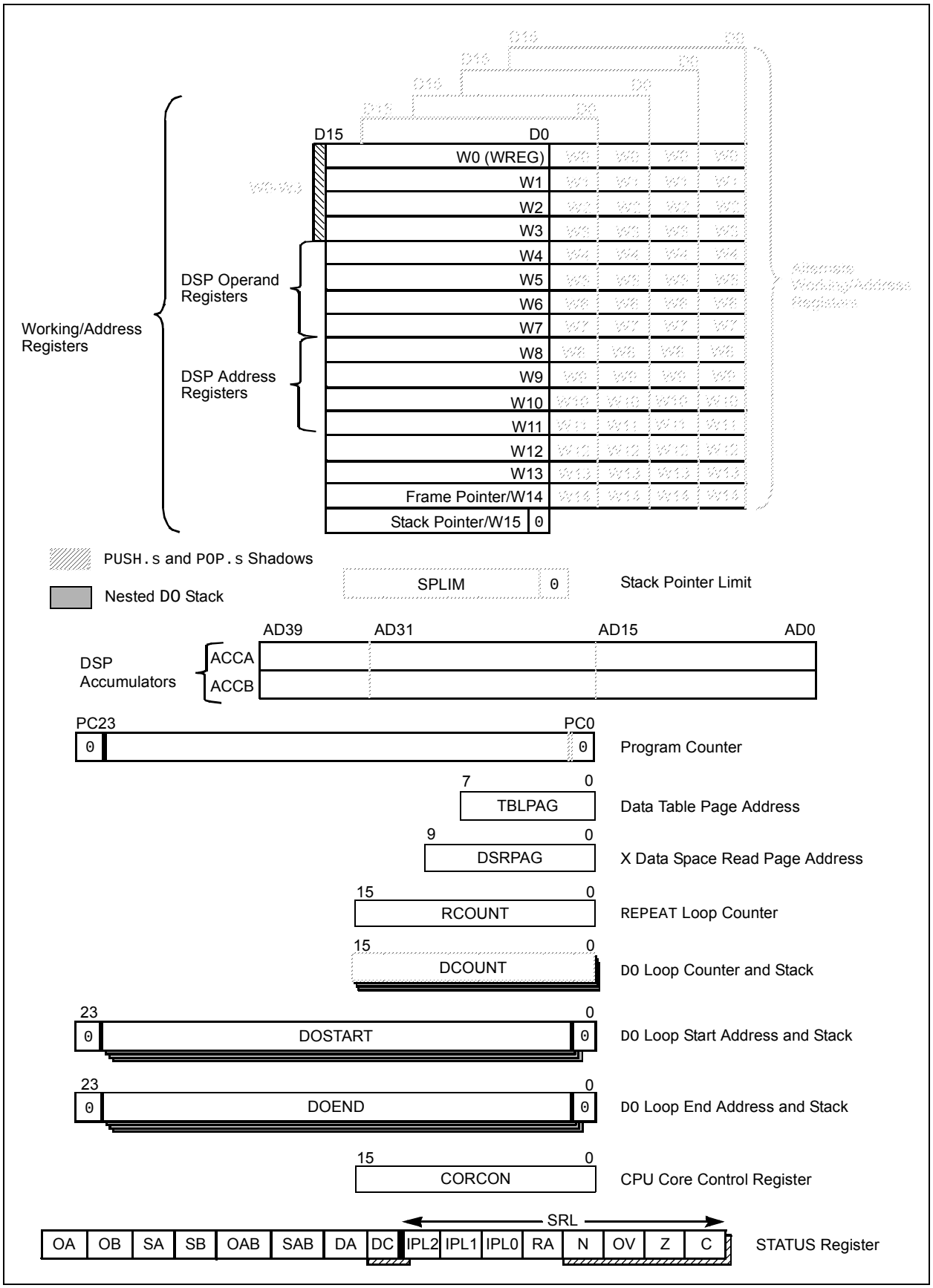
80-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PWM4L/**RP67**/RD3	41	PGEC2/ADTRG31/**RP36**/RB4
2	PWM1H/**RP20**/RA4	42	**RP62**/RC14
3	PWM1L/**RP19**/RA3	43	RE8
4	PWM8L/RE0	44	RE9
5	PWM8H/RE1	45	EXTREF1/AN9/CMP4D/**RP50**/RC2
6	FLT12/**RP48**/RC0	46	ASDA1/**RP55**/RC7
7	FLT11/**RP61**/RC13	47	ASCL1/**RP56**/RC8
8	CLC4OUT/FLT10/**RP74**/RD10	48	VDD
9	MCLR	49	CLC3OUT/RD14
10	T5CK/FLT9/**RP76**/RD12	50	SCK3/**RP73**/RD9
11	VSS	51	VSS
12	VDD	52	FLT21/RE10
13	FLT17/RE2	53	FLT22/RE11
14	FLT18/RE3	54	AN5/CMP2D/CMP3B/ISRC3/**RP72**/RD8
15	AVDD	55	PGED3/SDA2/FLT31/**RP40**/RB8
16	AN14/PGA2N3/**RP60**/RC12	56	PGEC3/SCL2/**RP47**/RB15
17	AN0/CMP1A/PGA1P1/**RP16**/RA0	57	INT4/**RP75**/RD11
18	AN1/CMP1B/PGA1P2/PGA2P1/**RP17**/RA1	58	TD0/AN19/PGA2N2/**RP37**/RB5
19	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/**RP18**/RA2	59	T4CK/**RP64**/RD0
20	AN3/CMP1D/CMP2B/PGA2P3/**RP32**/RB0	60	PGED1/TDI/AN20/SCL1/**RP38**/RB6
21	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9	61	PGEC1/AN21/SDA1/**RP39**/RB7
22	RE4	62	AN1ALT/**RP52**/RC4
23	RE5	63	RE12
24	AVDD	64	RE13
25	AVDD	65	AN0ALT/**RP53**/RC5
26	AVSS	66	AN17/**RP54**/RC6
27	AN15/**RP71**/RD7	67	AN12/ISRC1/**RP69**/RD5
28	DACOUT2/AN13/RD13	68	PWM5H/**RP70**/RD6
29	AN11/PGA1N3/**RP57**/RC9	69	PWM5L/**RP51**/RC3
30	EXTREF2/AN10/PGA1P4/**RP58**/RC10	70	VCAP
31	VSS	71	VDD
32	VDD	72	PWM6H/**RP68**/RD4
33	AN8/CMP4C/PGA2P4/**RP49**/RC1	73	PWM6L/RD15
34	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1	74	PWM7L/RE14
35	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/**RP34**/RB2	75	PWM7H/RE15
36	AN16/**RP66**/RD2	76	TMS/PWM3H/**RP43**/RB11
37	FLT19/RE6	77	TCK/PWM3L/**RP44**/RB12
38	FLT20/RE7	78	PWM2H/**RP45**/RB13
39	ASDA2/**RP63**/RC15	79	PWM2L/**RP46**/RB14
40	PGED2/DACOUT1/AN18/ASCL2/INT0/**RP35**/RB3	80	PWM4H/**RP65**/RD1

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 11-12 and Table 11-13 for the complete list of remappable sources.

FIGURE 3-2: PROGRAMMER'S MODEL



4.6.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note:	For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal

Note:	Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.6.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY.N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note:	Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

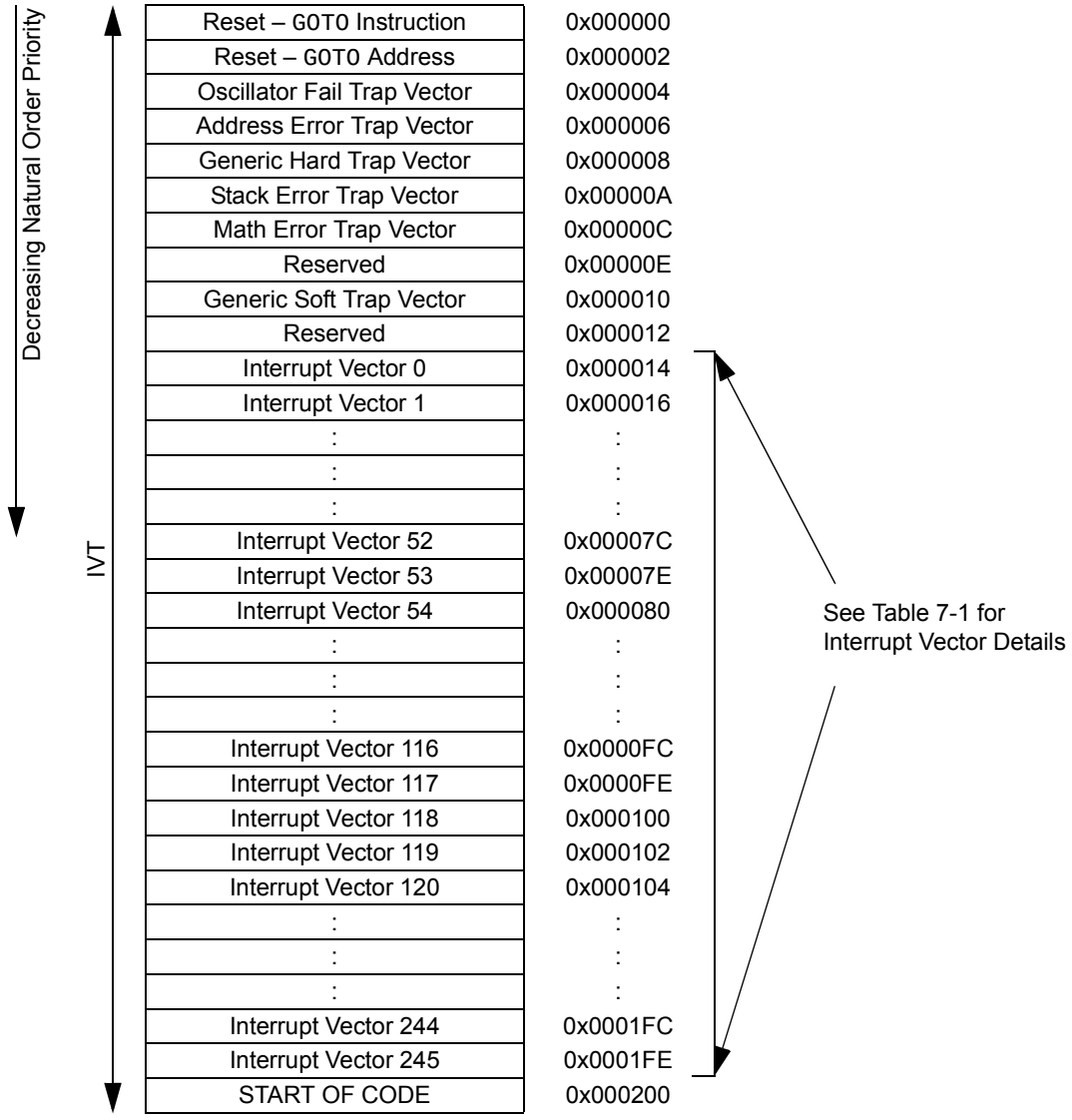
In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.6.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

FIGURE 7-1: dsPIC33EPXXXGS70X/80X FAMILY INTERRUPT VECTOR TABLE



Note: In Dual Partition Flash modes, each partition has a dedicated Interrupt Vector Table.

In addition, DMA transfers can be triggered by timers as well as external interrupts. Each DMA channel is unidirectional. Two DMA channels must be allocated to read and write to a peripheral. If more than one channel receives a request to transfer data, a simple fixed priority scheme, based on channel number, dictates which channel completes the transfer and which channel, or channels, are left pending. Each DMA channel moves a block of data, after which, it generates an interrupt to the CPU to indicate that the block is available for processing.

The DMA Controller provides these functional capabilities:

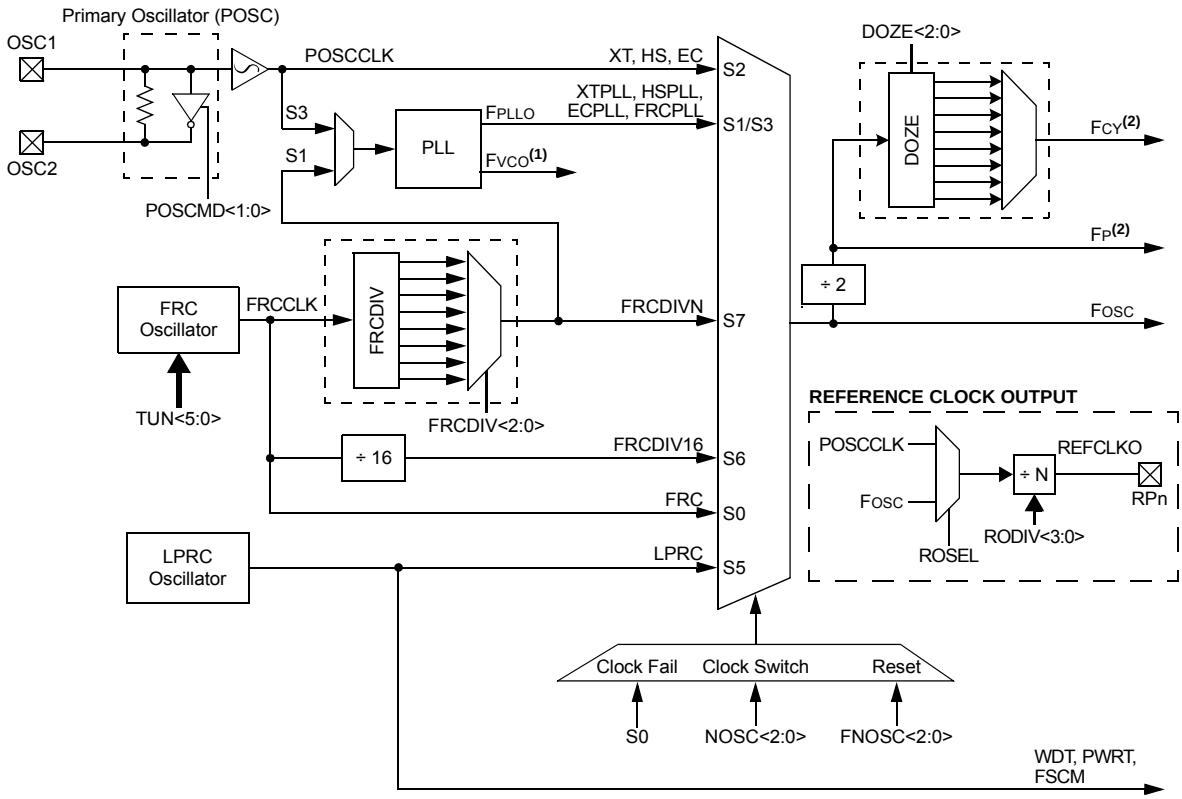
- Four DMA Channels
- Register Indirect with Post-Increment Addressing mode
- Register Indirect without Post-Increment Addressing mode
- Peripheral Indirect Addressing mode (peripheral generates destination address)
- CPU Interrupt after Half or Full Block Transfer Complete
- Byte or Word Transfers
- Fixed Priority Channel Arbitration
- Manual (software) or Automatic (peripheral DMA requests) Transfer Initiation
- One-Shot or Auto-Repeat Block Transfer modes
- Ping-Pong mode (automatic switch between two SRAM Start addresses after each block transfer complete)
- DMA Request for each Channel can be Selected from any Supported Interrupt Source
- Debug Support Features

The peripherals that can utilize DMA are listed in Table 8-1.

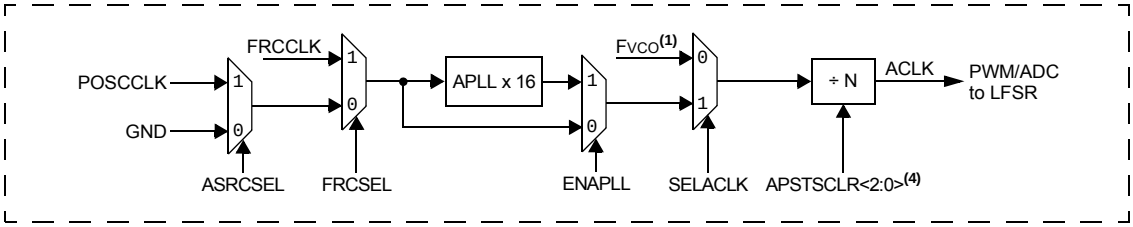
TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
INT0 – External Interrupt 0	00000000	—	—
IC1 – Input Capture 1	00000001	0x0144 (IC1BUF)	—
IC2 – Input Capture 2	00000101	0x014C (IC2BUF)	—
IC3 – Input Capture 3	00100101	0x0154 (IC3BUF)	—
IC4 – Input Capture 4	00100110	0x015C (IC4BUF)	—
OC1 – Output Compare 1	00000010	—	0x0906 (OC1R) 0x0904 (OC1RS)
OC2 – Output Compare 2	00000110	—	0x0910 (OC2R) 0x090E (OC2RS)
OC3 – Output Compare 3	00011001	—	0x091A (OC3R) 0x0918 (OC3RS)
OC4 – Output Compare 4	00011010	—	0x0924 (OC4R) 0x0922 (OC4RS)
TMR2 – Timer2	00000111	—	—
TMR3 – Timer3	00001000	—	—
TMR4 – Timer4	00011011	—	—
TMR5 – Timer5	00011100	—	—
UART1RX – UART1 Receiver	00001011	0x0226 (U1RXREG)	—
UART1TX – UART1 Transmitter	00001100	—	0x0224 (U1TXREG)
UART2RX – UART2 Receiver	00011110	0x0236 (U2RXREG)	—
UART2TX – UART2 Transmitter	00011111	—	0x0234 (U2TXREG)
CAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
CAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
CAN2 – RX Data Ready	00110111	0X0540(C2RXD)	—
CAN2 – TX Data Request	01000111	—	0X0542(C2TXD)

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



AUXILIARY CLOCK GENERATOR CIRCUIT BLOCK DIAGRAM



Note 1: See Figure 9-2 for the source of the FVCO signal.

2: FP refers to the clock source for all the peripherals, while FCY (or MIPS) refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used in any ratio other than 1:1.

3: The auxiliary clock postscaler must be configured to divide-by-1 (APSTSCLR<2:0> = 111) for proper operation of the PWM and ADC modules.

REGISTER 11-37: RPOR4: PERIPHERAL PIN SELECT OUTPUT REGISTER 4

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP36R6	RP36R5	RP36R4	RP36R3	RP36R2	RP36R1	RP36R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP35R6	RP35R5	RP35R4	RP35R3	RP35R2	RP35R1	RP35R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP36R<6:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP35R<6:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-38: RPOR5: PERIPHERAL PIN SELECT OUTPUT REGISTER 5

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP38R6	RP38R5	RP38R4	RP38R3	RP38R2	RP38R1	RP38R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP37R6	RP37R5	RP37R4	RP37R3	RP37R2	RP37R1	RP37R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP38R<6:0>:** Peripheral Output Function is Assigned to RP38 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP37R<6:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-59: RPOR26: PERIPHERAL PIN SELECT OUTPUT REGISTER 26

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP181R6	RP181R5	RP181R4	RP181R3	RP181R2	RP181R1	RP181R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP180R6	RP180R5	RP180R4	RP180R3	RP180R2	RP180R1	RP180R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP181R<6:0>:** Peripheral Output Function is Assigned to RP181 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP180R<6:0>:** Peripheral Output Function is Assigned to RP180 Output Pin bits (see Table 11-13 for peripheral function numbers)

16.0 HIGH-SPEED PWM

Note: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"High-Speed PWM Module"** (DS70000323) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

The high-speed PWM on dsPIC33EPXXXGS70X/80X devices supports a wide variety of PWM modes and output formats. This PWM module is ideal for power conversion applications, such as:

- AC/DC Converters
- DC/DC Converters
- Power Factor Correction
- Uninterruptible Power Supply (UPS)
- Inverters
- Battery Chargers
- Digital Lighting

16.1 Features Overview

The high-speed PWM module incorporates the following features:

- Eight PWMx Generators with Two Outputs per Generator
- Two Master Time Base modules
- Individual Time Base and Duty Cycle for each PWM Output
- Duty Cycle, Dead Time, Phase Shift and a Frequency Resolution of 1.04 ns
- Independent Fault and Current-Limit Inputs
- Redundant Output
- True Independent Output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Dual Trigger from PWMx to Analog-to-Digital Converter (ADC)
- PWMxL and PWMxH Output Pin Swapping
- Independent PWMx Frequency, Duty Cycle and Phase-Shift Changes
- Enhanced Leading-Edge Blanking (LEB) Functionality
- PWM Capture Functionality

Note: Duty cycle, dead time, phase shift and frequency resolution is 8.32 ns in Center-Aligned PWM mode.

Figure 16-1 conceptualizes the PWM module in a simplified block diagram. Figure 16-2 illustrates how the module hardware is partitioned for each PWMx output pair for the Complementary PWM mode.

The PWM module contains eight PWM generators. The module has up to 16 PWMx output pins: PWM1H/PWM1L through PWM8H/PWM8L. For complementary outputs, these 16 I/O pins are grouped into high/low pairs. PWM1 through PWM6 can be used to trigger an ADC conversion.

16.2 Feature Description

The PWM module is designed for applications that require:

- High resolution at high PWM frequencies
- The ability to drive Standard, Edge-Aligned, Center-Aligned Complementary mode and Push-Pull mode outputs
- The ability to create multiphase PWM outputs

Two common, medium power converter topologies are push-pull and half-bridge. These designs require the PWM output signal to be switched between alternate pins, as provided by the Push-Pull PWM mode.

Phase-shifted PWM describes the situation where each PWM generator provides outputs, but the phase relationship between the generator outputs is specifiable and changeable.

Multiphase PWM is often used to improve DC/DC Converter load transient response, and reduce the size of output filter capacitors and inductors. Multiple DC/DC Converters are often operated in parallel, but phase shifted in time. A single PWM output, operating at 250 kHz, has a period of 4 μs but an array of four PWM channels, staggered by 1 μs each, yields an effective switching frequency of 1 MHz. Multiphase PWM applications typically use a fixed-phase relationship.

Variable phase PWM is useful in Zero Voltage Transition (ZVT) power converters. Here, the PWM duty cycle is always 50% and the power flow is controlled by varying the relative phase shift between the two PWM generators.

REGISTER 17-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER(1,2) (CONTINUED)

bit 4 **OC1CS:** Clock Source for OC1 bit
1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 3 **OC4TSS:** Trigger/Synchronization Source for OC4 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 2 **OC3TSS:** Trigger/Synchronization Source for OC3 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 1 **OC2TSS:** Trigger/Synchronization Source for OC2 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 0 **OC1TSS:** Trigger/Synchronization Source for OC1 bit
1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

REGISTER 19-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 6 **STREN:** SCLx Clock Stretch Enable bit (when operating as I^2C slave)
Used in conjunction with the SCLREL bit.
1 = Enables software or receives clock stretching
0 = Disables software or receives clock stretching

bit 5 **ACKDT:** Acknowledge Data bit (when operating as I^2C master, applicable during master receive)
Value that is transmitted when the software initiates an Acknowledge sequence.
1 = Sends NACK during Acknowledge
0 = Sends ACK during Acknowledge

bit 4 **ACKEN:** Acknowledge Sequence Enable bit
(when operating as I^2C master, applicable during master receive)
1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence
0 = Acknowledge sequence is not in progress

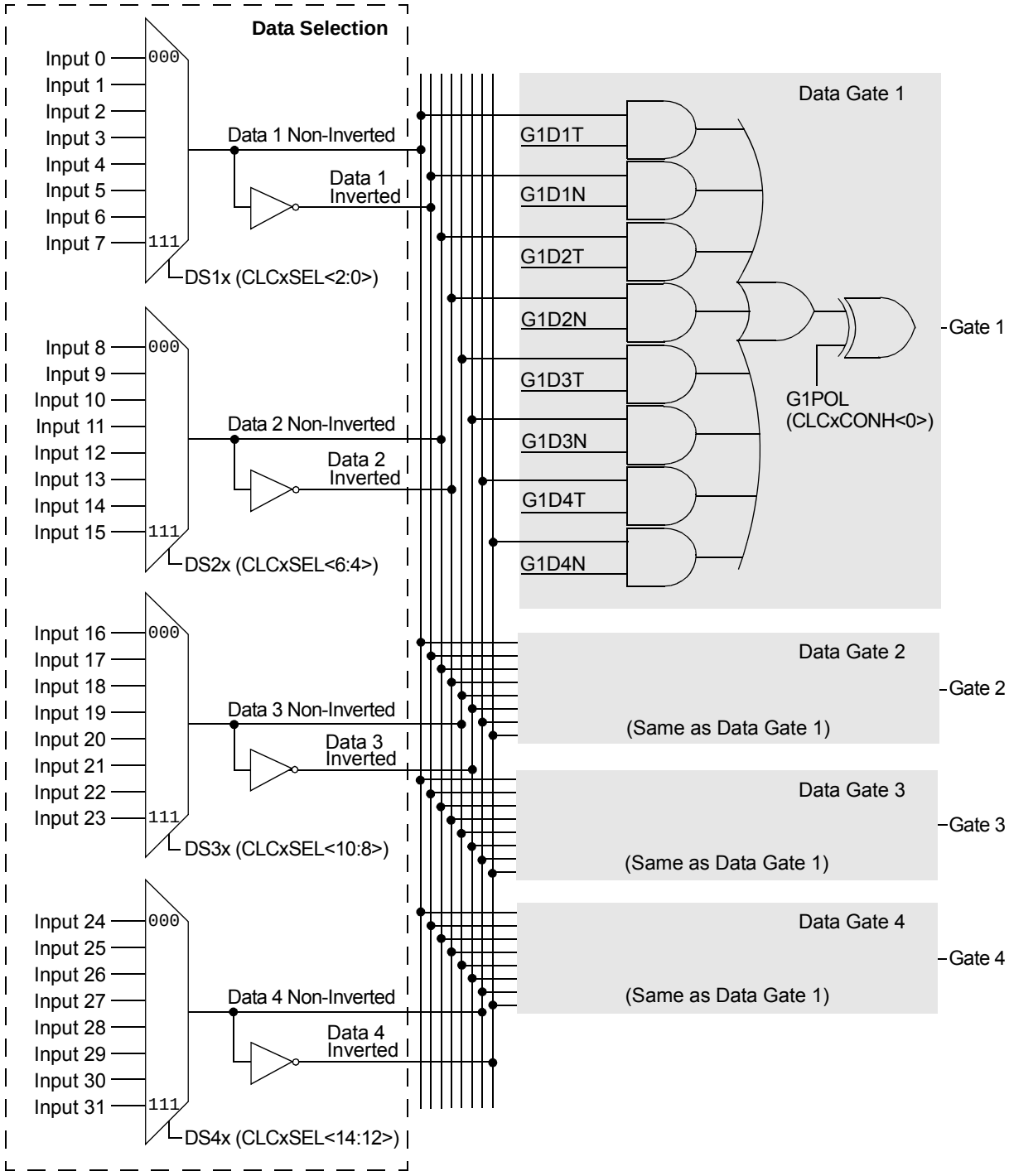
bit 3 **RCEN:** Receive Enable bit (when operating as I^2C master)
1 = Enables Receive mode for I^2C; hardware is clear at the end of the eighth bit of the master receive data byte
0 = Receive sequence is not in progress

bit 2 **PEN:** Stop Condition Enable bit (when operating as I^2C master)
1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
0 = Stop condition is not in progress

bit 1 **RSEN:** Repeated Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
0 = Repeated Start condition is not in progress

bit 0 **SEN:** Start Condition Enable bit (when operating as I^2C master)
1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence
0 = Start condition is not in progress

FIGURE 21-3: CLCx INPUT SOURCE SELECTION DIAGRAM



Note: All controls are undefined at power-up.

REGISTER 21-1: CLCxCONL: CLCx CONTROL REGISTER (LOW) (CONTINUED)

bit 2-0 **MODE<2:0>:** CLCx Mode bits
111 = Single Input Transparent Latch with S and R
110 = JK Flip-Flop with R
101 = Two-Input D Flip-Flop with R
100 = Single Input D Flip-Flop with S and R
011 = SR Latch
010 = Four-Input AND
001 = Four-Input OR-XOR
000 = Four-Input AND-OR

REGISTER 21-2: CLCxCONH: CLCx CONTROL REGISTER (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	G4POL	G3POL	G2POL	G1POL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

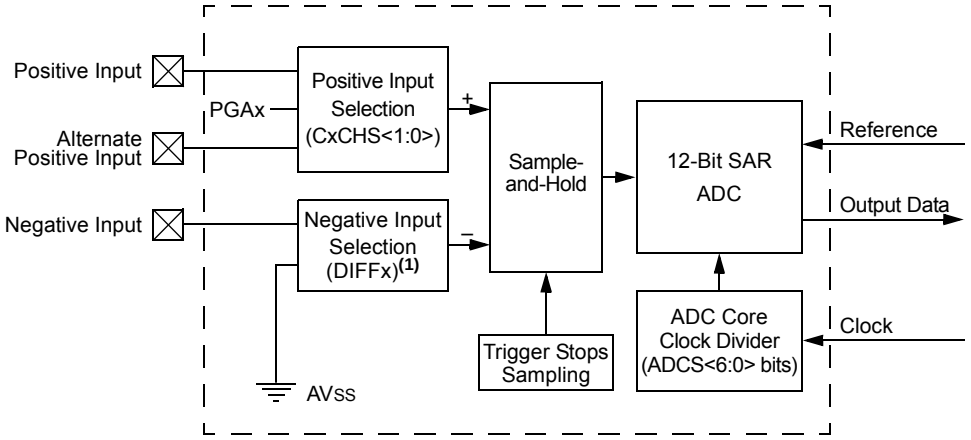
bit 3 **G4POL:** Gate 4 Polarity Control bit
1 = Channel 4 logic output is inverted when applied to the logic cell
0 = Channel 4 logic output is not inverted

bit 2 **G3POL:** Gate 3 Polarity Control bit
1 = Channel 3 logic output is inverted when applied to the logic cell
0 = Channel 3 logic output is not inverted

bit 1 **G2POL:** Gate 2 Polarity Control bit
1 = Channel 2 logic output is inverted when applied to the logic cell
0 = Channel 2 logic output is not inverted

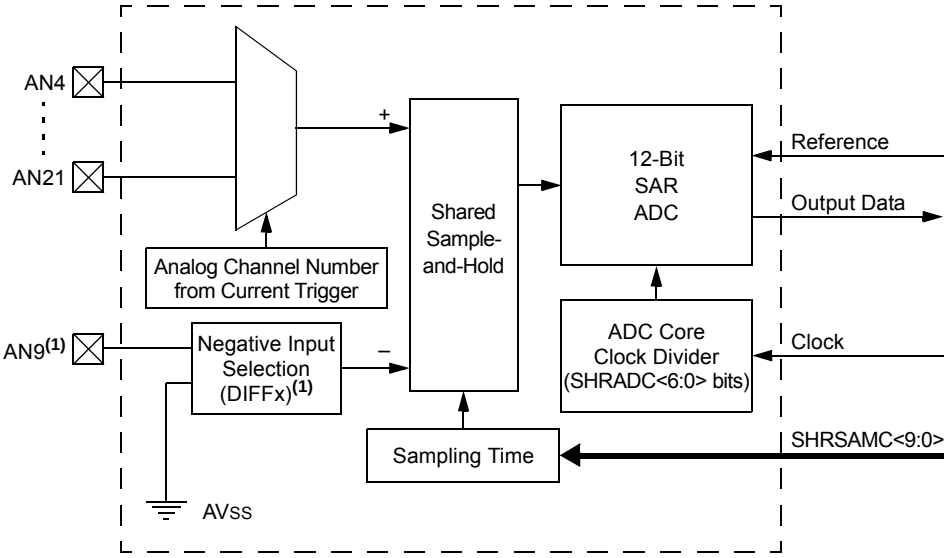
bit 0 **G1POL:** Gate 1 Polarity Control bit
1 = Channel 1 logic output is inverted when applied to the logic cell
0 = Channel 1 logic output is not inverted

FIGURE 22-2: DEDICATED ADC CORES 0 TO 3 BLOCK DIAGRAM



Note 1: The DIFFx bit for the corresponding positive input channel must be set in order to use the negative differential input.

FIGURE 22-3: SHARED ADC CORE BLOCK DIAGRAM



Note 1: Differential-mode conversion is not available for the shared ADC core in dsPIC33EPXXGS70X/80X devices. For all other devices, the DIFFx bit for the corresponding positive input channel must be set to use AN9 as the negative differential input.

REGISTER 22-29: ADCAL0H: ADC CALIBRATION REGISTER 0 HIGH

R-0, HSC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL3RDY	—	—	—	CAL3SKIP	CAL3DIFF	CAL3EN	CAL3RUN
bit 15							bit 8

R-0, HSC	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CAL2RDY	—	—	—	CAL2SKIP	CAL2DIFF	CAL2EN	CAL2RUN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CAL3RDY:** Dedicated ADC Core 3 Calibration Status Flag bit
1 = Dedicated ADC Core 3 calibration is finished
0 = Dedicated ADC Core 3 calibration is in progress

bit 14-12 **Unimplemented:** Read as '0'

bit 11 **CAL3SKIP:** Dedicated ADC Core 3 Calibration Bypass bit
1 = After power-up, the dedicated ADC Core 3 will not be calibrated
0 = After power-up, the dedicated ADC Core 3 will be calibrated

bit 10 **CAL3DIFF:** Dedicated ADC Core 3 Differential-Mode Calibration bit
1 = Dedicated ADC Core 3 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 3 will be calibrated in Single-Ended Input mode

bit 9 **CAL3EN:** Dedicated ADC Core 3 Calibration Enable bit
1 = Dedicated ADC Core 3 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 3 calibration bits are disabled

bit 8 **CAL3RUN:** Dedicated ADC Core 3 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 3 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

bit 7 **CAL2RDY:** Dedicated ADC Core 2 Calibration Status Flag bit
1 = Dedicated ADC Core 2 calibration is finished
0 = Dedicated ADC Core 2 calibration is in progress

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **CAL2SKIP:** Dedicated ADC Core 2 Calibration Bypass bit
1 = After power-up, the dedicated ADC Core 2 will not be calibrated
0 = After power-up, the dedicated ADC Core 2 will be calibrated

bit 2 **CAL2DIFF:** Dedicated ADC Core 2 Differential-Mode Calibration bit
1 = Dedicated ADC Core 2 will be calibrated in Differential Input mode
0 = Dedicated ADC Core 2 will be calibrated in Single-Ended Input mode

bit 1 **CAL2EN:** Dedicated ADC Core 2 Calibration Enable bit
1 = Dedicated ADC Core 2 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software
0 = Dedicated ADC Core 2 calibration bits are disabled

bit 0 **CAL2RUN:** Dedicated ADC Core 2 Calibration Start bit
1 = If this bit is set by software, the dedicated ADC Core 2 calibration cycle is started; this bit is automatically cleared by hardware
0 = Software can start the next calibration cycle

REGISTER 23-11: CxFEN1: CANx ACCEPTANCE FILTER ENABLE REGISTER 1

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN<15:8>							
bit 15							bit 8

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
FLTEN<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **FLTEN<15:0>:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n

REGISTER 23-12: CxBUFPNT1: CANx FILTERS 0-3 BUFFER POINTER REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bits 15-12)

bit 7-4 **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bits 15-12)

bit 3-0 **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bits 15-12)

27.7 JTAG Interface

The dsPIC33EPXXXGS70X/80X family devices implement a JTAG interface, which supports boundary scan device testing. Detailed information on this interface is provided in future revisions of the document.

Note: Refer to **"Programming and Diagnostics"** (DS70608) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of the JTAG interface.

27.8 In-Circuit Serial Programming™ (ICSP™)

The dsPIC33EPXXXGS70X/80X family devices can be serially programmed while in the end application circuit. This is done with two lines for clock and data, and three other lines for power, ground and the programming sequence. Serial programming allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. Serial programming also allows the most recent firmware or a custom firmware to be programmed. Refer to the *"dsPIC33E/PIC24E Flash Programming Specification for Devices with Volatile Configuration Bits"* (DS70663) for details about In-Circuit Serial Programming™ (ICSP™).

Any of the three pairs of programming clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

27.9 In-Circuit Debugger

When MPLAB® ICD 3 or REAL ICE™ emulator is selected as a debugger, the in-circuit debugging functionality is enabled. This function allows simple debugging functions when used with MPLAB IDE. Debugging functionality is controlled through the PGECx (Emulation/Debug Clock) and PGEDx (Emulation/Debug Data) pin functions.

Any of the three pairs of debugging clock/data pins can be used:

- PGEC1 and PGED1
- PGEC2 and PGED2
- PGEC3 and PGED3

To use the in-circuit debugger function of the device, the design must implement ICSP connections to $\overline{MCLR}$, V_{DD}, V_{SS} and the PGECx/PGEDx pin pair. In addition, when the feature is enabled, some of the resources are not available for general use. These resources include the first 80 bytes of data RAM and two I/O pins (PGECx and PGEDx).

27.10 Code Protection and CodeGuard™ Security

dsPIC33EPXXXGS70X/80X devices offer multiple levels of security for protecting individual intellectual property. The program Flash protection can be broken up into three segments: Boot Segment (BS), General Segment (GS) and Configuration Segment (CS). Boot Segment has the highest security privilege and can be thought to have limited restrictions when accessing other segments. General Segment has the least security and is intended for the end user system code. Configuration Segment contains only the device user configuration data which is located at the end of the program memory space.

The code protection features are controlled by the Configuration registers, FSEC and FBSLIM. The FSEC register controls the code-protect level for each segment and if that segment is write-protected. The size of BS and GS will depend on the BSLIM<12:0> bits setting and if the Alternate Interrupt Vector Table (AIVT) is enabled. The BSLIM<12:0> bits define the number of pages for BS with each page containing 512 IW. The smallest BS size is one page, which will consist of the Interrupt Vector Table (IVT) and 256 IW of code protection.

If the AIVT is enabled, the last page of BS will contain the AIVT and will not contain any BS code. With AIVT enabled, the smallest BS size is now two pages (1024 IW), with one page for the IVT and BS code, and the other page for the AIVT. Write protection of the BS does not cover the AIVT. The last page of BS can always be programmed or erased by BS code. The General Segment will start at the next page and will consume the rest of program Flash except for the Flash Configuration Words. The IVT will assume GS security only if BS is not enabled. The IVT is protected from being programmed or page erased when either security segment has enabled write protection.

Note: Refer to **"CodeGuard™ Intermediate Security"** (DS70005182) in the *"dsPIC33/PIC24 Family Reference Manual"* for further information on usage, configuration and operation of CodeGuard Security.

TABLE 30-43: SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING REQUIREMENTS(5)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK3 Input Frequency	—	—	25	MHz	**(Note 3)**
SP72	TscF	SCK3 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK3 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO3 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO3 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO3 Data Output Valid after SCK3 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO3 Data Output Setup to First SCK3 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI3 Data Input to SCK3 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI3 Data Input to SCK3 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS3}$ ↓ to SCK3 ↑ or SCK3 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS3}$ ↑ to SDO3 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH TscL2ssH	$\overline{SS3}$ ↑ after SCK3 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**
SP60	TssL2doV	SDO3 Data Output Valid after $\overline{SS3}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

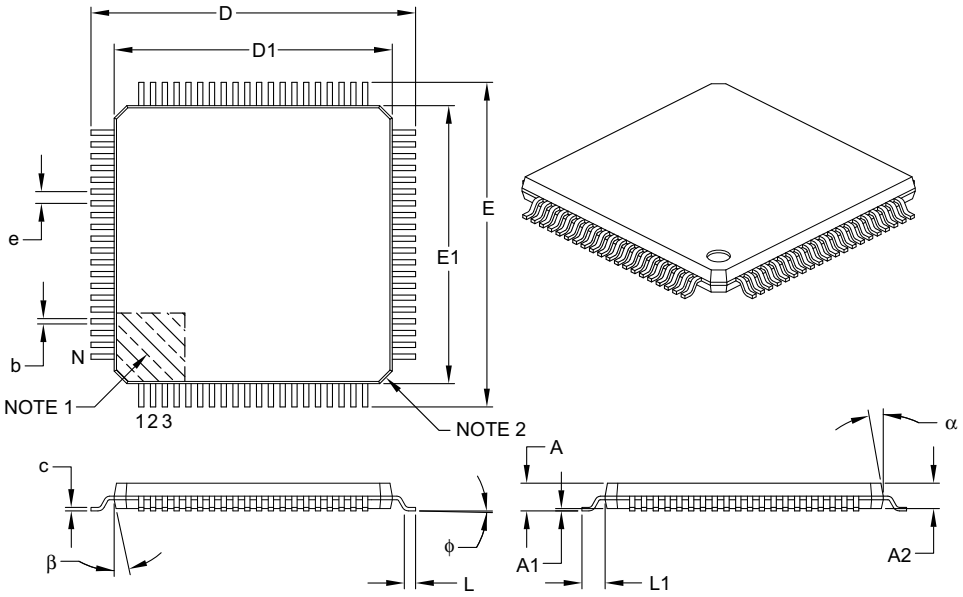
3: The minimum clock period for SCK3 is 66.7 ns. Therefore, the SCK3 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI3 pins.

5: For dsPIC33EPXXXGSX06 and dsPIC33EPXXXGSX08 devices with a fixed SCK3 pin.

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B