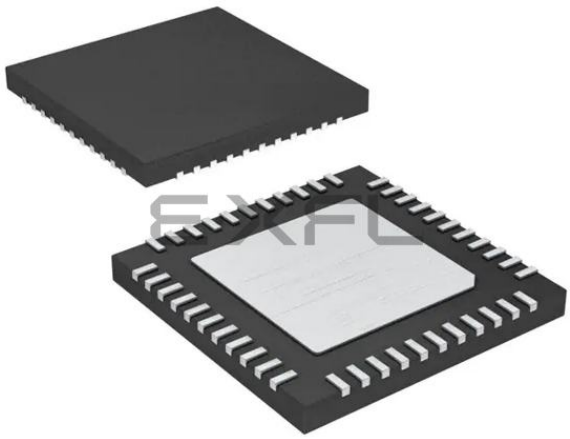
Microchip Technology - DSPIC33EP128GS704-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs704-i-ml

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
CMP1A-CMP4A	I	Analog	No	Comparator Channels 1A through 4A inputs.
CMP1B-CMP4B	I	Analog	No	Comparator Channels 1B through 4B inputs.
CMP1C-CMP4C	I	Analog	No	Comparator Channels 1C through 4C inputs.
CMP1D-CMP4D	I	Analog	No	Comparator Channels 1D through 4D inputs.
ACMP1-ACMP4	O	—	Yes	Analog Comparator Outputs 1-4.
DACOUT1, DACOUT2	O	—	No	DAC Output Voltages 1 and 2.
EXTREF1, EXTREF2	I	Analog	No	External Voltage Reference Inputs 1 and 2 for the Reference DACs.
PGA1P1-PGA1P4	I	Analog	No	PGA1 Positive Inputs 1 through 4.
PGA1N1-PGA1N3	I	Analog	No	PGA1 Negative Inputs 1 through 3.
PGA2P1-PGA2P4	I	Analog	No	PGA2 Positive Inputs 1 through 4.
PGA2N1-PGA2N3	I	Analog	No	PGA2 Negative Inputs 1 through 3.
ADTRG31	I	ST	No	External ADC trigger source.
PGED1	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 1.
PGEC1	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 1.
PGED2	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 2.
PGEC2	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 2.
PGED3	I/O	ST	No	Data I/O pin for Programming/Debugging Communication Channel 3.
PGEC3	I	ST	No	Clock input pin for Programming/Debugging Communication Channel 3.
$\overline{MCLR}$	I/P	ST	No	Master Clear (Reset) input. This pin is an active-low Reset to the device.
AV_{DD}	P	P	No	Positive supply for analog modules. This pin must be connected at all times.
AV_{SS}	P	P	No	Ground reference for analog modules. This pin must be connected at all times.
V_{DD}	P	—	No	Positive supply for peripheral logic and I/O pins.
V_{CAP}	P	—	No	CPU logic filter capacitor connection.
V_{SS}	P	—	No	Ground reference for logic and I/O pins.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

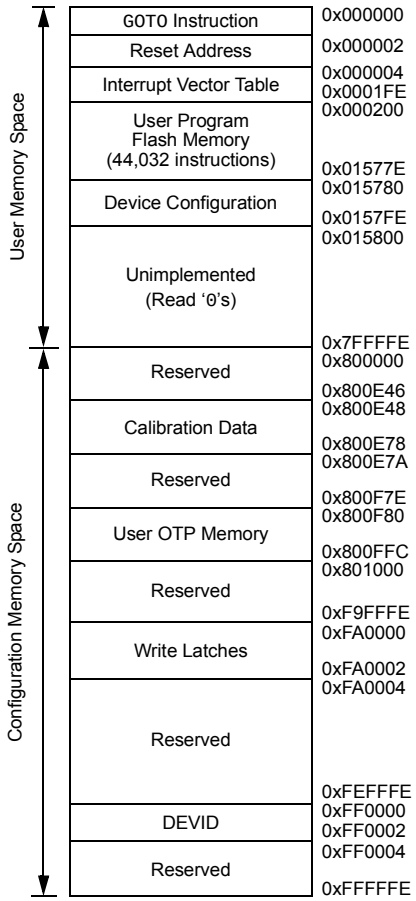
1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4H/L through PWM8H/L are fixed on dsPIC33EPXXXGS708/808 devices. PWM4H/L through PWM6H/L are fixed on dsPIC33EPXXXGS706/806 devices.

3: The SCK3 pin is fixed on dsPIC33EPXXXGS706/806 and dsPIC33EPXXXGS708/808 devices.

4: PPS is available on dsPIC33EPXXXGS702 devices only.

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP128GS70X/80X DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-10: SFR BLOCK 800h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Interrupt Controller			IEC9	832	0000000000000000	IPC26	874	0000000001000100
IFS0	800	0000000000000000	IEC10	834	0000000000000000	IPC27	876	0100010000000000
IFS1	802	0000000000000000	IEC11	836	0000000000000000	IPC28	878	0100010001000100
IFS2	804	0000000000000000	IPC0	840	0100010001000100	IPC29	87A	0000000001000100
IFS3	806	0000000000000000	IPC1	842	0100010001000000	IPC35	886	0100010000000000
IFS4	808	0000000000000000	IPC2	844	0100010001000100	IPC36	888	0000000000000000
IFS5	80A	0000000000000000	IPC3	846	0100000001000100	IPC37	88A	0100000000000000
IFS6	80C	0000000000000000	IPC4	848	0100010001000100	IPC38	88C	0100010001000100
IFS7	80E	0000000000000000	IPC5	84A	0000000000000100	IPC39	88E	0100010001000100
IFS8	810	0000000000000000	IPC6	84C	0100010001000000	IPC40	890	0100010001000100
IFS9	812	0000000000000000	IPC7	84E	0100010001000100	IPC41	892	0100010001000100
IFS10	814	0000000000000000	IPC8	850	0000000001000100	IPC42	894	0000000001000100
IFS11	816	0000000000000000	IPC9	852	0000010001000000	IPC43	896	0000010001000000
IEC0	820	0000000000000000	IPC11	856	0000000000000000	IPC44	898	0100010001000000
IEC1	822	0000000000000000	IPC12	858	0000010001000000	IPC45	89A	0000000000000100
IEC2	824	0000000000000000	IPC13	85A	0000010000000000	IPC46	89C	0100010000000000
IEC3	826	0000000000000000	IPC14	85C	0000000001000000	IPC47	89E	0000010001000100
IEC4	828	0000000000000000	IPC16	860	0000010001000000	INTCON1	8C0	0000000000000000
IEC5	82A	0000000000000000	IPC18	864	0000000001000000	INTCON2	8C2	0000000000000000
IEC6	82C	0000000000000000	IPC23	86E	0100010000000000	INTCON3	8C4	0000000000000000
IEC7	82E	0000000000000000	IPC24	870	0000010001000100	INTCON4	8C6	0000000000000000
IEC8	830	0000000000000000	IPC25	872	0100000000000000	INTTREG	8C8	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-11: SFR BLOCK 900h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Output Compare			OC3R	91A	xxxxxxxxxxxxxxxx	CLC2CONH	9CE	0000000000000000
OC1CON1	900	0000000000000000	OC3TMR	91C	0000000000000000	CLC2SEL	9D0	0000000000000000
OC1CON2	902	0000000000001100	OC4CON1	91E	0000000000000000	CLC2GLSL	9D4	0000000000000000
OC1RS	904	xxxxxxxxxxxxxxxx	OC4CON2	920	0000000000001100	CLC2GLSH	9D6	0000000000000000
OC1R	906	xxxxxxxxxxxxxxxx	OC4RS	922	xxxxxxxxxxxxxxxx	CLC3CONL	9D8	0000000000000000
OC1TMR	908	0000000000000000	OC4R	924	xxxxxxxxxxxxxxxx	CLC3CONH	9DA	0000000000000000
OC2CON1	90A	0000000000000000	OC4TMR	926	0000000000000000	CLC3SEL	9DC	0000000000000000
OC2CON2	90C	0000000000001100	**CLC**			CLC3GLSL	9E0	0000000000000000
OC2RS	90E	xxxxxxxxxxxxxxxx	CLC1CONL	9C0	0000000000000000	CLC3GLSH	9E2	0000000000000000
OC2R	910	xxxxxxxxxxxxxxxx	CLC1CONH	9C2	0000000000000000	CLC4CONL	9E4	0000000000000000
OC2TMR	912	0000000000000000	CLC1SEL	9C4	0000000000000000	CLC4CONH	9E6	0000000000000000
OC3CON1	914	0000000000000000	CLC1GLSL	9C8	0000000000000000	CLC4SEL	9E8	0000000000000000
OC3CON2	916	0000000000001100	CLC1GLSH	9CA	0000000000000000	CLC4GLSL	9EC	0000000000000000
OC3RS	918	xxxxxxxxxxxxxxxx	CLC2CONL	9CC	0000000000000000	CLC4GLSH	9EE	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

4.7 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.7.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-2).

Note:	Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.7.2 W ADDRESS REGISTER SELECTION

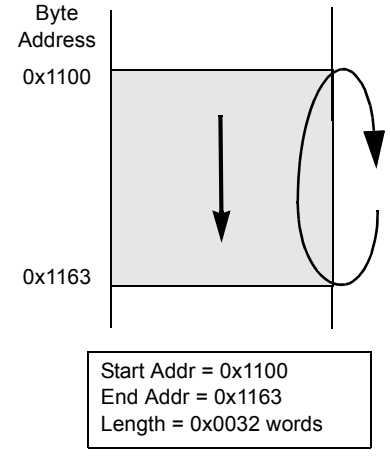
The Modulo and Bit-Reversed Addressing Control register, MODCON<15:0>, contains enable flags, as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W (XWM) register, to which Modulo Addressing is to be applied, is stored in MODCON<3:0> (see Table 4-2). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than ‘1111’ and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W (YWM) register, to which Modulo Addressing is to be applied, is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than ‘1111’ and the YMODEN bit (MODCON<14>) is set.

FIGURE 4-10: MODULO ADDRESSING OPERATION EXAMPLE




```
MOV     #0x1100, W0
MOV     W0, XMODSRT     ;set modulo start address
MOV     #0x1163, W0
MOV     W0, MODEND      ;set modulo end address
MOV     #0x8001, W0
MOV     W0, MODCON      ;enable W1, X AGU for modulo

MOV     #0x0000, W0     ;W0 holds buffer fill value

MOV     #0x1110, W1     ;point W1 to buffer

DO      AGAIN, #0x31    ;fill the 50 buffer locations
MOV     W0, [W1++]      ;fill the next location
AGAIN:  INC W0, W0      ;increment the fill value
```

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
T4 – Timer4	35	27	0x00004A	IFS1<11> T4IF	IEC1<11> T4IE	IPC6<14:12> T4IP<2:0>
T5 – Timer5	36	28	0x00004C	IFS1<12> T5IF	IEC1<12> T5IE	IPC7<2:0> T5IP<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13> INT2IF	IEC1<13> INT2IE	IPC7<6:4> INT2IP<2:0>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14> U2RXIF	IEC1<14> U2RXIE	IPC7<10:8> U2RXIP<2:0>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15> U2TXIF	IEC1<15> U2TXIE	IPC7<14:12> U2TXIP<2:0>
SPI2TX – SPI2 Transfer Done	40	32	0x000054	IFS2<0> SPI2TXIF	IEC2<0> SPI2TXIE	IPC8<2:0> SPI2TXIP<2:0>
SPI2RX – SPI2 Receive Done	41	33	0x000056	IFS2<1> SPI2RXIF	IEC2<1> SPI2RXIE	IPC8<6:4> SPI2RXIP<2:0>
C1RX – CAN1 RX Data Ready	42	34	0x000058	IFS2<2> C1RXIF	IEC2<2> C1RXIE	IPC8<10:8> C1RXIP<2:0>
C1 – CAN1 Combined Error	43	35	0x000059	IFS2<3> C1IF	IEC2<3> C1IE	IPC8<14:12> C1IP<2:0>
DMA3 – DMA Channel 3	44	36	0x00005A	IFS2<4> DMA3IF	IEC2<4> DMA3IE	IPC9<2:0> DMA3IP<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5> IC3IF	IEC2<5> IC3IE	IPC9<6:4> IC3IP<2:0>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6> IC4IF	IEC2<6> IC4IE	IPC9<10:8> IC4IP<2:0>
Reserved	47-56	39-48	0x000062-0x000074	—	—	—
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1> SI2C2IF	IEC3<1> SI2C2IE	IPC12<6:4> SI2C2IP<2:0>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2> MI2C2IF	IEC3<2> MI2C2IE	IPC12<10:8> MI2C2IP<2:0>
Reserved	59-61	51-53	0x00007A-0x00007E	—	—	—
INT4 – External Interrupt 4	62	54	0x000080	IFS3<6> INT4IF	IEC3<6> INT4IE	IPC13<10:8> INT4IP<2:0>
C2RX – CAN2 RX Data Ready	63	55	0x000082	IFS3<7> C2RXIF	IEC3<7> C2RXIE	IPC13<14:12> C2RXIP<2:0>
C2 – CAN 2 Combined Error	64	56	0x000083	IFS3<8> C2IF	IEC3<8> C2IE	IPC14<2:0> C2IP<2:0>
PSEM – PWM Special Event Match	65	57	0x000086	IFS3<9> PSEMIF	IEC3<9> PSEMIE	IPC14<6:4> PSEMIP<2:0>
Reserved	66-72	58-64	0x000088-0x000094	—	—	—
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1> U1EIF	IEC4<1> U1EIE	IPC16<6:4> U1EIP<2:0>
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2> U2EIF	IEC4<2> U2EIE	IPC16<10:8> U2EIP<2:0>
Reserved	75-77	67-69	0x00009A-0x0000A2	—	—	—
C1TX – CAN1 TX Data Request	78	70	0x0000A0	IFS4<6> C1TXIF	IEC4<6> C1TXIE	IPC17<10:8> C1TXIP<2:0>
C2TX – CAN2 TX Data Request	79	71	0x0000A	IFS4<7> C2TXIF	IEC4<7> C2TXIE	IPC17<14:12> C2TXIP<2:0>
Reserved	80	72	0x0000A4	—	—	—

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH<3:0>:** Last DMA Controller Channel Active Status bits

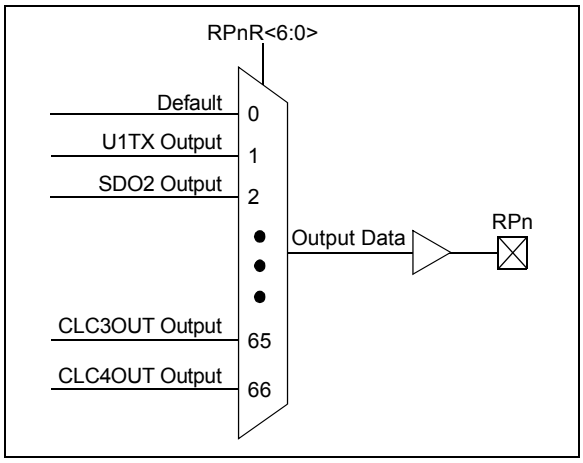
1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

11.6.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-33 through Register 11-56). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-13 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUTS FOR RPn



11.6.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings, across any or all of the RPn pins, is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

REGISTER 11-45: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP53R6	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP52R6	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP53R<6:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP52R<6:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-46: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP55R6	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP54R6	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP55R<6:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP54R<6:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-13 for peripheral function numbers)

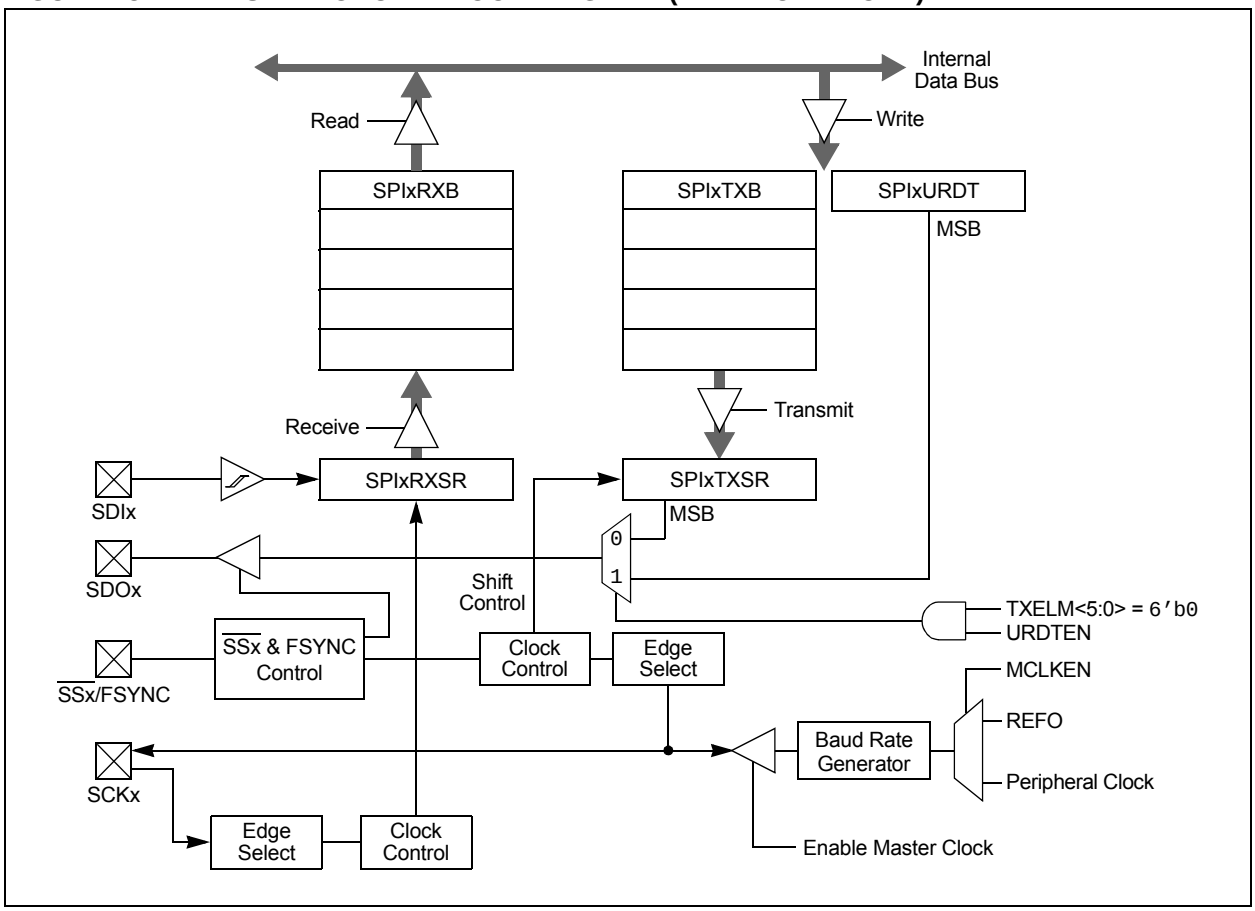
To set up the SPIx module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

FIGURE 18-2: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



20.1 UART Helpful Tips

1. In multi-node, direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pull-up or pull-down resistor on the RX pin depending on the value of the URXINV bit.
   a) If URXINV = 0, use a pull-up resistor on the UxRX pin.
   b) If URXINV = 1, use a pull-down resistor on the UxRX pin.
2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UARTx module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

20.2.1 KEY RESOURCES

- **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 21-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = Data Source 4 non-inverted signal is enabled for Gate 2
0 = Data Source 4 non-inverted signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 2
0 = Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = Data Source 3 non-inverted signal is enabled for Gate 2
0 = Data Source 3 non-inverted signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 2
0 = Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = Data Source 2 non-inverted signal is enabled for Gate 2
0 = Data Source 2 non-inverted signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 2
0 = Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = Data Source 1 non-inverted signal is enabled for Gate 2
0 = Data Source 1 non-inverted signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 2
0 = Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = Data Source 4 non-inverted signal is enabled for Gate 1
0 = Data Source 4 non-inverted signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 1
0 = Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = Data Source 3 non-inverted signal is enabled for Gate 1
0 = Data Source 3 non-inverted signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 1
0 = Data Source 3 inverted signal is disabled for Gate 1

BUFFER 21-5: CANx MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 3<15:8>:** CANx Message Byte 3 bits

bit 7-0 **Byte 2<7:0>:** CANx Message Byte 2 bits

BUFFER 21-6: CANx MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 5<15:8>:** CANx Message Byte 5 bits

bit 7-0 **Byte 4<7:0>:** CANx Message Byte 4 bits

25.0 PROGRAMMABLE GAIN AMPLIFIER (PGA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Programmable Gain Amplifier (PGA)"** (DS70005146) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

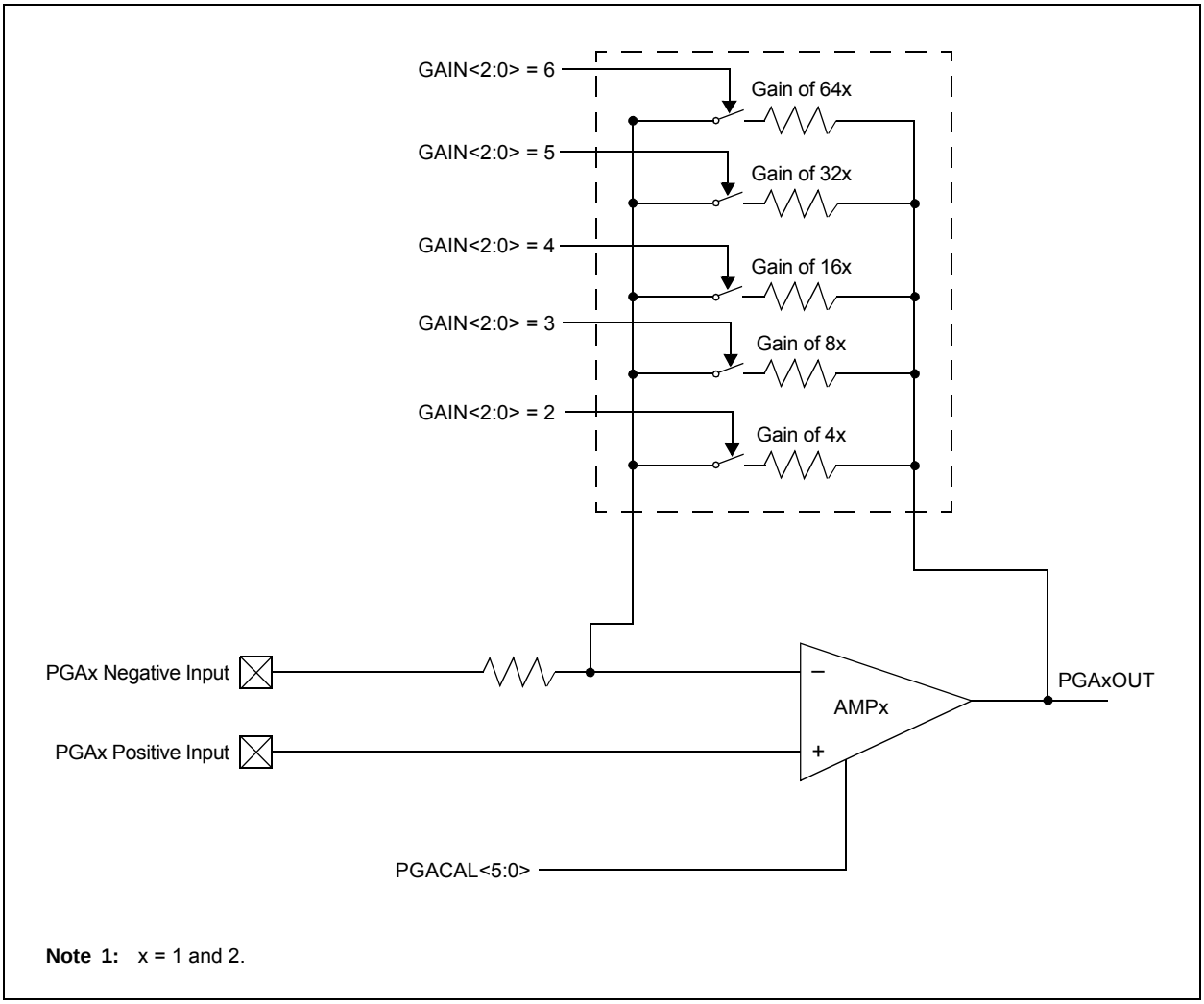
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family devices have two Programmable Gain Amplifiers (PGA1, PGA2). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x, 32x and 64x
- High Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

FIGURE 25-1: PGAx MODULE BLOCK DIAGRAM



Note 1: x = 1 and 2.

TABLE 30-11: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DI60a	IICL	**Input Low Injection Current**	0	—	-5(5,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP and RB7
DI60b	IICH	**Input High Injection Current**	0	—	+5(6,7,8)	mA	All pins except VDD, VSS, AVDD, AVSS, MCLR, VCAP, RB7 and all 5V tolerant pins(7)
DI60c	∑IICT	**Total Input Injection Current (sum of all I/O and control pins)**	-20(9)	—	+20(9)	mA	Absolute instantaneous sum of all ± input injection currents from all I/O pins (| IICL | + | IICH |) ≤ ∑IICT

Note 1: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: See the **"Pin Diagrams"** section for the 5V tolerant I/O pins.

5: VIL Source < (VSS – 0.3). Characterized but not tested.

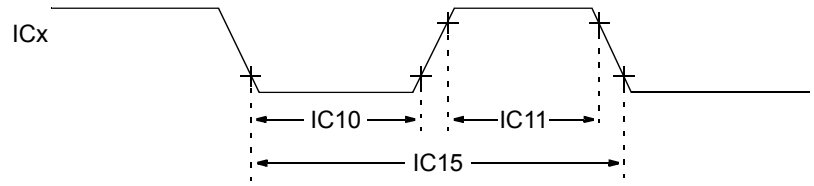
6: VIH Source > (VDD + 0.3) for pins that are not 5V tolerant only.

7: Digital 5V tolerant pins do not have internal high-side diodes to VDD and cannot tolerate any "positive" input injection current.

8: Injection Currents > | 0 | can affect the ADC results by approximately 4-6 counts.

9: Any number and/or combination of I/O pins not excluded under IICL or IICH conditions are permitted provided the mathematical "absolute instantaneous" sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 30-6: INPUT CAPTURE x (ICx) TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-27: INPUT CAPTURE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param. No.	**Symbol**	**Characteristics(1)**	**Min.**	**Max.**	**Units**	**Conditions**	
IC10	TccL	ICx Input Low Time	Greater of: 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	N = Prescale Value (1, 4, 16)
IC11	TccH	ICx Input High Time	Greater of: 12.5 + 25 or (0.5 TCY/N) + 25	—	ns	Must also meet Parameter IC15	
IC15	TccP	ICx Input Period	Greater of: 25 + 50 or (1 TCY/N) + 50	—	ns		

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-44: SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS(5)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK3 Input Frequency	—	—	25	MHz	**(Note 3)**
SP72	TscF	SCK3 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK3 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO3 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO3 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO3 Data Output Valid after SCK3 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO3 Data Output Setup to First SCK3 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI3 Data Input to SCK3 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI3 Data Input to SCK3 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS3}$ ↓ to SCK3 ↑ or SCK3 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS3}$ ↑ to SDO3 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SS3}$ ↑ after SCK3 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**
SP60	TssL2doV	SDO3 Data Output Valid after $\overline{SS3}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK3 is 91 ns. Therefore, the SCK3 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI3 pins.

5: For dsPIC33EPXXXGSX06 and dsPIC33EPXXXGSX08 devices with a fixed SCK3 pin.

31.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

FIGURE 31-1: VOH – 4x DRIVER PINS

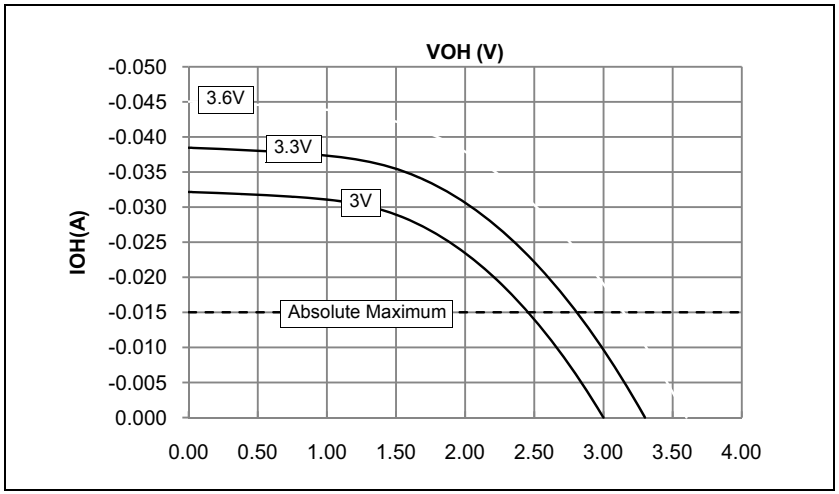


FIGURE 31-2: VOH – 8x DRIVER PINS

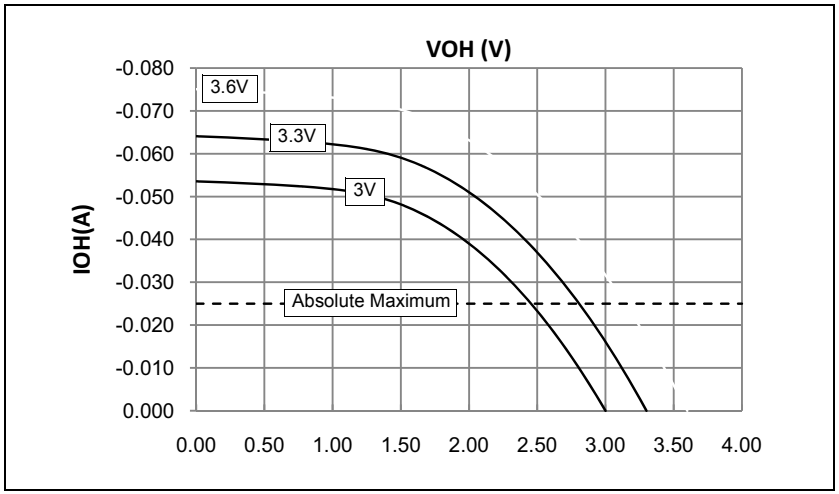


FIGURE 31-3: VOL – 4x DRIVER PINS

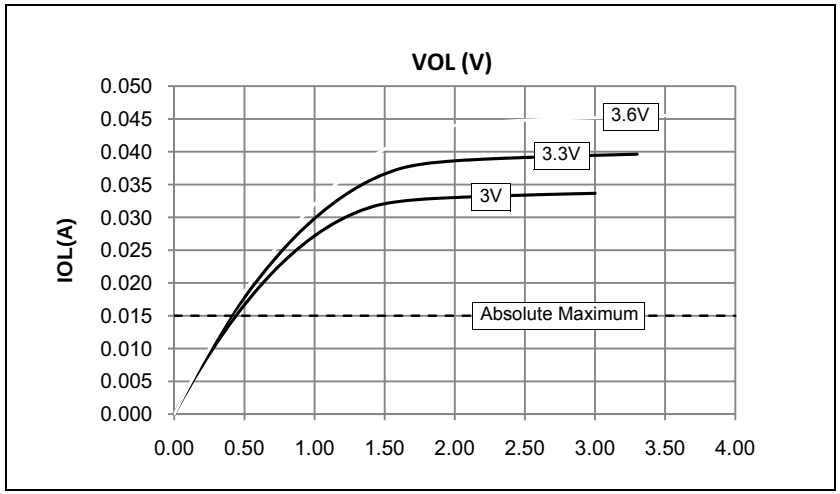


FIGURE 31-4: VOL – 8x DRIVER PINS

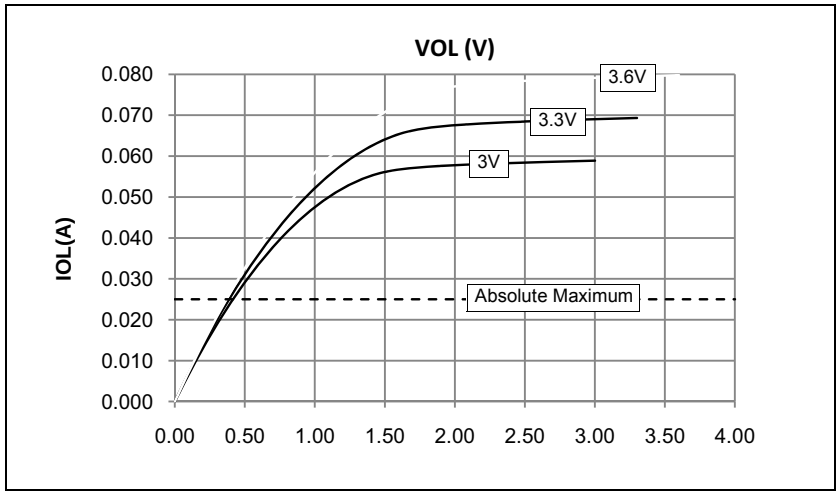


FIGURE 31-5: TYPICAL IPD CURRENT @ VDD = 3.3V

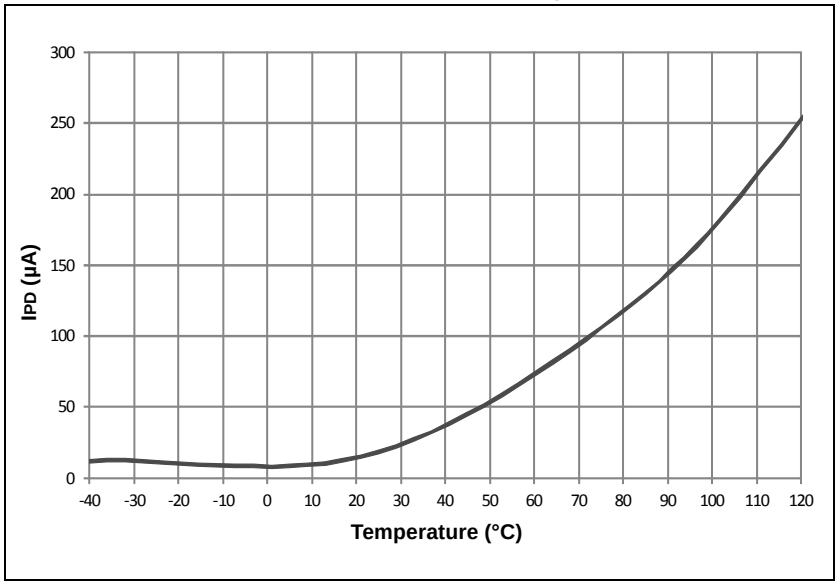


FIGURE 31-6: TYPICAL IDD CURRENT @ VDD = 3.3V, +25°C

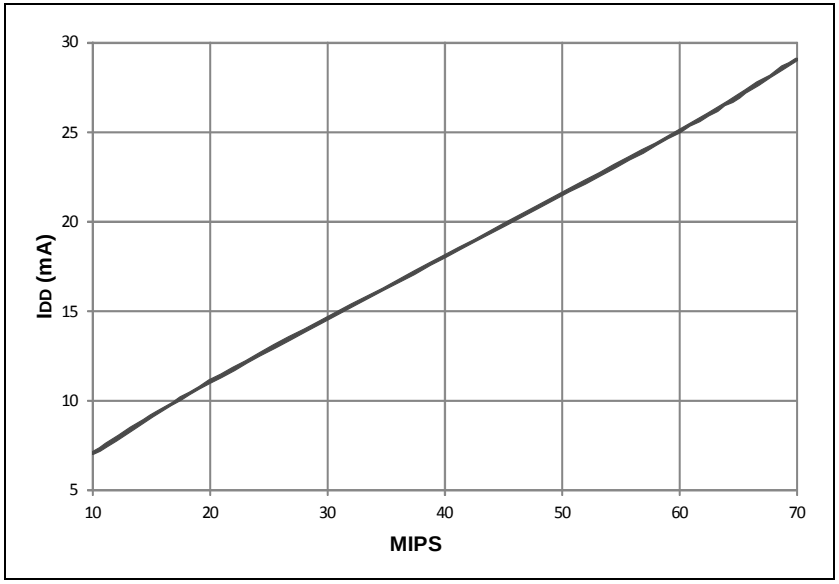


FIGURE 31-7: TYPICAL IDOZE CURRENT @ VDD = 3.3V, +25°C

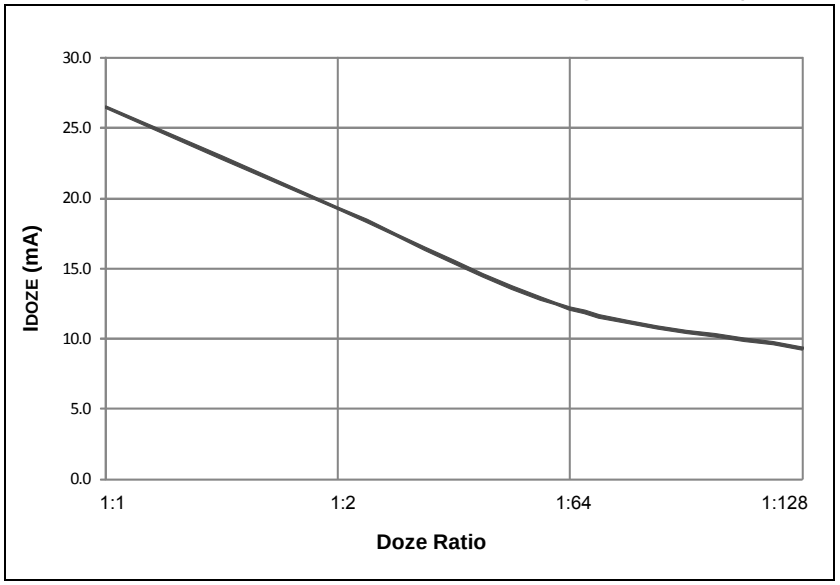
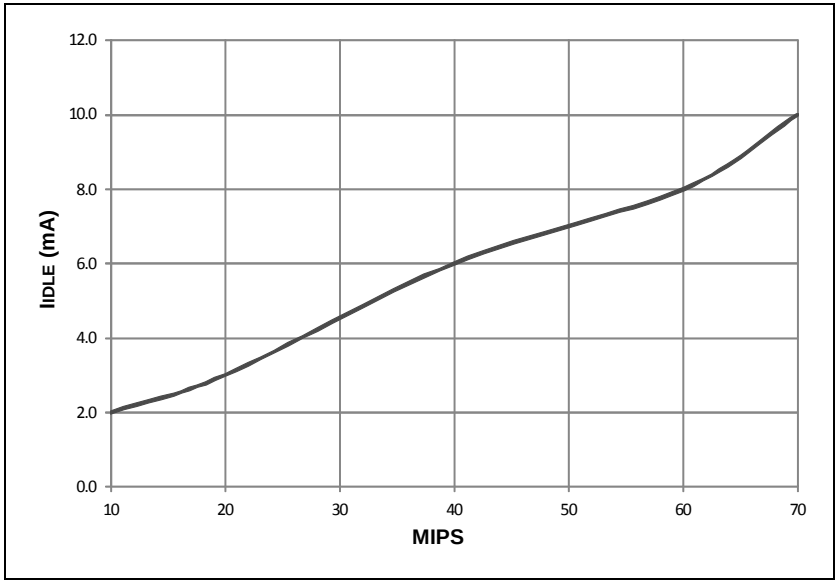
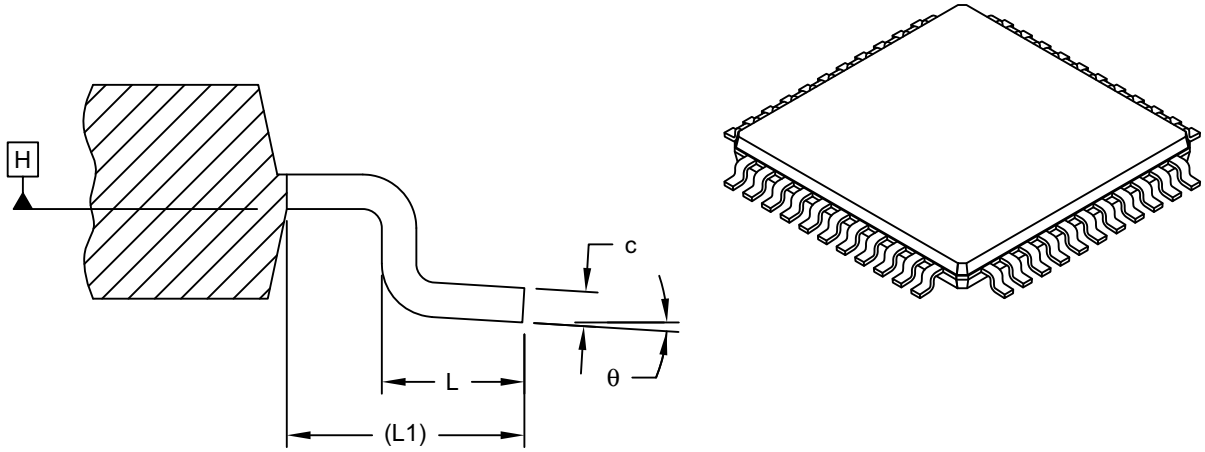


FIGURE 31-8: TYPICAL IIDLE CURRENT @ VDD = 3.3V, +25°C



44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

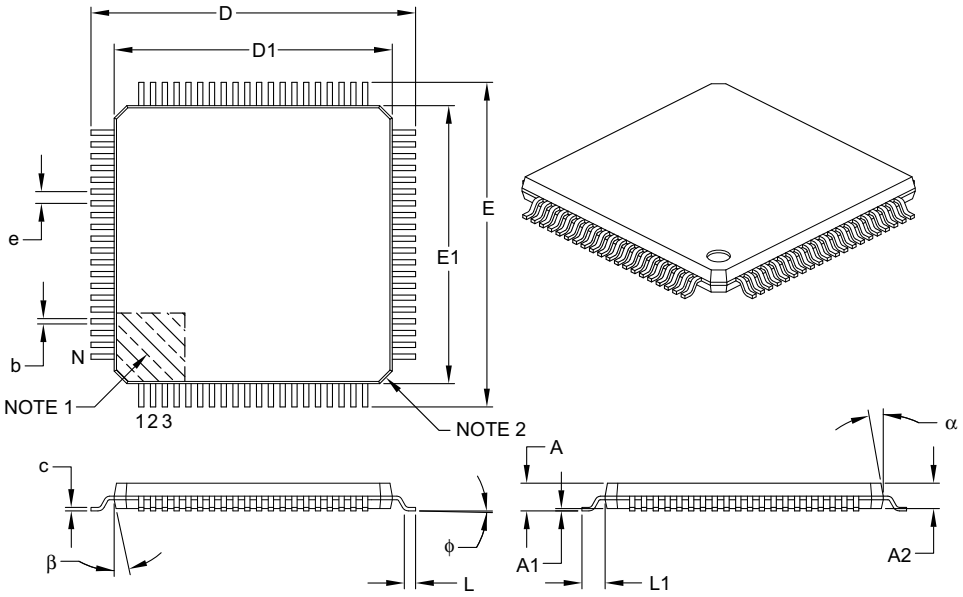
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076C Sheet 2 of 2

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		80	
Lead Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	ϕ	0°	3.5°	7°
Overall Width	E		14.00 BSC	
Overall Length	D		14.00 BSC	
Molded Package Width	E1		12.00 BSC	
Molded Package Length	D1		12.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.17	0.22	0.27
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B