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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs704t-i-ml

dsPIC33EPXXXGS70X/80X FAMILY

TABLE 4-10: SFR BLOCK 800h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Interrupt Controller			IEC9	832	0000000000000000	IPC26	874	000000001000100
IFS0	800	0000000000000000	IEC10	834	0000000000000000	IPC27	876	0100010000000000
IFS1	802	0000000000000000	IEC11	836	0000000000000000	IPC28	878	0100010001000100
IFS2	804	0000000000000000	IPC0	840	0100010001000100	IPC29	87A	000000001000100
IFS3	806	0000000000000000	IPC1	842	0100010001000000	IPC35	886	0100010000000000
IFS4	808	0000000000000000	IPC2	844	0100010001000100	IPC36	888	0000000000000000
IFS5	80A	0000000000000000	IPC3	846	0100000001000100	IPC37	88A	0100000000000000
IFS6	80C	0000000000000000	IPC4	848	0100010001000100	IPC38	88C	0100010001000100
IFS7	80E	0000000000000000	IPC5	84A	0000000000000100	IPC39	88E	0100010001000100
IFS8	810	0000000000000000	IPC6	84C	0100010001000000	IPC40	890	0100010001000100
IFS9	812	0000000000000000	IPC7	84E	0100010001000100	IPC41	892	0100010001000100
IFS10	814	0000000000000000	IPC8	850	0000000001000100	IPC42	894	000000001000100
IFS11	816	0000000000000000	IPC9	852	0000010001000000	IPC43	896	0000010001000000
IEC0	820	0000000000000000	IPC11	856	0000000000000000	IPC44	898	0100010001000000
IEC1	822	0000000000000000	IPC12	858	0000010001000000	IPC45	89A	0000000000000100
IEC2	824	0000000000000000	IPC13	85A	0000010000000000	IPC46	89C	0100010000000000
IEC3	826	0000000000000000	IPC14	85C	0000000001000000	IPC47	89E	0000010001000100
IEC4	828	0000000000000000	IPC16	860	0000010001000000	INTCON1	8C0	0000000000000000
IEC5	82A	0000000000000000	IPC18	864	0000000001000000	INTCON2	8C2	0000000000000000
IEC6	82C	0000000000000000	IPC23	86E	0100010000000000	INTCON3	8C4	0000000000000000
IEC7	82E	0000000000000000	IPC24	870	0000010001000100	INTCON4	8C6	0000000000000000
IEC8	830	0000000000000000	IPC25	872	0100000000000000	INTTREG	8C8	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-11: SFR BLOCK 900h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
Output Compare			OC3R	91A	xxxxxxxxxxxxxxxx	CLC2CONH	9CE	0000000000000000
OC1CON1	900	0000000000000000	OC3TMR	91C	0000000000000000	CLC2SEL	9D0	0000000000000000
OC1CON2	902	0000000000001100	OC4CON1	91E	0000000000000000	CLC2GLSL	9D4	0000000000000000
OC1RS	904	xxxxxxxxxxxxxxxx	OC4CON2	920	0000000000001100	CLC2GLSH	9D6	0000000000000000
OC1R	906	xxxxxxxxxxxxxxxx	OC4RS	922	xxxxxxxxxxxxxxxx	CLC3CONL	9D8	0000000000000000
OC1TMR	908	0000000000000000	OC4R	924	xxxxxxxxxxxxxxxx	CLC3CONH	9DA	0000000000000000
OC2CON1	90A	0000000000000000	OC4TMR	926	0000000000000000	CLC3SEL	9DC	0000000000000000
OC2CON2	90C	0000000000001100	CLC			CLC3GLSL	9E0	0000000000000000
OC2RS	90E	xxxxxxxxxxxxxxxx	CLC1CONL	9C0	0000000000000000	CLC3GLSH	9E2	0000000000000000
OC2R	910	xxxxxxxxxxxxxxxx	CLC1CONH	9C2	0000000000000000	CLC4CONL	9E4	0000000000000000
OC2TMR	912	0000000000000000	CLC1SEL	9C4	0000000000000000	CLC4CONH	9E6	0000000000000000
OC3CON1	914	0000000000000000	CLC1GLSL	9C8	0000000000000000	CLC4SEL	9E8	0000000000000000
OC3CON2	916	0000000000001100	CLC1GLSH	9CA	0000000000000000	CLC4GLSL	9EC	0000000000000000
OC3RS	918	xxxxxxxxxxxxxxxx	CLC2CONL	9CC	0000000000000000	CLC4GLSH	9EE	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

dsPIC33EPXXXGS70X/80X FAMILY

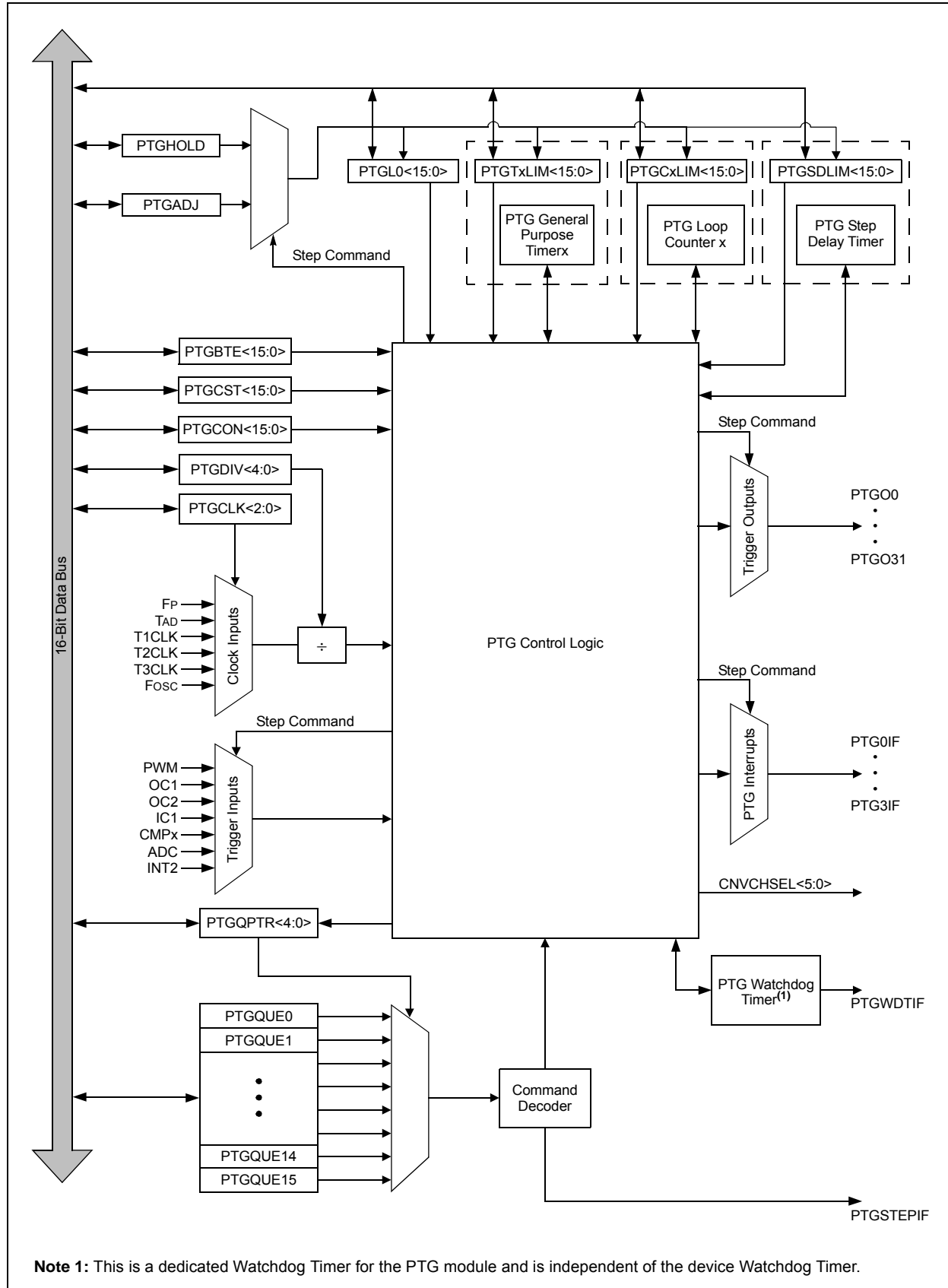
REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device has been in Idle mode 0 = Device has not been in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the WDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

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FIGURE 17-1: PTG BLOCK DIAGRAM



dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 19-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enables interrupt on detection of Stop condition

0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I²C Slave mode only)

1 = Enables interrupt on detection of Start or Restart conditions

0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I²C Slave mode only)

1 = I2CxRCV is updated and ACK is generated for a received address/data byte, ignoring the state of the I2COV only if the RBF bit = 0

0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit

1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx

0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I²C Slave mode only)

1 = Enables slave bus collision interrupts

0 = Slave bus collision interrupts are disabled

If the rising edge of SCLx and SDAx is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit (I²C Slave mode only)

1 = Following the 8th falling edge of SCLx for a matching received address byte, the SCLREL (I2CxCONL<12>) bit will be cleared and SCLx will be held low

0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I²C Slave mode only)

1 = Following the 8th falling edge of SCLx for a received data byte, the slave hardware clears the SCLREL (I2CxCONL<12>) bit and SCLx is held low

0 = Data holding is disabled

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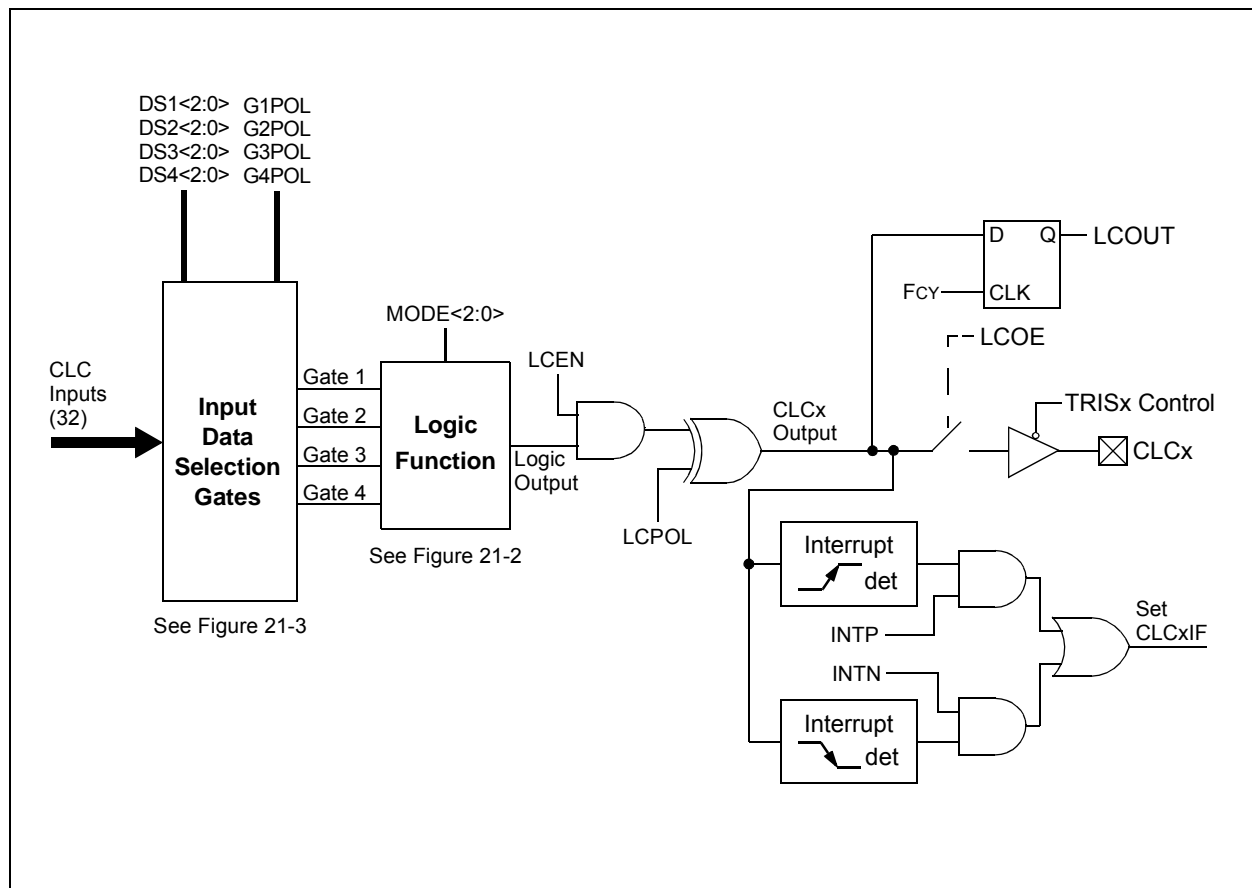
21.0 CONFIGURABLE LOGIC CELL (CLC)

Note: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Configurable Logic Cell (CLC)**” (DS70005298) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

The Configurable Logic Cell (CLC) module allows the user to specify combinations of signals as inputs to a logic function and to use the logic output to control other peripherals or I/O pins. This provides greater flexibility and potential in embedded designs since the CLC module can operate outside the limitations of software execution and supports a vast amount of output designs.

There are four input gates to the selected logic function. These four input gates select from a pool of up to 32 signals that are selected using four data source selection multiplexers. Figure 21-1 shows an overview of the module. Figure 21-3 shows the details of the data source multiplexers and logic input gate connections.

FIGURE 21-1: CLCx MODULE



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REGISTER 21-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

- bit 3 **G1D2T:** Gate 1 Data Source 2 True Enable bit
1 = Data Source 2 non-inverted signal is enabled for Gate 1
0 = Data Source 2 non-inverted signal is disabled for Gate 1
- bit 2 **G1D2N:** Gate 1 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 1
0 = Data Source 2 inverted signal is disabled for Gate 1
- bit 1 **G1D1T:** Gate 1 Data Source 1 True Enable bit
1 = Data Source 1 non-inverted signal is enabled for Gate 1
0 = Data Source 1 non-inverted signal is disabled for Gate 1
- bit 0 **G1D1N:** Gate 1 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 1
0 = Data Source 1 inverted signal is disabled for Gate 1

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REGISTER 22-12: ADCORExH: DEDICATED ADC CORE x CONTROL REGISTER HIGH (x = 0 to 3)⁽¹⁾

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1
—	—	—	EISEL2	EISEL1	EISEL0	RES1	RES0
bit 15						bit 8	

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	ADCS6	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-10 **EISEL<2:0>:** ADC Core x Early Interrupt Time Selection bits

111 = Early interrupt is set and an interrupt is generated 8 TADCORE clocks prior to when the data is ready
 110 = Early interrupt is set and an interrupt is generated 7 TADCORE clocks prior to when the data is ready
 101 = Early interrupt is set and an interrupt is generated 6 TADCORE clocks prior to when the data is ready
 100 = Early interrupt is set and an interrupt is generated 5 TADCORE clocks prior to when the data is ready
 011 = Early interrupt is set and an interrupt is generated 4 TADCORE clocks prior to when the data is ready
 010 = Early interrupt is set and an interrupt is generated 3 TADCORE clocks prior to when the data is ready
 001 = Early interrupt is set and an interrupt is generated 2 TADCORE clocks prior to when the data is ready
 000 = Early interrupt is set and an interrupt is generated 1 TADCORE clock prior to when the data is ready

bit 9-8 **RES<1:0>:** ADC Core x Resolution Selection bits

11 = 12-bit resolution
 10 = 10-bit resolution
 01 = 8-bit resolution
 00 = 6-bit resolution

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ADCS<6:0>:** ADC Core x Input Clock Divider bits

These bits determine the number of Source Clock Periods (TCORESRC) for one Core Clock Period (TADCORE).

1111111 = 254 Source Clock Periods

•
•
•

0000011 = 6 Source Clock Periods

0000010 = 4 Source Clock Periods

0000001 = 2 Source Clock Periods

0000000 = 2 Source Clock Periods

Note 1: For the 6-bit ADC core resolution (RES<1:0> = 00), the EISEL<2:0> bits settings, from '100' to '111', are not valid and should not be used. For the 8-bit ADC core resolution (RES<1:0> = 01), the EISEL<2:0> bits settings, '110' and '111', are not valid and should not be used.

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23.3 CAN Control Registers

REGISTER 23-1: CxCTRL1: CANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15						bit 8	
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13 **CSIDL:** CANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted
- bit 11 **CANCKS:** CANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP
- bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode
- bit 7-5 **OPMODE<2:0>:** Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode
- bit 4 **Unimplemented:** Read as '0'
- bit 3 **CANCAP:** CANx Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

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24.3 Module Applications

This module provides a means for the SMPS dsPIC[®] DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 12-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWMx Signal (current limit)
- Truncate the PWMx Period (current minimum)
- Disable the PWMx Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) generate an interrupt, 2) have the ADC take a sample and convert it, and 3) truncate the PWMx output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

24.4 Digital-to-Analog Comparator (DAC)

Each analog comparator has a dedicated 12-bit DAC that is used to program the comparator threshold voltage via the CMPxDAC register. The DAC voltage reference source is selected using the EXTREF and RANGE bits in the CMPxCON register.

The EXTREF bit selects either the external voltage reference, EXTREFx, or an internal source as the voltage reference source. The EXTREFx input enables users to connect to a voltage reference that better suits their application. The RANGE bit enables AVDD as the voltage reference source for the DAC when an internal voltage reference is selected.

Note: EXTREF2 is not available on all devices.

Each DACx has an output enable bit, DACOE, in the CMPxCON register that enables the DACx reference voltage to be routed to an external output pin (DACOUTx). Refer to Figure 24-1 for connecting the DACx output voltage to the DACOUTx pins.

Note 1: Ensure that multiple DACOE bits are not set in software. The output on the DACOUTx pin will be indeterminate if multiple comparators enable the DACx output.

2: DACOUT2 is not available on all devices.

24.5 Pulse Stretcher and Digital Logic

The analog comparator can respond to very fast transient signals. After the comparator output is given the desired polarity, the signal is passed to a pulse stretching circuit. The pulse stretching circuit has an asynchronous set function and a delay circuit that ensures the minimum pulse width is three system clock cycles wide to allow the attached circuitry to properly respond to a narrow pulse event.

The pulse stretcher circuit is followed by a digital filter. The digital filter is enabled via the FLTREN bit in the CMPxCON register. The digital filter operates with the clock specified via the FCLKSEL bit in the CMPxCON register. The comparator signal must be stable in a high or low state, for at least three of the selected clock cycles, for it to pass through the digital filter.

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26.3 Current Source Control Register

REGISTER 26-1: ISRCCON: CONSTANT-CURRENT SOURCE CONTROL REGISTER

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ISRCEN	—	—	—	—	OUTSEL2	OUTSEL1	OUTSEL0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ISRCCAL5	ISRCCAL4	ISRCCAL3	ISRCCAL2	ISRCCAL1	ISRCCAL0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **ISRCEN:** Constant-Current Source Enable bit

1 = Current source is enabled
0 = Current source is disabled

bit 14-11 **Unimplemented:** Read as '0'

bit 10-8 **OUTSEL<2:0>:** Output Constant-Current Select bits

111 = Reserved
110 = Reserved
101 = Reserved
100 = Input pin, ISRC4 (AN4)
011 = Input pin, ISRC3 (AN5)
010 = Input pin, ISRC2 (AN6)
001 = Input pin, ISRC1 (AN12)
000 = No output is selected

bit 7-6 **Unimplemented:** Read as '0'

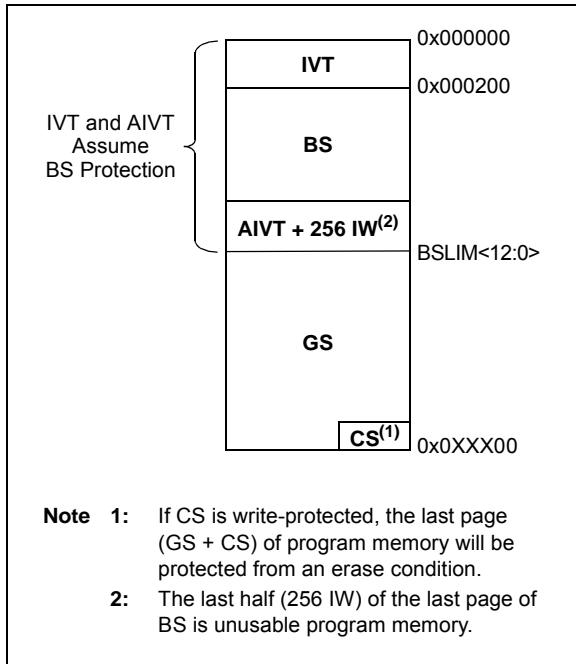
bit 5-0 **ISRCCAL<5:0>:** Constant-Current Source Calibration bits

The calibration value must be copied from Flash address, 0x800E78, into these bits before the module is enabled. Refer to the calibration data address table (Table 27-3) in **Section 27.0 “Special Features”** for more information.

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The different device security segments are shown in Figure 27-3. Here, all three segments are shown but are not required. If only basic code protection is required, then GS can be enabled independently or combined with CS, if desired.

FIGURE 27-3: SECURITY SEGMENTS EXAMPLE FOR dsPIC33EPXXXGS70X/80X DEVICES

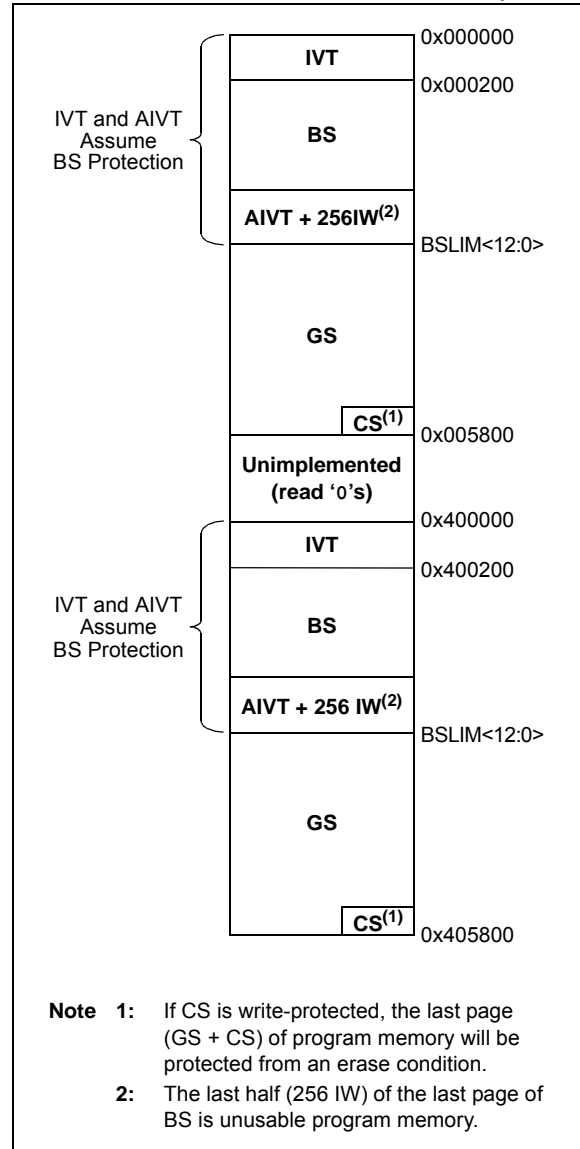


dsPIC33EPXXXGS70X/80X family devices can be operated in Dual Partition mode, where security is required for each partition. When operating in Dual Partition mode, the Active and Inactive Partitions both contain unique copies of the Reset vector, Interrupt Vector Tables (IVT and AIVT, if enabled) and the Flash Configuration Words. Both partitions have the three security segments described previously. Code may not be executed from the Inactive Partition, but it may be programmed by, and read from, the Active Partition, subject to defined code protection. Figure 27-4 and Figure 27-5 show the different security segments for devices operating in Dual Partition mode.

The device may also operate in a Protected Dual Partition mode or in Privileged Dual Partition mode. In Protected Dual Partition mode, Partition 1 is permanently erase/write-protected. This implementation allows for a “Factory Default” mode, which provides a fail-safe backup image to be stored in Partition 1. For example, a fail-safe bootloader can be placed in Partition 1, along with a fail-safe backup code image, which can be used or rewritten into Partition 2 in the event of a failed Flash update to Partition 2.

Privileged Dual Partition mode performs the same function as Protected Dual Partition mode, except additional constraints are applied in an effort to prevent code in the Boot Segment and General Segment from being used against each other.

FIGURE 27-4: SECURITY SEGMENTS EXAMPLE FOR dsPIC33EP64GS70X/80X DEVICES (DUAL PARTITION MODES)



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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽¹⁾	Status Flags Affected
26	CTXTSWP	CTXTSWP #lit3	Switch CPU register context to context defined by lit3	1	2	None
		CTXTSWP Wn	Switch CPU register context to context defined by Wn	1	2	None
27	DAW	DAW Wn	Wn = decimal adjust Wn	1	1	C
28	DEC	DEC f	$f = f - 1$	1	1	C,DC,N,OV,Z
		DEC f, WREG	WREG = $f - 1$	1	1	C,DC,N,OV,Z
		DEC Ws, Wd	Wd = Ws - 1	1	1	C,DC,N,OV,Z
29	DEC2	DEC2 f	$f = f - 2$	1	1	C,DC,N,OV,Z
		DEC2 f, WREG	WREG = $f - 2$	1	1	C,DC,N,OV,Z
		DEC2 Ws, Wd	Wd = Ws - 2	1	1	C,DC,N,OV,Z
30	DISI	DISI #lit14	Disable Interrupts for k instruction cycles	1	1	None
31	DIV	DIV.S Wm, Wn	Signed 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.SD Wm, Wn	Signed 32/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.U Wm, Wn	Unsigned 16/16-bit Integer Divide	1	18	N,Z,C,OV
		DIV.UD Wm, Wn	Unsigned 32/16-bit Integer Divide	1	18	N,Z,C,OV
32	DIVF	DIVF Wm, Wn	Signed 16/16-bit Fractional Divide	1	18	N,Z,C,OV
33	DO	DO #lit15, Expr	Do code to PC + Expr, lit15 + 1 times	2	2	None
		DO Wn, Expr	Do code to PC + Expr, (Wn) + 1 times	2	2	None
34	ED	ED Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance (no accumulate)	1	1	OA,OB,OAB,SA,SB,SAB
35	EDAC	EDAC Wm*Wm, Acc, Wx, Wy, Wxd	Euclidean Distance	1	1	OA,OB,OAB,SA,SB,SAB
36	EXCH	EXCH Wns, Wnd	Swap Wns with Wnd	1	1	None
37	FBCL	FBCL Ws, Wnd	Find Bit Change from Left (MSb) Side	1	1	C
38	FF1L	FF1L Ws, Wnd	Find First One from Left (MSb) Side	1	1	C
39	FF1R	FF1R Ws, Wnd	Find First One from Right (LSb) Side	1	1	C
40	GOTO	GOTO Expr	Go to address	2	4	None
		GOTO Wn	Go to indirect	1	4	None
		GOTO.L Wn	Go to indirect (long address)	1	4	None
41	INC	INC f	$f = f + 1$	1	1	C,DC,N,OV,Z
		INC f, WREG	WREG = $f + 1$	1	1	C,DC,N,OV,Z
		INC Ws, Wd	Wd = Ws + 1	1	1	C,DC,N,OV,Z
42	INC2	INC2 f	$f = f + 2$	1	1	C,DC,N,OV,Z
		INC2 f, WREG	WREG = $f + 2$	1	1	C,DC,N,OV,Z
		INC2 Ws, Wd	Wd = Ws + 2	1	1	C,DC,N,OV,Z
43	IOR	IOR f	$f = f .IOR. WREG$	1	1	N,Z
		IOR f, WREG	WREG = $f .IOR. WREG$	1	1	N,Z
		IOR #lit10, Wn	Wd = lit10 .IOR. Wd	1	1	N,Z
		IOR Wb, Ws, Wd	Wd = Wb .IOR. Ws	1	1	N,Z
		IOR Wb, #lit5, Wd	Wd = Wb .IOR. lit5	1	1	N,Z
44	LAC	LAC Wso, #Slit4, Acc	Load Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
45	LNK	LNK #lit14	Link Frame Pointer	1	1	SFA
46	LSR	LSR f	$f = \text{Logical Right Shift } f$	1	1	C,N,OV,Z
		LSR f, WREG	WREG = Logical Right Shift f	1	1	C,N,OV,Z
		LSR Ws, Wd	Wd = Logical Right Shift Ws	1	1	C,N,OV,Z
		LSR Wb, Wns, Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N,Z
		LSR Wb, #lit5, Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N,Z
47	MAC	MAC Wm*Wn, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB
		MAC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square and Accumulate	1	1	OA,OB,OAB,SA,SB,SAB

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles ⁽¹⁾	Status Flags Affected
48	MOV	MOV f, Wn	Move f to Wn	1	1	None
		MOV f	Move f to f	1	1	None
		MOV f, WREG	Move f to WREG	1	1	None
		MOV #lit16, Wn	Move 16-bit literal to Wn	1	1	None
		MOV.b #lit8, Wn	Move 8-bit literal to Wn	1	1	None
		MOV Wn, f	Move Wn to f	1	1	None
		MOV Wso, Wdo	Move Ws to Wd	1	1	None
		MOV WREG, f	Move WREG to f	1	1	None
		MOV.D Wns, Wd	Move Double from W(ns):W(ns + 1) to Wd	1	2	None
		MOV.D Ws, Wnd	Move Double from Ws to W(nd + 1):W(nd)	1	2	None
49	MOVPAG	MOVPAG #lit10, DSRPAG	Move 10-bit literal to DSRPAG	1	1	None
		MOVPAG #lit8, TBLPAG	Move 8-bit literal to TBLPAG	1	1	None
		MOVPAGW Ws, DSRPAG	Move Ws<9:0> to DSRPAG	1	1	None
		MOVPAGW Ws, TBLPAG	Move Ws<7:0> to TBLPAG	1	1	None
50	MOVSAC	MOVSAC Acc, Wx, Wxd, Wy, Wyd, AWB	Prefetch and store accumulator	1	1	None
51	MPY	MPY Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	Multiply Wm by Wn to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
		MPY Wm*Wm, Acc, Wx, Wxd, Wy, Wyd	Square Wm to Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
52	MPY.N	MPY.N Wm*Wn, Acc, Wx, Wxd, Wy, Wyd	-(Multiply Wm by Wn) to Accumulator	1	1	None
53	MSC	MSC Wm*Wm, Acc, Wx, Wxd, Wy, Wyd, AWB	Multiply and Subtract from Accumulator	1	1	OA,OB,OAB,SA,SB,SAB
54	MUL	MUL.SS Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * signed(Ws)	1	1	None
		MUL.SS Wb, Ws, Acc	Accumulator = signed(Wb) * signed(Ws)	1	1	None
		MUL.SU Wb, Ws, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, Ws, Acc	Accumulator = signed(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Acc	Accumulator = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.US Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.US Wb, Ws, Acc	Accumulator = unsigned(Wb) * signed(Ws)	1	1	None
		MUL.UU Wb, Ws, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.UU Wb, #lit5, Acc	Accumulator = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, Ws, Acc	Accumulator = unsigned(Wb) * unsigned(Ws)	1	1	None
		MULW.SS Wb, Ws, Wnd	Wnd = signed(Wb) * signed(Ws)	1	1	None
		MULW.SU Wb, Ws, Wnd	Wnd = signed(Wb) * unsigned(Ws)	1	1	None
		MULW.US Wb, Ws, Wnd	Wnd = unsigned(Wb) * signed(Ws)	1	1	None
		MULW.UU Wb, Ws, Wnd	Wnd = unsigned(Wb) * unsigned(Ws)	1	1	None
		MUL.SU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.SU Wb, #lit5, Wnd	Wnd = signed(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	{Wnd + 1, Wnd} = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL.UU Wb, #lit5, Wnd	Wnd = unsigned(Wb) * unsigned(lit5)	1	1	None
		MUL f	W3:W2 = f * WREG	1	1	None

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

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TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO10	VOL	Output Low Voltage 4x Sink Driver Pins ⁽²⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins ⁽³⁾	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	Output High Voltage 4x Source Driver Pins ⁽²⁾	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	Output High Voltage 4x Source Driver Pins ⁽²⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins ⁽³⁾	1.5 ⁽¹⁾	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0 ⁽¹⁾	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0 ⁽¹⁾	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes RA0-RA2, RB0-RB1, RB9, RC1-RC2, RC9-RC10, RC12, RD7, RD8, RE4-RE5, RE8-RE9 and RE12-RE13 pins.

3: Includes all I/O pins that are not 4x driver pins (see **Note 2**).

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min. ⁽²⁾	Typ.	Max.	Units	Conditions
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD (Notes 2 and 3)

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, PGAs and comparators) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

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30.2 AC Characteristics and Timing Parameters

This section defines the dsPIC33EPXXXGS70X/80X family AC characteristics and timing parameters.

TABLE 30-15: TEMPERATURE AND VOLTAGE SPECIFICATIONS – AC

AC CHARACTERISTICS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)
	Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended
	Operating voltage V_{DD} range as described in Section 30.1 “DC Characteristics” .

FIGURE 30-1: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

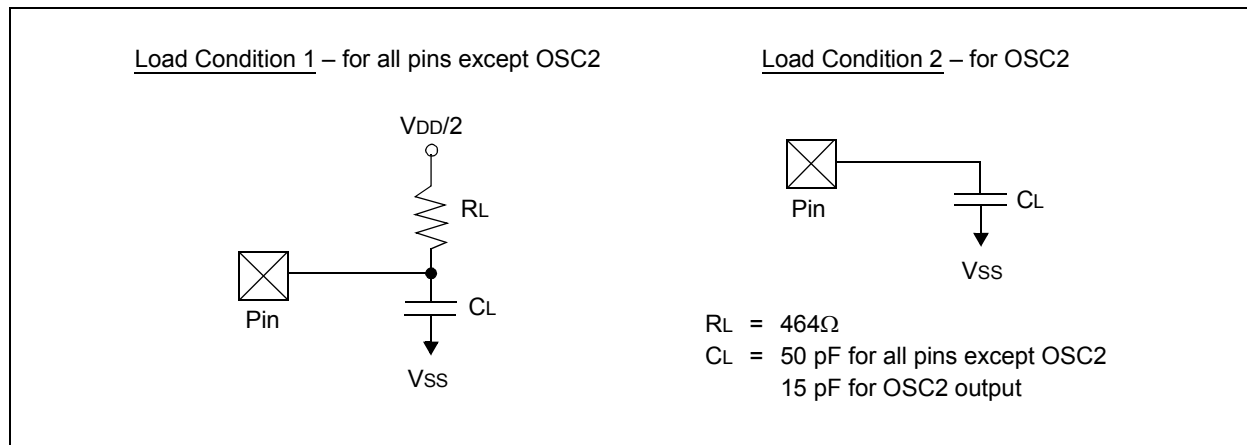


TABLE 30-16: CAPACITIVE LOADING REQUIREMENTS ON OUTPUT PINS

Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DO50	Cosco	OSC2 Pin	—	—	15	pF	In XT and HS modes, when external clock is used to drive OSC1
DO56	Cio	All I/O Pins and OSC2	—	—	50	pF	EC mode
DO58	CB	SCLx, SDAx	—	—	400	pF	In I ² C mode

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FIGURE 30-31: CANx MODULE I/O TIMING CHARACTERISTICS

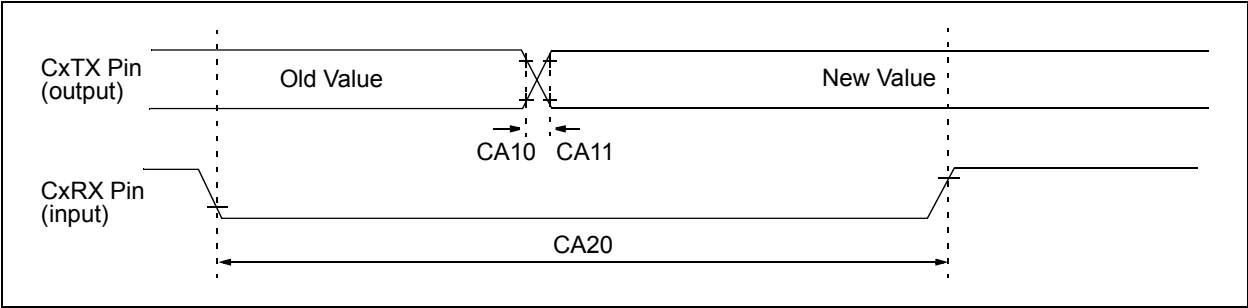


TABLE 30-49: CANx MODULE I/O TIMING REQUIREMENTS

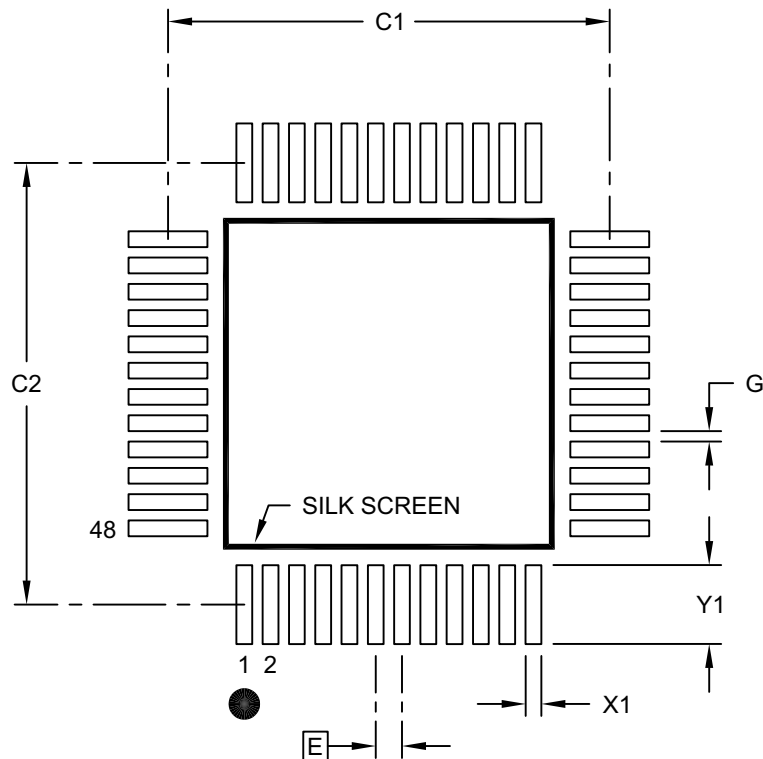
AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
CA10	TioF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TioR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TcWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

- Note 1:** These parameters are characterized but not tested in manufacturing.
- 2:** Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

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48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Contact Pitch	E		0.50 BSC		
Contact Pad Spacing	C1			8.40	
Contact Pad Spacing	C2			8.40	
Contact Pad Width (X48)	X1				0.30
Contact Pad Length (X48)	Y1				1.50
Distance Between Pads	G		0.20		

Notes:

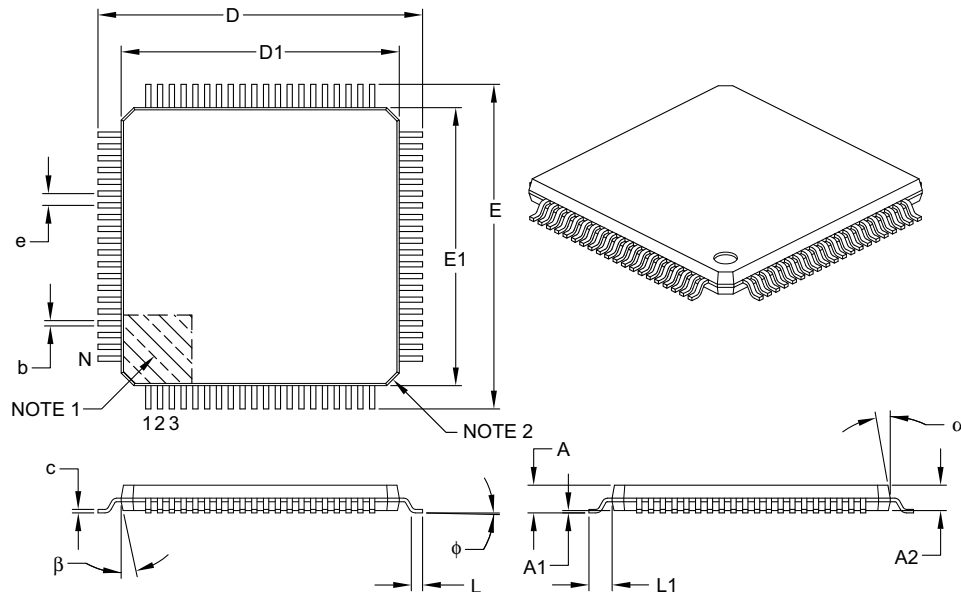
1. Dimensioning and tolerancing per ASME Y14.5M
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2300-PT Rev A

dsPIC33EPXXXGS70X/80X FAMILY

80-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Leads	N		80		
Lead Pitch	e		0.50 BSC		
Overall Height	A		–	–	1.20
Molded Package Thickness	A2		0.95	1.00	1.05
Standoff	A1		0.05	–	0.15
Foot Length	L		0.45	0.60	0.75
Footprint	L1		1.00 REF		
Foot Angle	φ		0°	3.5°	7°
Overall Width	E		14.00 BSC		
Overall Length	D		14.00 BSC		
Molded Package Width	E1		12.00 BSC		
Molded Package Length	D1		12.00 BSC		
Lead Thickness	c		0.09	–	0.20
Lead Width	b		0.17	0.22	0.27
Mold Draft Angle Top	α		11°	12°	13°
Mold Draft Angle Bottom	β		11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-092B

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