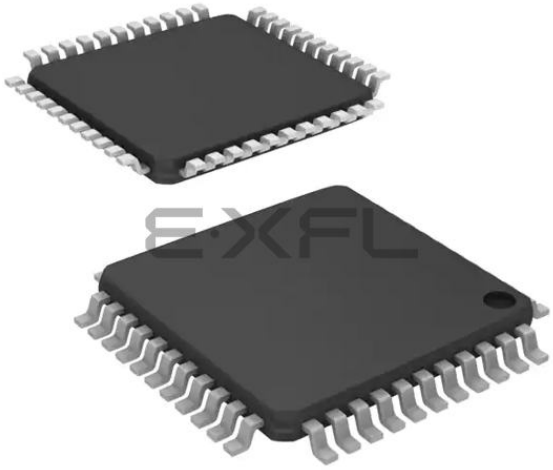
Microchip Technology - DSPIC33EP128GS704T-I/PT Datasheet



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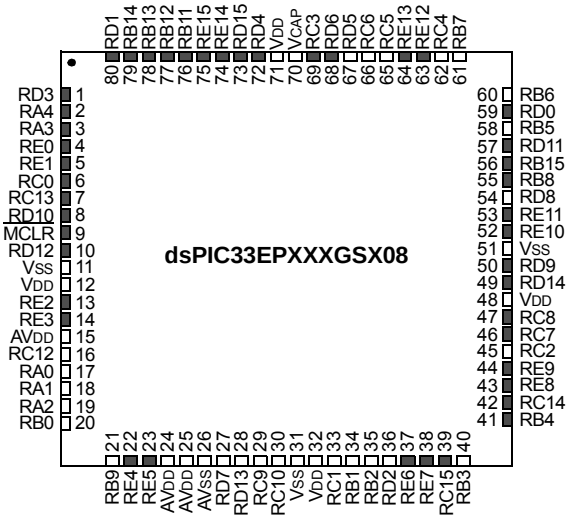
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs704t-i-pt

Pin Diagrams (Continued)

80-Pin TQFP



Pin	Pin Function	Pin	Pin Function
1	PWM4L/**RP67**/RD3	41	PGEC2/ADTRG31/**RP36**/RB4
2	PWM1H/**RP20**/RA4	42	**RP62**/RC14
3	PWM1L/**RP19**/RA3	43	RE8
4	PWM8L/RE0	44	RE9
5	PWM8H/RE1	45	EXTREF1/AN9/CMP4D/**RP50**/RC2
6	FLT12/**RP48**/RC0	46	ASDA1/**RP55**/RC7
7	FLT11/**RP61**/RC13	47	ASCL1/**RP56**/RC8
8	CLC4OUT/FLT10/**RP74**/RD10	48	VDD
9	MCLR	49	CLC3OUT/RD14
10	T5CK/FLT9/**RP76**/RD12	50	SCK3/**RP73**/RD9
11	VSS	51	VSS
12	VDD	52	FLT21/RE10
13	FLT17/RE2	53	FLT22/RE11
14	FLT18/RE3	54	AN5/CMP2D/CMP3B/ISRC3/**RP72**/RD8
15	AVDD	55	PGED3/SDA2/FLT31/**RP40**/RB8
16	AN14/PGA2N3/**RP60**/RC12	56	PGEC3/SCL2/**RP47**/RB15
17	AN0/CMP1A/PGA1P1/**RP16**/RA0	57	INT4/**RP75**/RD11
18	AN1/CMP1B/PGA1P2/PGA2P1/**RP17**/RA1	58	TD0/AN19/PGA2N2/**RP37**/RB5
19	AN2/CMP1C/CMP2A/PGA1P3/PGA2P2/**RP18**/RA2	59	T4CK/**RP64**/RD0
20	AN3/CMP1D/CMP2B/PGA2P3/**RP32**/RB0	60	PGED1/TDI/AN20/SCL1/**RP38**/RB6
21	AN4/CMP2C/CMP3A/ISRC4/**RP41**/RB9	61	PGEC1/AN21/SDA1/**RP39**/RB7
22	RE4	62	AN1ALT/**RP52**/RC4
23	RE5	63	RE12
24	AVDD	64	RE13
25	AVDD	65	AN0ALT/**RP53**/RC5
26	AVSS	66	AN17/**RP54**/RC6
27	AN15/**RP71**/RD7	67	AN12/ISRC1/**RP69**/RD5
28	DACOUT2/AN13/RD13	68	PWM5H/**RP70**/RD6
29	AN11/PGA1N3/**RP57**/RC9	69	PWM5L/**RP51**/RC3
30	EXTREF2/AN10/PGA1P4/**RP58**/RC10	70	VCAP
31	VSS	71	VDD
32	VDD	72	PWM6H/**RP68**/RD4
33	AN8/CMP4C/PGA2P4/**RP49**/RC1	73	PWM6L/RD15
34	OSCI/CLKI/AN6/CMP3C/CMP4A/ISRC2/**RP33**/RB1	74	PWM7L/RE14
35	OSC2/CLKO/AN7/CMP3D/CMP4B/PGA1N2/**RP34**/RB2	75	PWM7H/RE15
36	AN16/**RP66**/RD2	76	TMS/PWM3H/**RP43**/RB11
37	FLT19/RE6	77	TCK/PWM3L/**RP44**/RB12
38	FLT20/RE7	78	PWM2H/**RP45**/RB13
39	ASDA2/**RP63**/RC15	79	PWM2L/**RP46**/RB14
40	PGED2/DACOUT1/AN18/ASCL2/INT0/**RP35**/RB3	80	PWM4H/**RP65**/RD1

Legend: **Shaded pins** are up to 5 VDC tolerant.
RPn represents remappable peripheral functions. See Table 11-12 and Table 11-13 for the complete list of remappable sources.

TABLE 4-14: SFR BLOCK C00h-D00h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
PWM			FCLCON3	C64	0000000000000000	IOCON6	CC2	1100000000000000
PTCON	C00	0000000000000000	PDC3	C66	0000000000000000	FCLCON6	CC4	0000000000000000
PTCON2	C02	0000000000000000	PHASE3	C68	0000000000000000	PDC6	CC6	0000000000000000
PTPER	C04	1111111111111000	DTR3	C6A	0000000000000000	PHASE6	CC8	0000000000000000
SEVTCMP	C06	0000000000000000	ALTDTR3	C6C	0000000000000000	DTR6	CCA	0000000000000000
MDC	C0A	0000000000000000	SDC3	C6E	0000000000000000	ALTDTR6	CCC	0000000000000000
STCON	C0E	0000000000000000	SPHASE3	C70	0000000000000000	SDC6	CCE	0000000000000000
STCON2	C10	0000000000000000	TRIG3	C72	0000000000000000	SPHASE6	CD0	0000000000000000
STPER	C12	1111111111111000	TRGCON3	C74	0000000000000000	TRIG6	CD2	0000000000000000
SSEVTCMP	C14	0000000000000000	STRIG3	C76	0000000000000000	TRGCON6	CD4	0000000000000000
CHOP	C1A	0000000000000000	PWMCAP3	C78	0000000000000000	STRIG6	CD6	0000000000000000
PWMKEY	C1E	xxxxxxxxxxxxxxxx	LEBCON3	C7A	0000000000000000	PWMCAP6	CD8	0000000000000000
PWM Generator			LEBDLY3	C7C	0000000000000000	LEBCON6	CDA	0000000000000000
PWMCON1	C20	0000000000000000	AUXCON3	C7E	0000000000000000	LEBDLY6	CDC	0000000000000000
IOCON1	C22	1100000000000000	PWMCON4	C80	0000000000000000	AUXCON6	CDE	0000000000000000
FCLCON1	C24	0000000000000000	IOCON4	C82	1100000000000000	PWMCON7	CE0	0000000000000000
PDC1	C26	0000000000000000	FCLCON4	C84	0000000000000000	IOCON7	CE2	1100000000000000
PHASE1	C28	0000000000000000	PDC4	C86	0000000000000000	FCLCON7	CE4	0000000000000000
DTR1	C2A	0000000000000000	PHASE4	C88	0000000000000000	PDC7	CE6	0000000000000000
ALTDTR1	C2C	0000000000000000	DTR4	C8A	0000000000000000	PHASE7	CE8	0000000000000000
SDC1	C2E	0000000000000000	ALTDTR4	C8C	0000000000000000	DTR7	CEA	0000000000000000
SPHASE1	C30	0000000000000000	SDC4	C8E	0000000000000000	ALTDTR7	CEC	0000000000000000
TRIG1	C32	0000000000000000	SPHASE4	C90	0000000000000000	SDC7	CEE	0000000000000000
TRGCON1	C34	0000000000000000	TRIG4	C92	0000000000000000	SPHASE7	CF0	0000000000000000
STRIG1	C36	0000000000000000	TRGCON4	C94	0000000000000000	TRIG7	CF2	0000000000000000
PWMCAP1	C38	0000000000000000	STRIG4	C96	0000000000000000	TRGCON7	CF4	0000000000000000
LEBCON1	C3A	0000000000000000	PWMCAP4	C98	0000000000000000	STRIG7	CF6	0000000000000000
LEBDLY1	C3C	0000000000000000	LEBCON4	C9A	0000000000000000	PWMCAP7	CF8	0000000000000000
AUXCON1	C3E	0000000000000000	LEBDLY4	C9C	0000000000000000	LEBCON7	CFA	0000000000000000
PWMCON2	C40	0000000000000000	AUXCON4	C9E	0000000000000000	LEBDLY7	CFC	0000000000000000
IOCON2	C42	1100000000000000	PWMCON5	CA0	0000000000000000	AUXCON7	CFE	0000000000000000
FCLCON2	C44	0000000000000000	IOCON5	CA2	1100000000000000	PWMCON8	D00	0000000000000000
PDC2	C46	0000000000000000	FCLCON5	CA4	0000000000000000	IOCON8	D02	1100000000000000
PHASE2	C48	0000000000000000	PDC5	CA6	0000000000000000	FCLCON8	D04	0000000000000000
DTR2	C4A	0000000000000000	PHASE5	CA8	0000000000000000	PDC8	D06	0000000000000000
ALTDTR2	C4C	0000000000000000	DTR5	CAA	0000000000000000	PHASE8	D08	0000000000000000
SDC2	C4E	0000000000000000	ALTDTR5	CAC	0000000000000000	ALTDTR8	D0C	0000000000000000
SPHASE2	C50	0000000000000000	SDC5	CAE	0000000000000000	SDC8	D0E	0000000000000000
TRIG2	C52	0000000000000000	SPHASE5	CB0	0000000000000000	SPHASE8	D10	0000000000000000
TRGCON2	C54	0000000000000000	TRIG5	CB2	0000000000000000	TRIG8	D12	0000000000000000
STRIG2	C56	0000000000000000	TRGCON5	CB4	0000000000000000	TRGCON8	D14	0000000000000000
PWMCAP2	C58	0000000000000000	STRIG5	CB6	0000000000000000	STRIG8	D16	0000000000000000
LEBCON2	C5A	0000000000000000	PWMCAP5	CB8	0000000000000000	PWMCAP8	D18	0000000000000000
LEBDLY2	C5C	0000000000000000	LEBCON5	CBA	0000000000000000	LEBCON8	D1A	0000000000000000
AUXCON2	C5E	0000000000000000	LEBDLY5	CBC	0000000000000000	LEBDLY8	D1C	0000000000000000
PWMCON3	C60	0000000000000000	AUXCON5	CBE	0000000000000000	AUXCON8	D1E	0000000000000000
IOCON3	C62	1100000000000000	PWMCON6	CC0	0000000000000000			

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

4.9 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGS70X/80X family architecture uses a 24-bit wide Program Space (PS) and a 16-bit wide Data Space (DS). The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGS70X/80X family devices provides two methods by which Program Space can be accessed during operation:

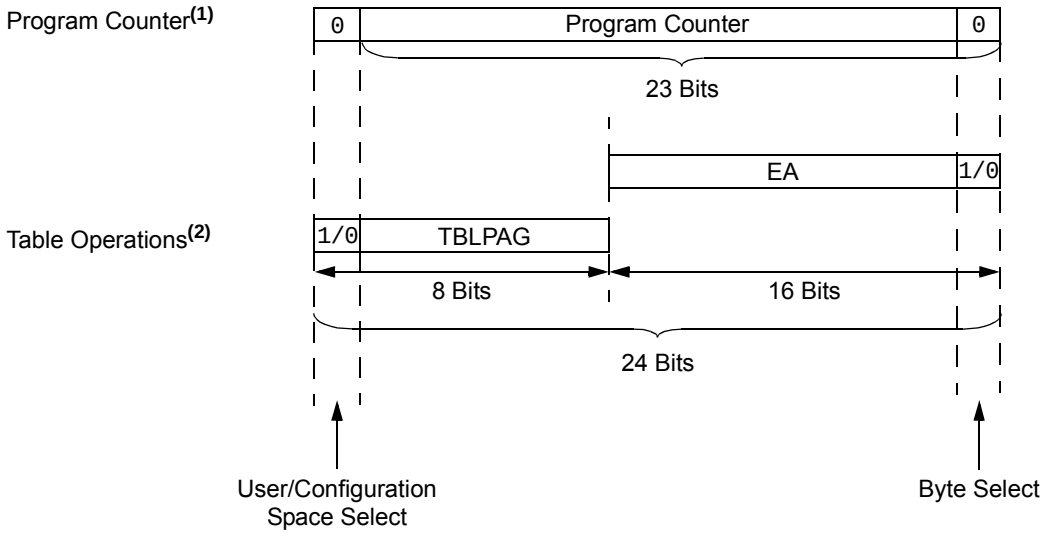
- Using table instructions to access individual bytes or words anywhere in the Program Space
- Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-19: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	<22:16>	<15>	<14:1>	<0>
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		0xxx xxxx xxxx xxxx xxxx xxx0				
TBLRD/TBLWT (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		0xxx xxxx		xxxx xxxx xxxx xxxx		
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		1xxx xxxx		xxxx xxxx xxxx xxxx		

FIGURE 4-12: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION



Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

REGISTER 5-1: NVMCON: NONVOLATILE MEMORY (NVM) CONTROL REGISTER

R/SO-0(1)	R/W-0(1)	R/W-0(1)	R/W-0	R/C-0	R-0	R/W-0	R/C-0
WR	WREN	WRERR	NVMSIDL(2)	SFTSWP(6)	P2ACTIV(6)	RPDF	URERR
bit 15							bit 8

U-0	U-0	U-0	U-0	R/W-0(1)	R/W-0(1)	R/W-0(1)	R/W-0(1)
—	—	—	—	NVMOP3(3,4)	NVMOP2(3,4)	NVMOP1(3,4)	NVMOP0(3,4)
bit 7							bit 0

Legend:	C = Clearable bit	SO = Settable Only bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **WR:** Write Control bit(1)
- 1 = Initiates a Program Flash Memory or erase operation; the operation is self-timed and the bit is cleared by hardware once the operation is complete
- 0 = Program or erase operation is complete and inactive

bit 14 **WREN:** Write Enable bit(1)
- 1 = Enables Flash program/erase operations
- 0 = Inhibits Flash program/erase operations

bit 13 **WRERR:** Write Sequence Error Flag bit(1)
- 1 = An improper program or erase sequence attempt, or termination has occurred (bit is set automatically on any set attempt of the WR bit)
- 0 = The program or erase operation completed normally

bit 12 **NVMSIDL:** NVM Stop in Idle Control bit(2)
- 1 = Flash voltage regulator goes into Standby mode during Idle mode
- 0 = Flash voltage regulator is active during Idle mode

bit 11 **SFTSWP:** Partition Soft Swap Status bit(6)
- 1 = Partitions have been successfully swapped using the BOOTSWP instruction (soft swap)
- 0 = Awaiting successful partition swap using the BOOTSWP instruction or a device Reset will determine the Active Partition based on the FBTSEQ register

bit 10 **P2ACTIV:** Partition 2 Active Status bit(6)
- 1 = Partition 2 Flash is mapped into the active region
- 0 = Partition 1 Flash is mapped into the active region

bit 9 **RPDF:** Row Programming Data Format bit
- 1 = Row data to be stored in RAM is in compressed format
- 0 = Row data to be stored in RAM is in uncompressed format

bit 8 **URERR:** Row Programming Data Underrun Error bit
- 1 = Indicates row programming operation has been terminated
- 0 = No data underrun error is detected

bit 7-4 **Unimplemented:** Read as '0'

Note 1: These bits can only be reset on a POR.

2: If this bit is set, power consumption will be further reduced (I_{IDLE}) and upon exiting Idle mode, there is a delay (T_{VREG}) before Flash memory becomes operational.

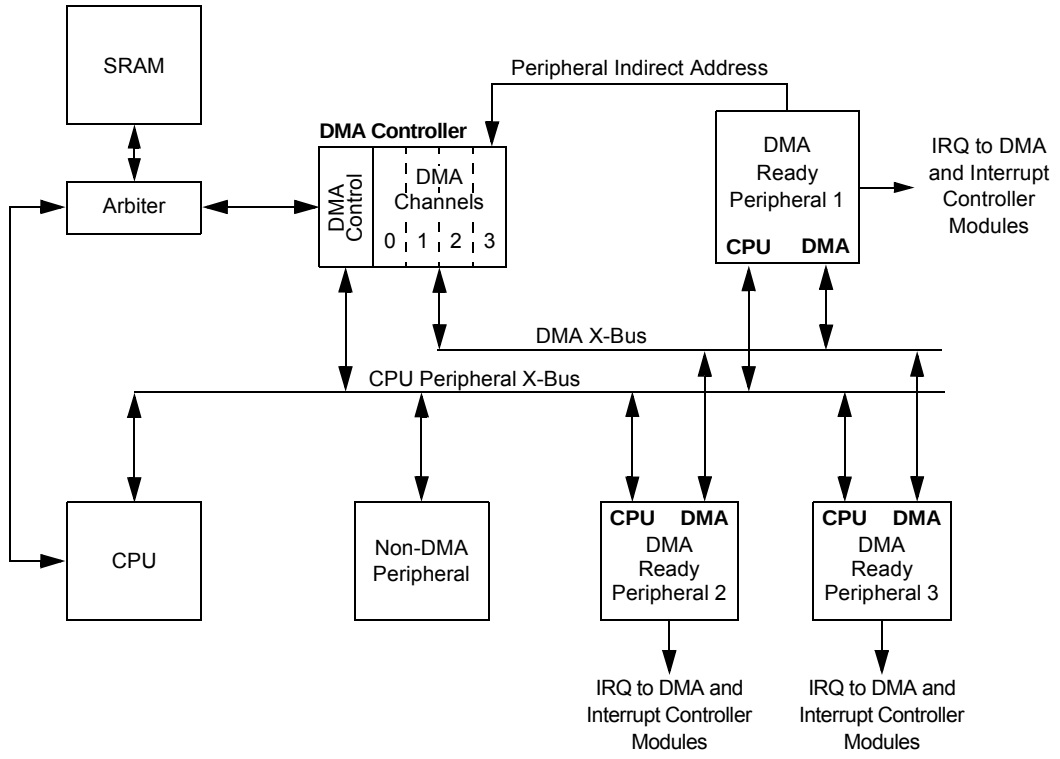
3: All other combinations of NVMOP<3:0> are unimplemented.

4: Execution of the PWRSAV instruction is ignored while any of the NVM operations are in progress.

5: Two adjacent words on a 4-word boundary are programmed during execution of this operation.

6: Only applicable when operating in Dual Partition mode.

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



Note: CPU and DMA address buses are not shown for clarity.

REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-1	R-1	R-1	R-1
—	—	—	—	LSTCH<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH<3:0>:** Last DMA Controller Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM8MD	PWM7MD	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SPI3MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PWM8MD:** PWM8 Module Disable bit
1 = PWM8 module is disabled
0 = PWM8 module is enabled

bit 14 **PWM7MD:** PWM7 Module Disable bit
1 = PWM7 module is disabled
0 = PWM7 module is enabled

bit 13 **PWM6MD:** PWM6 Module Disable bit
1 = PWM6 module is disabled
0 = PWM6 module is enabled

bit 12 **PWM5MD:** PWM5 Module Disable bit
1 = PWM5 module is disabled
0 = PWM5 module is enabled

bit 11 **PWM4MD:** PWM4 Module Disable bit
1 = PWM4 module is disabled
0 = PWM4 module is enabled

bit 10 **PWM3MD:** PWM3 Module Disable bit
1 = PWM3 module is disabled
0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit
1 = PWM1 module is disabled
0 = PWM1 module is enabled

bit 7-1 **Unimplemented:** Read as ‘0’

bit 0 **SPI3MD:** SPI3 Module Disable bit
1 = SPI3 module is disabled
0 = SPI3 module is enabled

TABLE 11-10: PORTE REGISTER MAP(1)

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISE	TRISE<15:0>															
PORTE	RE<15:0>															
LATE	LATE<15:0>															
ODCE	ODCE<15:0>															
CNENE	CNIEE<15:0>															
CNPUE	CNPUE<15:0>															
CNPDE	CNPDE<15:0>															
ANSELE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Legend: — = unimplemented, read as '0'.

Note 1: Refer to Table 11-5 for bit availability on each pin count variant.

REGISTER 11-17: RPINR13: PERIPHERAL PIN SELECT INPUT REGISTER 13

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT4R7	FLT4R6	FLT4R5	FLT4R4	FLT4R3	FLT4R2	FLT4R1	FLT4R0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLT3R7	FLT3R6	FLT3R5	FLT3R4	FLT3R3	FLT3R2	FLT3R1	FLT3R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **FLT4R<7:0>:** Assign PWM Fault 4 (FLT4) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **FLT3R<7:0>:** Assign PWM Fault 3 (FLT3) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

REGISTER 11-18: RPINR18: PERIPHERAL PIN SELECT INPUT REGISTER 18

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1CTSR7	U1CTSR6	U1CTSR5	U1CTSR4	U1CTSR3	U1CTSR2	U1CTSR1	U1CTSR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
U1RXR7	U1RXR6	U1RXR5	U1RXR4	U1RXR3	U1RXR2	U1RXR1	U1RXR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **U1CTSR<7:0>:** Assign UART1 Clear-to-Send ($\overline{\text{U1CTS}}$) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **U1RXR<7:0>:** Assign UART1 Receive (U1RX) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

REGISTER 11-45: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP53R6	RP53R5	RP53R4	RP53R3	RP53R2	RP53R1	RP53R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP52R6	RP52R5	RP52R4	RP52R3	RP52R2	RP52R1	RP52R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP53R<6:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP52R<6:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-46: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP55R6	RP55R5	RP55R4	RP55R3	RP55R2	RP55R1	RP55R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP54R6	RP54R5	RP54R4	RP54R3	RP54R2	RP54R1	RP54R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP55R<6:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP54R<6:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 16-10: MDC: PWMx MASTER DUTY CYCLE REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
MDC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **MDC<15:0>:** PWMx Master Duty Cycle Value bits

Note 1: The smallest pulse width that can be generated on the PWMx output corresponds to a value of 0x0008, while the maximum pulse width generated corresponds to a value of Period – 0x0008.

2: As the duty cycle gets closer to 0% or 100% of the PWMx period (0 to 40 ns, depending on the mode of operation), PWMx duty cycle resolution will increase from 1 to 3 LSBs.

REGISTER 16-11: PWMKEY: PWMx PROTECTION LOCK/UNLOCK KEY REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWMKEY<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PWMKEY<15:0>:** PWMx Protection Lock/Unlock Key Value bits

REGISTER 16-22: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (x = 1 to 8) (CONTINUED)

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select for PWMx Generator bits
11111 = Reserved
10001 = Reserved
10000 = Analog Comparator 4
01111 = Analog Comparator 3
01110 = Analog Comparator 2
01101 = Analog Comparator 1
01100 = Fault 12
01011 = Fault 11
01010 = Fault 10
01001 = Fault 9
01000 = Fault 8
00111 = Fault 7
00110 = Fault 6
00101 = Fault 5
00100 = Fault 4
00011 = Fault 3
00010 = Fault 2
00001 = Fault 1
00000 = Reserved

bit 2 **FLTPOL:** Fault Polarity for PWMx Generator bit(1)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWMx Generator bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (cycle)
00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (latched condition)

Note 1: These bits should be changed only when PTEN = 0 (PTCON<15>).

REGISTER 16-23: STRIGx: PWMx SECONDARY TRIGGER COMPARE VALUE REGISTER (x = 1 to 8)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STRGCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
STRGCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **STRGCMP<12:0>:** Secondary Trigger Compare Value bits
When the secondary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: STRIGx cannot generate the PWM trigger interrupts.

REGISTER 17-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 17-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-15)(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x +1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: Refer to Table 17-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

TABLE 17-2: PTG OUTPUT DESCRIPTIONS

PTG Output Number	PTG Output Description
PTGO0	Trigger/synchronization source for OC1
PTGO1	Trigger/synchronization source for OC2
PTGO2	Trigger/synchronization source for OC3
PTGO3	Trigger/synchronization source for OC4
PTGO4	Clock source for OC1
PTGO5	Clock source for OC2
PTGO6	Clock source for OC3
PTGO7	Clock source for OC4
PTGO8	Trigger/synchronization source for IC1
PTGO9	Trigger/synchronization source for IC2
PTGO10	Trigger/synchronization source for IC3
PTGO11	Trigger/synchronization source for IC4
PTGO12	Sample trigger for ADC
PTGO13	Reserved
PTGO14	Reserved
PTGO15	Reserved
PTGO16	PWM time base synchronous source for PWM3
PTGO17	PWM time base synchronous source for PWM4
PTGO18	PWM time base synchronous source for PWM5
PTGO19	PWM time base synchronous source for PWM6
PTGO20	Reserved
PTGO21	Reserved
PTGO22	Reserved
PTGO23	Reserved
PTGO24	Reserved
PTGO25	Reserved
PTGO26	CLC1 input
PTGO27	CLC2 input
PTGO28	CLC3 input
PTGO29	CLC4 input
PTGO30	PTG output to PPS input selection, RPI6
PTGO31	PTG output to PPS input selection, RPI7

REGISTER 23-3: CxVEC: CANx INTERRUPT CODE REGISTER

U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0
bit 15							bit 8

U-0	R-1	R-0	R-0	R-0	R-0	R-0	R-0
—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12-8 **FILHIT<4:0>:** Filter Hit Number bits

10000-11111 = Reserved
01111 = Filter 15
•
•
•
00001 = Filter 1
00000 = Filter 0

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **ICODE<6:0>:** Interrupt Flag Code bits

1000101-1111111 = Reserved
1000100 = FIFO almost full interrupt
1000011 = Receiver overflow interrupt
1000010 = Wake-up interrupt
1000001 = Error interrupt
1000000 = No interrupt
•
•
•
0010000-0111111 = Reserved
0001111 = RB15 buffer interrupt
•
•
•
0001001 = RB9 buffer interrupt
0001000 = RB8 buffer interrupt
0000111 = TRB7 buffer interrupt
0000110 = TRB6 buffer interrupt
0000101 = TRB5 buffer interrupt
0000100 = TRB4 buffer interrupt
0000011 = TRB3 buffer interrupt
0000010 = TRB2 buffer interrupt
0000001 = TRB1 buffer interrupt
0000000 = TRB0 buffer interrupt

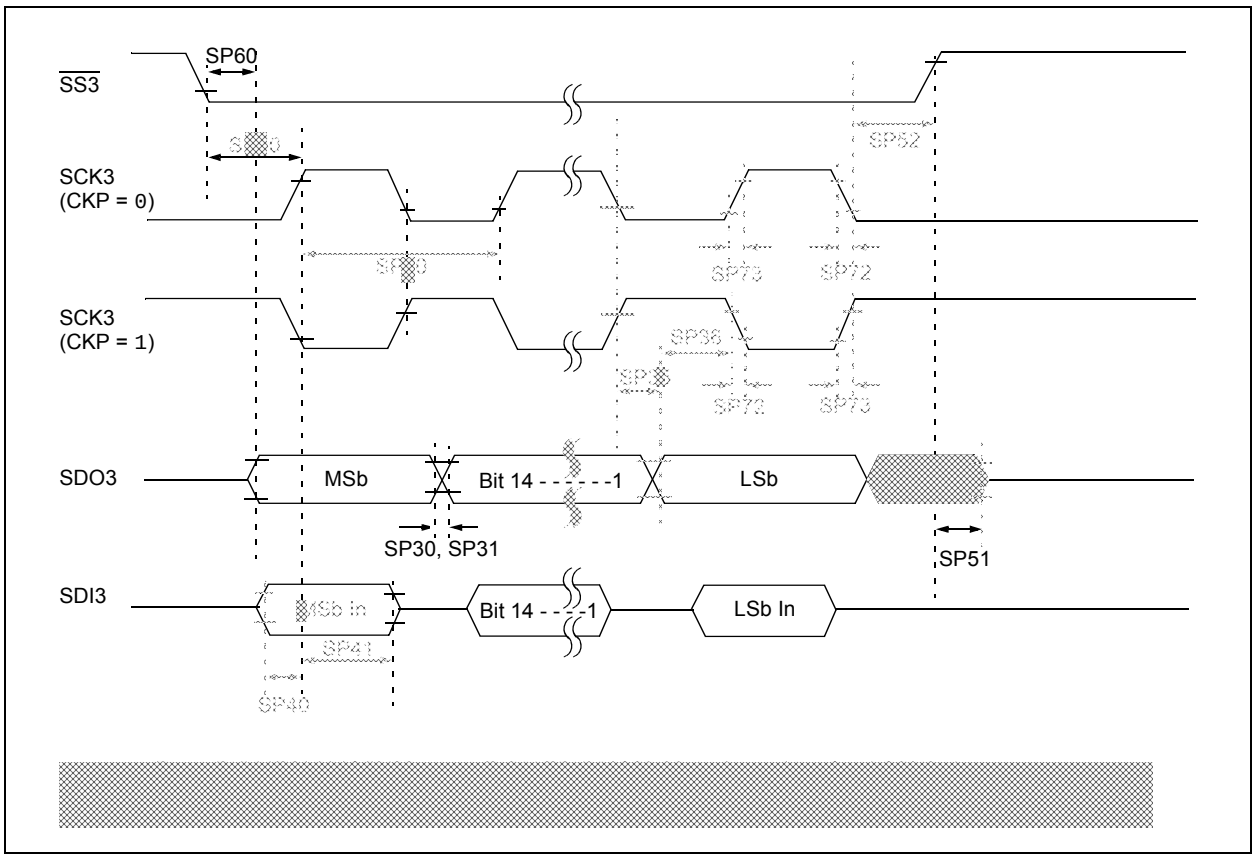
TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
CTXT4<2:0>	Alternate Working Register Set 4 Interrupt Priority Level (IPL) Select bits 111 = Reserved 110 = Assigned to IPL of 7 101 = Assigned to IPL of 6 100 = Assigned to IPL of 5 011 = Assigned to IPL of 4 010 = Assigned to IPL of 3 001 = Assigned to IPL of 2 000 = Assigned to IPL of 1
BTMODE<1:0>	Boot Mode Configuration bits 11 = Single Partition mode 10 = Dual Partition mode 01 = Protected Dual Partition mode 00 = Privileged Dual Partition mode

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

NOTES:

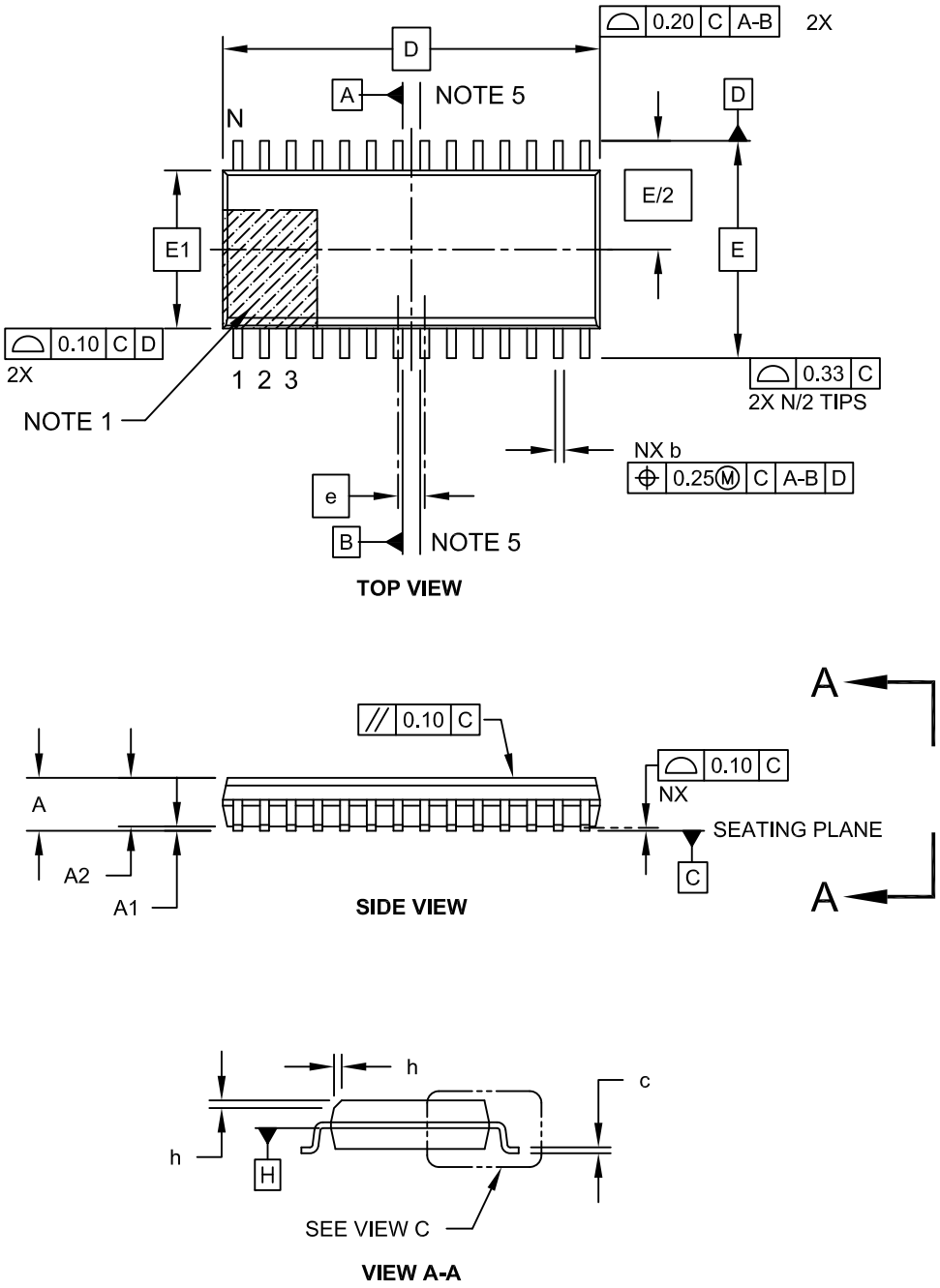
FIGURE 30-23: SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS(1,2)



32.2 Package Details

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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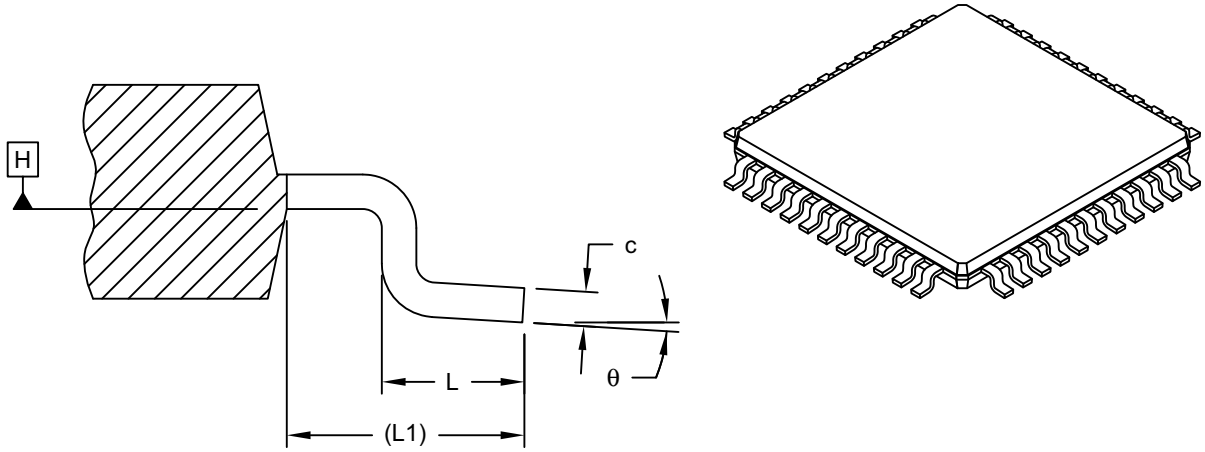
44-Lead Plastic Thin Quad Flatpack (PT) - 10x10x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



SECTION A-A

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	-	-	1.20
Standoff	A1	0.05	-	0.15
Molded Package Thickness	A2	0.95	1.00	1.05
Overall Width	E		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Width	b	0.30	0.37	0.45
Lead Thickness	c	0.09	-	0.20
Lead Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	3.5°	7°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Exact shape of each corner is optional.
3. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

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