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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, I ² S, POR, PWM, WDT
Number of I/O	67
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs708-e-pt

dsPIC33EPXXXGS70X/80X FAMILY

5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Dual Partition Flash Program Memory**” (DS70005156) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com)

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family devices contain internal Program Flash Memory for storing and executing application code. The memory is readable, writable and erasable during normal operation over the entire VDD range.

Flash memory can be programmed in three ways:

- In-Circuit Serial Programming™ (ICSP™) programming capability
- Enhanced In-Circuit Serial Programming (Enhanced ICSP)
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGS70X/80X family device to be serially programmed while in the end application circuit. This is done with a programming clock and programming data (PGECx/PGEDx) line, and three other lines for power (VDD), ground (VSS) and Master Clear (MCLR). This allows customers to

manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

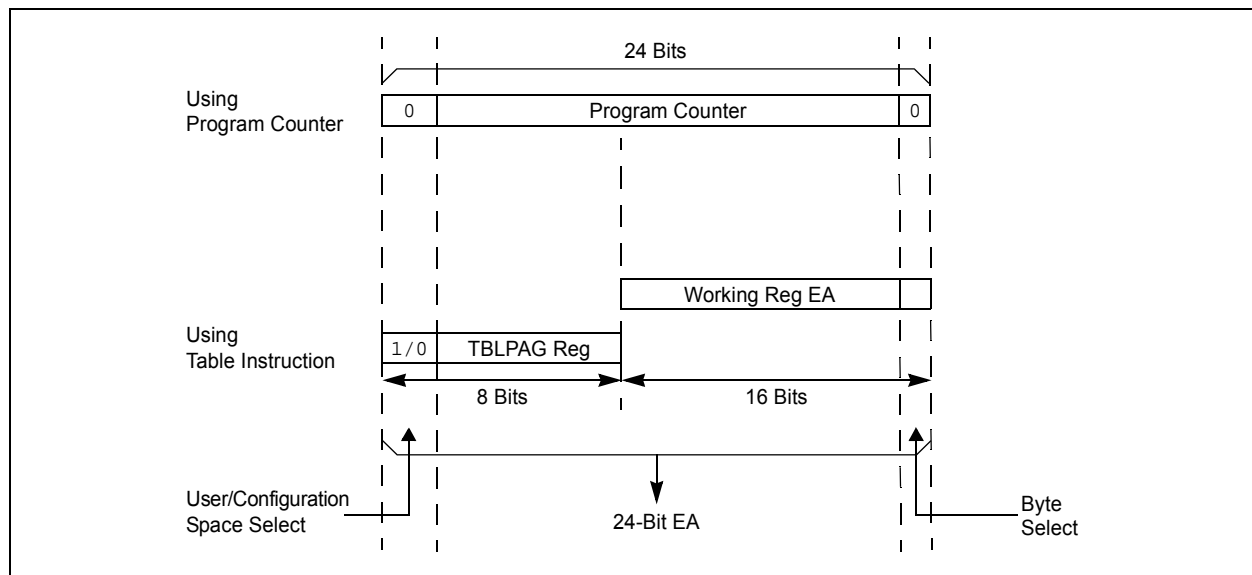
Enhanced In-Circuit Serial Programming uses an on-board bootloader, known as the Program Executive, to manage the programming process. Using an SPI data frame format, the Program Executive can erase, program and verify program memory. For more information on Enhanced ICSP, see the device programming specification.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data with a single program memory word and erase program memory in blocks or ‘pages’ of 512 instructions (1536 bytes) at a time.

5.1 Table Instructions and Flash Programming

Regardless of the method used, all programming of Flash memory is done with the Table Read and Table Write instructions. These instructions allow direct read and write access to the program memory space, from the data memory, while the device is in normal operating mode. The 24-bit target address in the program memory is formed using bits<7:0> of the TBLPAG register and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1. The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes. The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



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REGISTER 6-1: RCON: RESET CONTROL REGISTER⁽¹⁾ (CONTINUED)

bit 3	SLEEP: Wake-up from Sleep Flag bit 1 = Device has been in Sleep mode 0 = Device has not been in Sleep mode
bit 2	IDLE: Wake-up from Idle Flag bit 1 = Device has been in Idle mode 0 = Device has not been in Idle mode
bit 1	BOR: Brown-out Reset Flag bit 1 = A Brown-out Reset has occurred 0 = A Brown-out Reset has not occurred
bit 0	POR: Power-on Reset Flag bit 1 = A Power-on Reset has occurred 0 = A Power-on Reset has not occurred

- Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.
- 2:** If the WDTEN<1:0> Configuration bits are '11' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
SPI1 Error Interrupt	132	124	0x00010C	IFS7<12> SPI1IF	IEC7<12> SPI1IE	IPC31<2:0> SPI1IP<2:0>
SPI2 Error Interrupt	133	125	0x00010E	IFS7<13> SPI2IF	IEC7<13> SPI2IE	IPC31<6:4> SPI2IP<2:0>
SPI3 Error Interrupt	134	126	0x000110	IFS7<13> SPI3IF	IEC7<13> SPI3IE	IPC31<10:8> SPI3IP<2:0>
Reserved	135-145	127-137	0x000112-0x000126	—	—	—
CLC1 Interrupt	146	138	0x000128	IFS8<10> CLC1IF	IEC8<10> CLC1IE	IPC34<10:8> CLC1IP<2:0>
CLC2 Interrupt	147	139	0x00012A	IFS8<11> CLC2IF	IEC8<11> CLC2IE	IPC34<14:12> CLC2IP<2:0>
CLC3 Interrupt	148	140	0x00012C	IFS8<12> CLC3IF	IEC8<12> CLC3IE	IPC35<2:0> CLC3IP<2:0>
CLC4 Interrupt	149	141	0x00012E	IFS8<13> CLC4IF	IEC8<13> CLC4IE	IPC35<6:4> CLC4IP<2:0>
ICD – ICD Application	150	142	0x000130	IFS8<14> ICDIF	IEC8<14> ICDIE	IPC35<10:8> ICDIP<2:0>
JTAG – JTAG Programming	151	143	0x000132	IFS8<15> JTAGIF	IEC8<15> JTAGIE	IPC35<14:12> JTAGIP<2:0>
Reserved	152	144	0x000134	—	—	—
PTGSTEP – PTG Step	153	145	0x000136	IFS9<1> PTGSTEPIF	IEC9<1> PTGSTEPIE	IPC36<6:4> PTGSTEP<2:0>
PTGWDT – PTG WDT Time-out	154	146	0x000138	IFS9<2> PTGWDTIF	IEC9<2> PTGWDTIE	IPC36<10:8> PTGWDT<2:0>
PTG0 – PTG Interrupt Trigger 0	155	147	0x00013A	IFS9<3> PTG0IF	IEC9<3> PTG0IE	IPC36<14:12> PTG0IP<2:0>
PTG1 – PTG Interrupt Trigger 1	156	148	0x00013C	IFS9<4> PTG1IF	IEC9<4> PTG1IE	IPC37<2:0> PTG1IP<2:0>
PTG2 – PTG Interrupt Trigger 2	157	149	0x00013E	IFS9<5> PTG2IF	IEC9<5> PTG2IE	IPC37<6:4> PTG2IP<2:0>
PTG3 – PTG Interrupt Trigger 3	158	150	0x000140	IFS9<6> PTG3IF	IEC9<6> PTG3IE	IPC37<10:8> PTG3IP<2:0>
AN8 Conversion Done	159	151	0x000142	IFS9<7> AN8IF	IEC9<7> AN8IE	IPC37<14:12> AN8IP<2:0>
AN9 Conversion Done	160	152	0x000144	IFS9<8> AN9IF	IEC9<8> AN9IE	IPC38<2:0> AN9IP<2:0>
AN10 Conversion Done	161	153	0x000146	IFS9<9> AN10IF	IEC9<9> AN10IE	IPC38<6:4> AN10IP<2:0>
AN11 Conversion Done	162	154	0x000148	IFS9<10> AN11IF	IEC9<10> AN11IE	IPC38<10:8> AN11IP<2:0>
AN12 Conversion Done	163	155	0x00014A	IFS9<11> AN12IF	IEC9<11> AN12IE	IPC38<14:12> AN12IP<2:0>
AN13 Conversion Done	164	156	0x00014C	IFS9<12> AN13IF	IEC9<12> AN13IE	IPC39<2:0> AN13IP<2:0>
AN14 Conversion Done	165	157	0x00014E	IFS9<13> AN14IF	IEC9<13> AN14IE	IPC39<6:4> AN14IP<2:0>
AN15 Conversion Done	166	158	0x000150	IFS9<14> AN15IF	IEC9<14> AN15IE	IPC39<10:8> AN15IP<2:0>
AN16 Conversion Done	167	159	0x000152	IFS9<15> AN16IF	IEC9<15> AN16IE	IPC39<14:12> AN16IP<2:0>

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TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
AN17 Conversion Done	168	160	0x000154	IFS10<0> AN17IF	IEC10<0> AN17IE	IPC40<2:0> AN17IP<2:0>
AN18 Conversion Done	169	161	0x000156	IFS10<1> AN18IF	IEC10<1> AN18IE	IPC40<6:4> AN18IP<2:0>
AN19 Conversion Done	170	162	0x000158	IFS10<2> AN19IF	IEC10<2> AN19IE	IPC40<10:8> AN19IP<2:0>
AN20 Conversion Done	171	163	0x00015A	IFS10<3> AN20IF	IEC10<3> AN20IE	IPC40<14:12> AN20IP<2:0>
AN21 Conversion Done	172	164	0x00015C	IFS10<4> AN21IF	IEC10<4> AN21IE	IPC41<2:0> AN21IP<2:0>
Reserved	173-180	165-172	0x00015C-0x00016C	—	—	—
I2C1 – I2C1 Bus Collision	181	173	0x00016E	IFS10<13> I2C1IF	IEC10<13> I2C1IE	IPC43<6:4> I2C1IP<2:0>
I2C2 – I2C2 Bus Collision	182	174	0x000170	IFS10<14> I2C2IF	IEC10<14> I2C2IE	IPC43<10:8> I2C2IP<2:0>
Reserved	183-184	175-176	0x000172-0x000174	—	—	—
ADCMP0 – ADC Digital Comparator 0	185	177	0x000176	IFS11<1> ADCMP0IF	IEC11<1> ADCMP0IE	IPC44<6:4> ADCMP0IP<2:0>
ADCMP1 – ADC Digital Comparator 1	186	178	0x000178	IFS11<2> ADCMP1IF	IEC11<2> ADCMP1IE	IPC44<10:8> ADCMP1IP<2:0>
ADFLTR0 – ADC Filter 0	187	179	0x00017A	IFS11<3> ADFLTR0IF	IEC11<3> ADFLTR0IE	IPC44<14:12> ADFLTR0IP<2:0>
ADFLTR1 – ADC Filter 1	188	180	0x00017C	IFS11<4> ADFLTR1IF	IEC11<4> ADFLTR1IE	IPC45<2:0> ADFLTR1IP<2:0>
Reserved	189-253	181-245	0x00017E-0x000192	—	—	—

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REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15				bit 8			

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

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REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

bit 4-0 **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
.
.
.
00001 = Input divided by 3
00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV8
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>**: PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)
111111111 = 513
.
.
.
000110000 = 50 (default)
.
.
.
000000010 = 4
000000001 = 3
000000000 = 2

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REGISTER 10-5: PMD6: PERIPHERAL MODULE DISABLE CONTROL REGISTER 6

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PWM8MD	PWM7MD	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SPI3MD
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **PWM8MD:** PWM8 Module Disable bit

1 = PWM8 module is disabled

0 = PWM8 module is enabled

bit 14 **PWM7MD:** PWM7 Module Disable bit

1 = PWM7 module is disabled

0 = PWM7 module is enabled

bit 13 **PWM6MD:** PWM6 Module Disable bit

1 = PWM6 module is disabled

0 = PWM6 module is enabled

bit 12 **PWM5MD:** PWM5 Module Disable bit

1 = PWM5 module is disabled

0 = PWM5 module is enabled

bit 11 **PWM4MD:** PWM4 Module Disable bit

1 = PWM4 module is disabled

0 = PWM4 module is enabled

bit 10 **PWM3MD:** PWM3 Module Disable bit

1 = PWM3 module is disabled

0 = PWM3 module is enabled

bit 9 **PWM2MD:** PWM2 Module Disable bit

1 = PWM2 module is disabled

0 = PWM2 module is enabled

bit 8 **PWM1MD:** PWM1 Module Disable bit

1 = PWM1 module is disabled

0 = PWM1 module is enabled

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SPI3MD:** SPI3 Module Disable bit

1 = SPI3 module is disabled

0 = SPI3 module is enabled

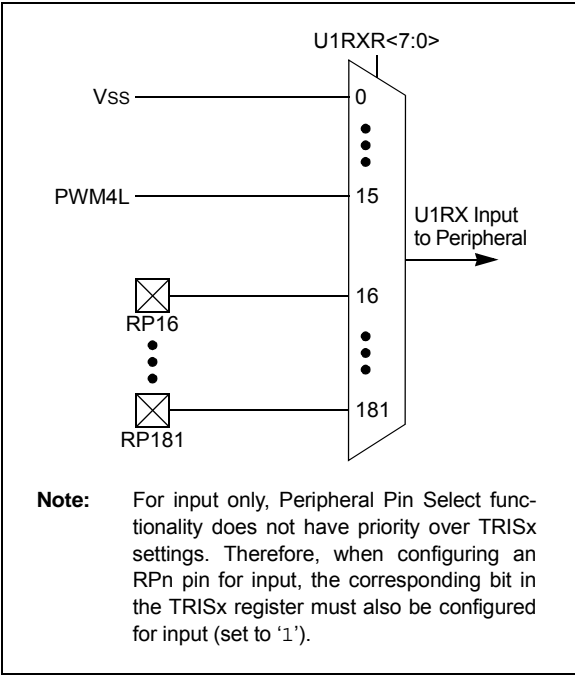
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11.6.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-9 through Register 11-32). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit index value maps the RPn pin with the corresponding value, or internal signal, to that peripheral. See Table 11-11 for a list of available inputs.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



11.6.4.1 Virtual Connections

The dsPIC33EPXXXGS70X/80X devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

TABLE 11-11: REMAPPABLE SOURCES

Remap Index	Output Function
0	Vss
1	CMP1
2	CMP2
3	CMP3
4	CMP4
5	PWM4H
6	PTGO30
7	PTGO31
8-11	Reserved
12	REFO
13	SYNCO1
14	SYNCO2
15	PWM4L
16-20	RP16-RP20
21-31	Reserved
32-41	RP32-RP41
42	Reserved
43-58	RP43-RP58
59	Reserved
60-76	RP60-RP76
77-175	Reserved
176-181	RP176-RP181

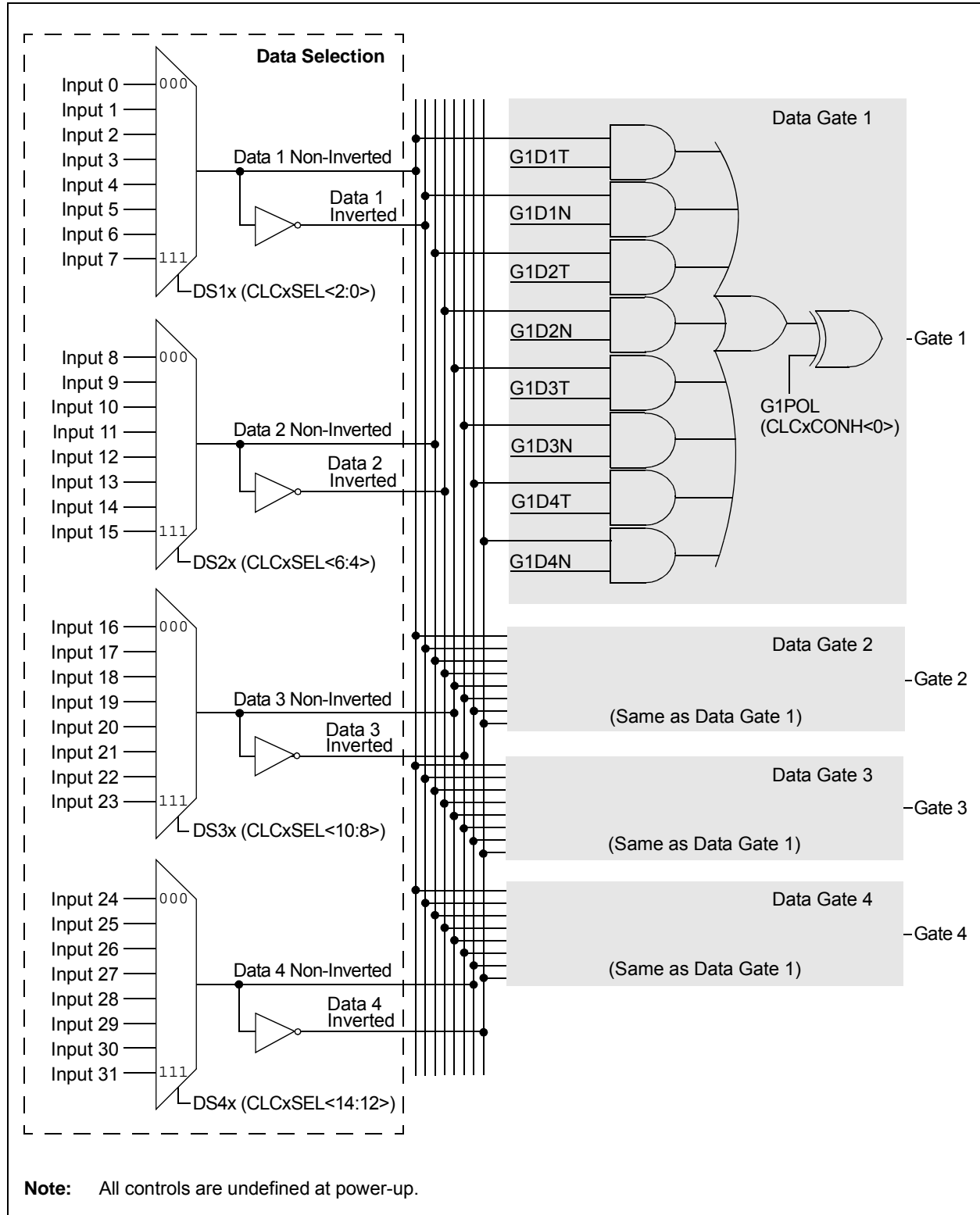
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REGISTER 19-3: I2CxSTAT: I2Cx STATUS REGISTER (CONTINUED)

bit 4	<p>P: Stop bit</p> <p>1 = Indicates that a Stop bit has been detected last 0 = Stop bit was not detected last</p> <p>Hardware is set or clear when a Start, Repeated Start or Stop is detected.</p>
bit 3	<p>S: Start bit</p> <p>1 = Indicates that a Start (or Repeated Start) bit has been detected last 0 = Start bit was not detected last</p> <p>Hardware is set or clear when a Start, Repeated Start or Stop is detected.</p>
bit 2	<p>R_W: Read/Write Information bit (I²C Slave mode only)</p> <p>1 = Read – Indicates data transfer is output from the slave 0 = Write – Indicates data transfer is input to the slave</p> <p>Hardware is set or clear after reception of an I²C device address byte.</p>
bit 1	<p>RBF: Receive Buffer Full Status bit</p> <p>1 = Receive is complete, I2CxRCV is full 0 = Receive is not complete, I2CxRCV is empty</p> <p>Hardware is set when I2CxRCV is written with a received byte. Hardware is clear when software reads I2CxRCV.</p>
bit 0	<p>TBF: Transmit Buffer Full Status bit</p> <p>1 = Transmit is in progress, I2CxTRN is full 0 = Transmit is complete, I2CxTRN is empty</p> <p>Hardware is set when software writes to I2CxTRN. Hardware is clear at completion of a data transmission.</p>

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FIGURE 21-3: CLCx INPUT SOURCE SELECTION DIAGRAM



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REGISTER 22-15: ADEIEL: ADC EARLY INTERRUPT ENABLE REGISTER LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<15:8>							
bit 15							
bit 8							

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EIEN<7:0>							
bit 7							
bit 0							

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **EIEN<15:0>**: Early Interrupt Enable for Corresponding Analog Inputs bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

REGISTER 22-16: ADEIEH: ADC EARLY INTERRUPT ENABLE REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							
bit 8							

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	EIEN<21:16>					
bit 7		bit 0					

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-6 **Unimplemented:** Read as '0'
bit 5-0 **EIEN<21:16>**: Early Interrupt Enable for Corresponding Analog Inputs bits
1 = Early interrupt is enabled for the channel
0 = Early interrupt is disabled for the channel

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REGISTER 23-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0
bit 7						bit 0	

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **F7MSK<1:0>**: Mask Source for Filter 7 bits

11 = Reserved

10 = Acceptance Mask 2 registers contain mask

01 = Acceptance Mask 1 registers contain mask

00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F6MSK<1:0>**: Mask Source for Filter 6 bits (same values as bits 15-14)

bit 11-10 **F5MSK<1:0>**: Mask Source for Filter 5 bits (same values as bits 15-14)

bit 9-8 **F4MSK<1:0>**: Mask Source for Filter 4 bits (same values as bits 15-14)

bit 7-6 **F3MSK<1:0>**: Mask Source for Filter 3 bits (same values as bits 15-14)

bit 5-4 **F2MSK<1:0>**: Mask Source for Filter 2 bits (same values as bits 15-14)

bit 3-2 **F1MSK<1:0>**: Mask Source for Filter 1 bits (same values as bits 15-14)

bit 1-0 **F0MSK<1:0>**: Mask Source for Filter 0 bits (same values as bits 15-14)

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REGISTER 23-19: CxFMSKSEL2: CANx FILTERS 15-8 MASK SELECTION REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-14 **F15MSK<1:0>**: Mask Source for Filter 15 bits

11 = Reserved

10 = Acceptance Mask 2 registers contain mask

01 = Acceptance Mask 1 registers contain mask

00 = Acceptance Mask 0 registers contain mask

bit 13-12 **F14MSK<1:0>**: Mask Source for Filter 14 bits (same values as bits 15-14)

bit 11-10 **F13MSK<1:0>**: Mask Source for Filter 13 bits (same values as bits 15-14)

bit 9-8 **F12MSK<1:0>**: Mask Source for Filter 12 bits (same values as bits 15-14)

bit 7-6 **F11MSK<1:0>**: Mask Source for Filter 11 bits (same values as bits 15-14)

bit 5-4 **F10MSK<1:0>**: Mask Source for Filter 10 bits (same values as bits 15-14)

bit 3-2 **F9MSK<1:0>**: Mask Source for Filter 9 bits (same values as bits 15-14)

bit 1-0 **F8MSK<1:0>**: Mask Source for Filter 8 bits (same values as bits 15-14)

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26.0 CONSTANT-CURRENT SOURCE

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The constant-current source module is a precision current generator and is used in conjunction with the ADC module to measure the resistance of external resistors connected to device pins.

26.1 Features Overview

The constant-current source module offers the following major features:

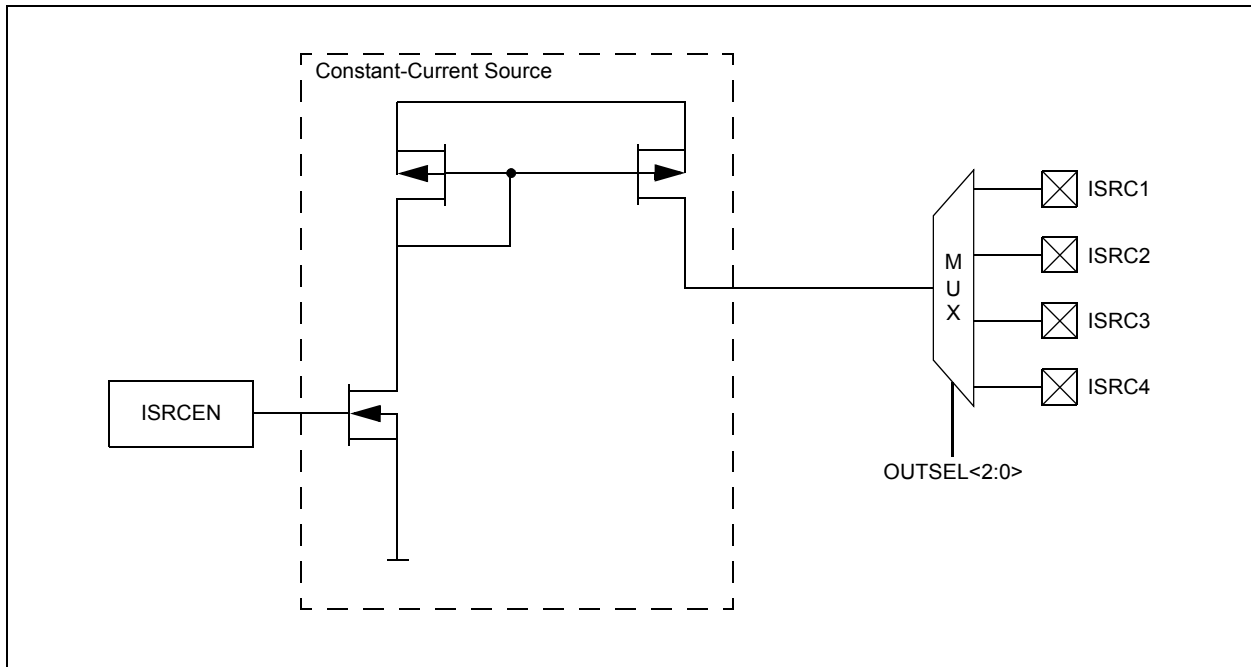
- Constant-Current Generator (10 μ A nominal)
- Internal Selectable Connection to One of Four Pins
- Enable/Disable bit

26.2 Module Description

Figure 26-1 shows a functional block diagram of the constant-current source module. It consists of a precision current generator with a nominal value of 10 μ A. The module can be enabled and disabled using the ISRCEN bit in the ISRCCON register. The output of the current generator is internally connected to a device pin. The dsPIC33EPXXXGS70X/80X family can have up to 4 selectable current source pins. The OUTSEL<2:0> bits in the ISRCCON register allow selection of the target pin.

The current source is calibrated during testing.

FIGURE 26-1: CONSTANT-CURRENT SOURCE MODULE BLOCK DIAGRAM



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TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
FNOSC<2:0>	Oscillator Selection bits 111 = Fast RC Oscillator with Divide-by-N (FRCDIVN) 110 = Fast RC Oscillator with Divide-by-16 101 = Low-Power RC Oscillator (LPRC) 100 = Reserved; do not use 011 = Primary Oscillator with PLL module (XT+PLL, HS+PLL, EC+PLL) 010 = Primary Oscillator (XT, HS, EC) 001 = Fast RC Oscillator with Divide-by-N with PLL module (FRCPLL) 000 = Fast RC Oscillator (FRC)
FCKSM<1:0>	Clock Switching Mode bits 1x = Clock switching is disabled, Fail-Safe Clock Monitor is disabled 01 = Clock switching is enabled, Fail-Safe Clock Monitor is disabled 00 = Clock switching is enabled, Fail-Safe Clock Monitor is enabled
IOL1WAY	Peripheral Pin Select Configuration bit 1 = Allows only one reconfiguration 0 = Allows multiple reconfigurations
OSCIOFNC	OSC2 Pin Function bit (except in XT and HS modes) 1 = OSC2 is the clock output 0 = OSC2 is a general purpose digital I/O pin
POSCMD<1:0>	Primary Oscillator Mode Select bits 11 = Primary Oscillator is disabled 10 = HS Crystal Oscillator mode 01 = XT Crystal Oscillator mode 00 = EC (External Clock) mode
WDTEN<1:0>	Watchdog Timer Enable bits 11 = Watchdog Timer is always enabled (LPRC oscillator cannot be disabled; clearing the SWDTEN bit in the RCON register will have no effect) 10 = Watchdog Timer is enabled/disabled by user software (LPRC can be disabled by clearing the SWDTEN bit in the RCON register) 01 = Watchdog Timer is enabled only while device is active and is disabled while in Sleep mode; software control is disabled in this mode 00 = Watchdog Timer and SWDTEN bit are disabled
WINDIS	Watchdog Timer Window Enable bit 1 = Watchdog Timer is in Non-Window mode 0 = Watchdog Timer is in Window mode
PLLKEN	PLL Lock Enable bit 1 = PLL lock is enabled 0 = PLL lock is disabled
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

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27.2 Device Calibration and Identification

The PGAx and current source modules on the dsPIC33EPXXXGS70X/80X family devices require Calibration Data registers to improve performance of the module over a wide operating range. These Calibration registers are read-only and are stored in configuration memory space. Prior to enabling the module, the calibration data must be read (TBLPAG and Table Read instruction) and loaded into its respective SFR registers. The device calibration addresses are shown in Table 27-3.

The dsPIC33EPXXXGS70X/80X devices have two Identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in Register 27-1 and Register 27-2.

TABLE 27-3: DEVICE CALIBRATION ADDRESSES⁽¹⁾

Calibration Name	Address	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGA1CAL	800E48	—	—	—	—	—	—	—	—	—	—	—	PGA1 Calibration Data					
PGA2CAL	800E4C	—	—	—	—	—	—	—	—	—	—	—	PGA2 Calibration Data					
ISRCCAL	800E78	—	—	—	—	—	—	—	—	—	—	—	Current Source Calibration Data					

Note 1: The calibration data must be copied into its respective SFR registers prior to enabling the module.

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FIGURE 30-7: OUTPUT COMPARE x MODULE (OCx) TIMING CHARACTERISTICS

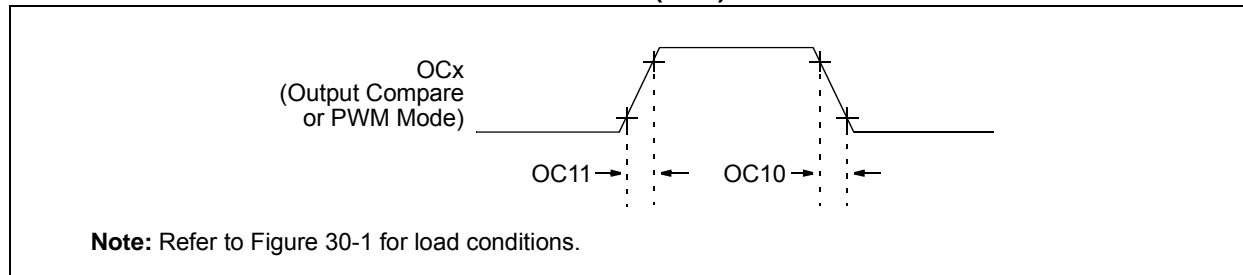


TABLE 30-28: OUTPUT COMPARE x MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC10	TccF	OCx Output Fall Time	—	—	—	ns	See Parameter DO32
OC11	TccR	OCx Output Rise Time	—	—	—	ns	See Parameter DO31

Note 1: These parameters are characterized but not tested in manufacturing.

FIGURE 30-8: OCx/PWMx MODULE TIMING CHARACTERISTICS

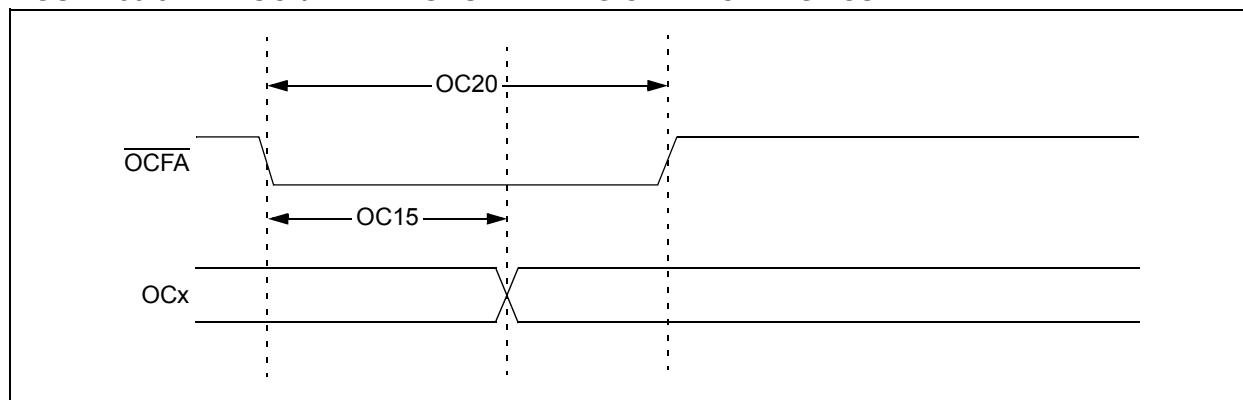


TABLE 30-29: OCx/PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic ⁽¹⁾	Min.	Typ.	Max.	Units	Conditions
OC15	TfD	Fault Input to PWMx I/O Change	—	—	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

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**TABLE 30-44: SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)
TIMING REQUIREMENTS⁽⁵⁾**

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions
SP70	FscP	Maximum SCK3 Input Frequency	—	—	25	MHz	(Note 3)
SP72	TscF	SCK3 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK3 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO3 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO3 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	Tsch2doV, TscL2doV	SDO3 Data Output Valid after SCK3 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO3 Data Output Setup to First SCK3 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI3 Data Input to SCK3 Edge	20	—	—	ns	
SP41	Tsch2diL, TscL2diL	Hold Time of SDI3 Data Input to SCK3 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS3} \downarrow$ to SCK3 \uparrow or SCK3 \downarrow Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS3} \uparrow$ to SDO3 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	Tsch2ssH, TscL2ssH	$\overline{SS3} \uparrow$ after SCK3 Edge	1.5 TCY + 40	—	—	ns	(Note 4)
SP60	TssL2doV	SDO3 Data Output Valid after $\overline{SS3}$ Edge	—	—	50	ns	

- Note 1:** These parameters are characterized, but are not tested in manufacturing.
Note 2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.
Note 3: The minimum clock period for SCK3 is 91 ns. Therefore, the SCK3 clock generated by the master must not violate this specification.
Note 4: Assumes 50 pF load on all SPI3 pins.
Note 5: For dsPIC33EPXXXGSX06 and dsPIC33EPXXXGSX08 devices with a fixed SCK3 pin.

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TABLE 30-53: ANALOG-TO-DIGITAL CONVERSION TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽²⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristics	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
Clock Parameters							
AD50	TAD	ADC Clock Period	14.28	—	—	ns	
Throughput Rate							
AD51	FTP	SH0-SH3	—	—	3.25	Msp/s	70 MHz ADC clock, 12 bits, no pending conversion at time of trigger
		SH4	—	—	3.25	Msp/s	

Note 1: These parameters are characterized but not tested in manufacturing.

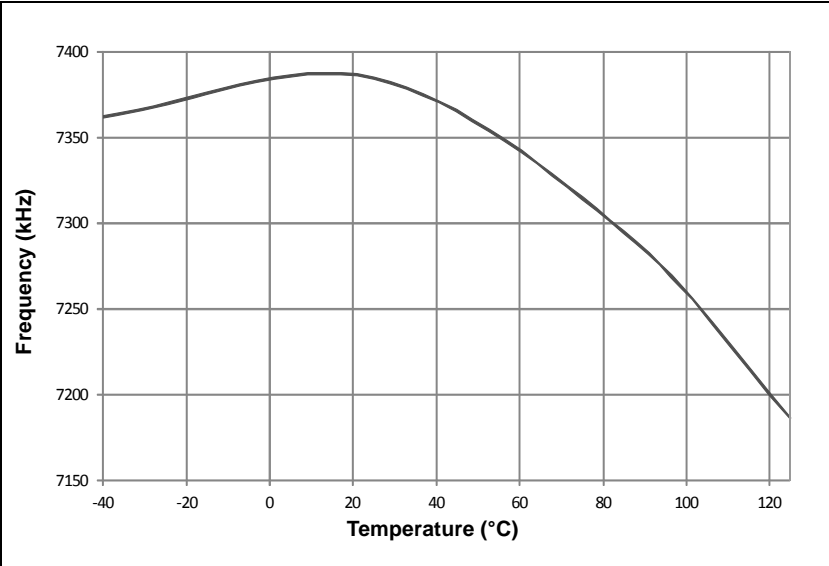
2: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

TABLE 30-54: HIGH-SPEED ANALOG COMPARATOR MODULE SPECIFICATIONS

AC/DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽²⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Comments
CM10	VIOFF	Input Offset Voltage	-35	±5	35	mV	
CM11	VICM	Input Common-Mode Voltage Range ⁽¹⁾	0	—	AVDD	V	
CM13	CMRR	Common-Mode Rejection Ratio	60	—	—	dB	
CM14	TRESP	Large Signal Response	—	15	—	ns	V+ input step of 100 mV while V- input is held at AVDD/2. Delay measured from analog input pin to PWMx output pin.
CM15	VHYST	Input Hysteresis	5	10	20	mV	Depends on HYSSEL<1:0>
CM16	TON	Comparator Enabled to Valid Output	—	—	1	μs	

Note 1: These parameters are for design guidance only and are not tested in manufacturing.

2: The comparator module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

FIGURE 31-9: TYPICAL FRC FREQUENCY @ $V_{DD} = 3.3V$ **FIGURE 31-10: TYPICAL LPRC FREQUENCY @ $V_{DD} = 3.3V$** 