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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, I²S, POR, PWM, WDT |
| Number of I/O | 67 |
| Program Memory Size | 128KB (43K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 22x12b; D/A 2x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 80-TQFP |
| Supplier Device Package | 80-TQFP (12x12) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs708-i-pt |

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### Errata

An errata sheet, describing minor operational differences from the data sheet and recommended workarounds, may exist for current devices. As device/documentation issues become known to us, we will publish an errata sheet. The errata will specify the revision of silicon and revision of document to which it applies.

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- Microchip's Worldwide Web site; **http://www.microchip.com**
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When contacting a sales office, please specify which device, revision of silicon and data sheet (include literature number) you are using.

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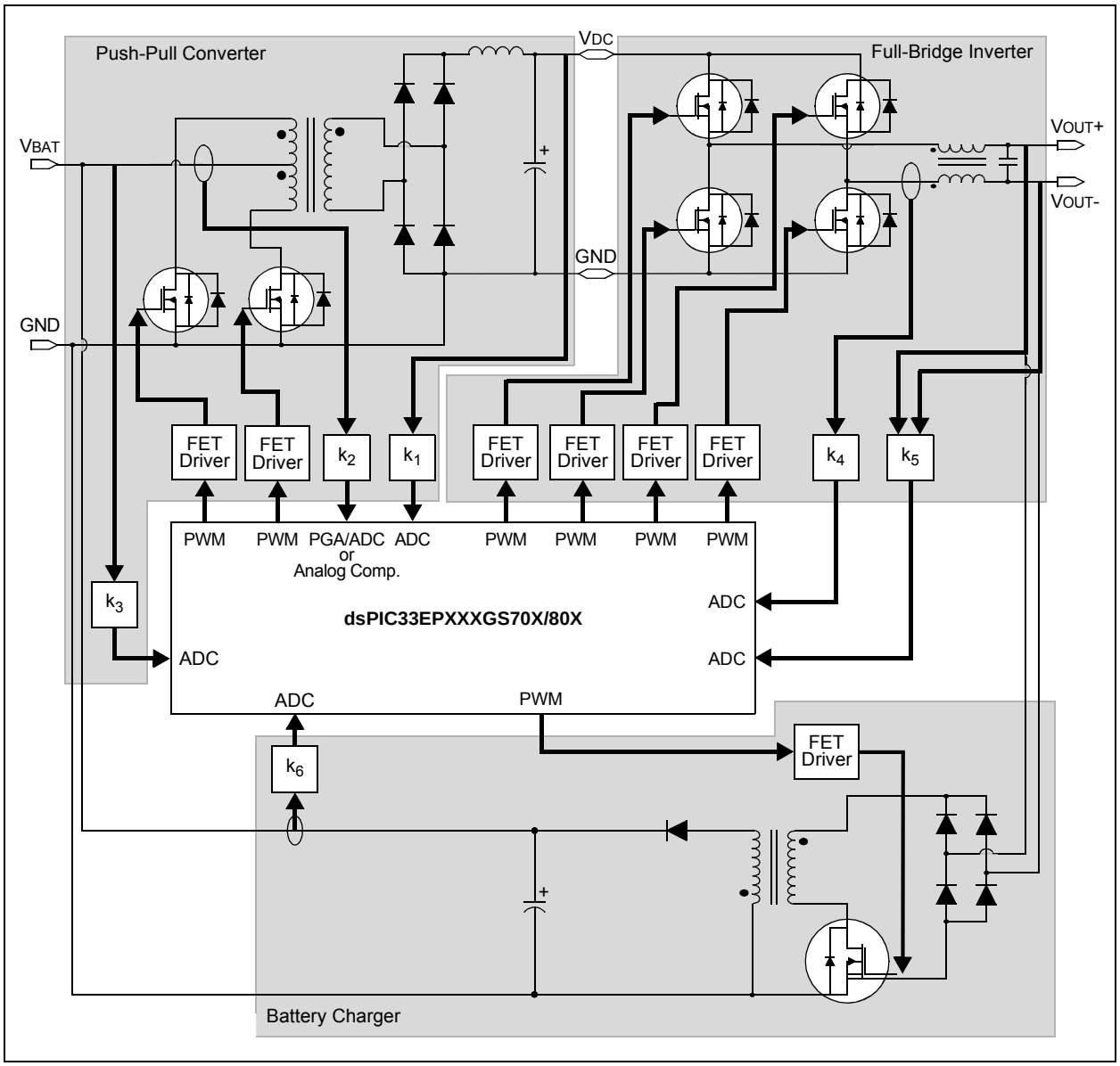
**FIGURE 2-6: OFF-LINE UPS**



## 6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 6.1.1 KEY RESOURCES

- **"Reset"** (DS70602) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1<11> T4IF | IEC1<11> T4IE | IPC6<14:12> T4IP<2:0> |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1<12> T5IF | IEC1<12> T5IE | IPC7<2:0> T5IP<2:0> |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> INT2IF | IEC1<13> INT2IE | IPC7<6:4> INT2IP<2:0> |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1<14> U2RXIF | IEC1<14> U2RXIE | IPC7<10:8> U2RXIP<2:0> |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1<15> U2TXIF | IEC1<15> U2TXIE | IPC7<14:12> U2TXIP<2:0> |
| SPI2TX – SPI2 Transfer Done | 40 | 32 | 0x000054 | IFS2<0> SPI2TXIF | IEC2<0> SPI2TXIE | IPC8<2:0> SPI2TXIP<2:0> |
| SPI2RX – SPI2 Receive Done | 41 | 33 | 0x000056 | IFS2<1> SPI2RXIF | IEC2<1> SPI2RXIE | IPC8<6:4> SPI2RXIP<2:0> |
| C1RX – CAN1 RX Data Ready | 42 | 34 | 0x000058 | IFS2<2> C1RXIF | IEC2<2> C1RXIE | IPC8<10:8> C1RXIP<2:0> |
| C1 – CAN1 Combined Error | 43 | 35 | 0x000059 | IFS2<3> C1IF | IEC2<3> C1IE | IPC8<14:12> C1IP<2:0> |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005A | IFS2<4> DMA3IF | IEC2<4> DMA3IE | IPC9<2:0> DMA3IP<2:0> |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2<5> IC3IF | IEC2<5> IC3IE | IPC9<6:4> IC3IP<2:0> |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2<6> IC4IF | IEC2<6> IC4IE | IPC9<10:8> IC4IP<2:0> |
| Reserved | 47-56 | 39-48 | 0x000062-0x000074 | — | — | — |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3<1> SI2C2IF | IEC3<1> SI2C2IE | IPC12<6:4> SI2C2IP<2:0> |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3<2> MI2C2IF | IEC3<2> MI2C2IE | IPC12<10:8> MI2C2IP<2:0> |
| Reserved | 59-61 | 51-53 | 0x00007A-0x00007E | — | — | — |
| INT4 – External Interrupt 4 | 62 | 54 | 0x000080 | IFS3<6> INT4IF | IEC3<6> INT4IE | IPC13<10:8> INT4IP<2:0> |
| C2RX – CAN2 RX Data Ready | 63 | 55 | 0x000082 | IFS3<7> C2RXIF | IEC3<7> C2RXIE | IPC13<14:12> C2RXIP<2:0> |
| C2 – CAN 2 Combined Error | 64 | 56 | 0x000083 | IFS3<8> C2IF | IEC3<8> C2IE | IPC14<2:0> C2IP<2:0> |
| PSEM – PWM Special Event Match | 65 | 57 | 0x000086 | IFS3<9> PSEMIF | IEC3<9> PSEMIE | IPC14<6:4> PSEMIP<2:0> |
| Reserved | 66-72 | 58-64 | 0x000088-0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4<1> U1EIF | IEC4<1> U1EIE | IPC16<6:4> U1EIP<2:0> |
| U2E – UART2 Error Interrupt | 74 | 66 | 0x000098 | IFS4<2> U2EIF | IEC4<2> U2EIE | IPC16<10:8> U2EIP<2:0> |
| Reserved | 75-77 | 67-69 | 0x00009A-0x0000A2 | — | — | — |
| C1TX – CAN1 TX Data Request | 78 | 70 | 0x0000A0 | IFS4<6> C1TXIF | IEC4<6> C1TXIE | IPC17<10:8> C1TXIP<2:0> |
| C2TX – CAN2 TX Data Request | 79 | 71 | 0x0000A | IFS4<7> C2TXIF | IEC4<7> C2TXIE | IPC17<14:12> C2TXIP<2:0> |
| Reserved | 80 | 72 | 0x0000A4 | — | — | — |

**REGISTER 11-49: RPOR16: PERIPHERAL PIN SELECT OUTPUT REGISTER 16**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP62R6 | RP62R5 | RP62R4 | RP62R3 | RP62R2 | RP62R1 | RP62R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP61R6 | RP61R5 | RP61R4 | RP61R3 | RP61R2 | RP61R1 | RP61R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP62R<6:0>:** Peripheral Output Function is Assigned to RP62 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP61R<6:0>:** Peripheral Output Function is Assigned to RP61 Output Pin bits (see Table 11-13 for peripheral function numbers)

**REGISTER 11-50: RPOR17: PERIPHERAL PIN SELECT OUTPUT REGISTER 17**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP64R6 | RP64R5 | RP64R4 | RP64R3 | RP64R2 | RP64R1 | RP64R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP63R6 | RP63R5 | RP63R4 | RP63R3 | RP63R2 | RP63R1 | RP63R0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP64R<6:0>:** Peripheral Output Function is Assigned to RP64 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP63R<6:0>:** Peripheral Output Function is Assigned to RP63 Output Pin bits (see Table 11-13 for peripheral function numbers)

## 13.0 TIMER2/3 AND TIMER4/5

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 operate in three modes:

- Two Independent 16-Bit Timers (e.g., Timer2 and Timer3) with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- Time Base for Input Capture and Output Compare modules (Timer2 and Timer3 only)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed previously, except for the event trigger; this is implemented only with Timer2/3. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1. T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word (lsw); Timer3 and Timer5 are the most significant word (msw) of the 32-bit timers.

**Note:** For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 and Timer5 interrupt flags.

A block diagram for an example 32-bit timer pair (Timer2/3 and Timer4/5) is shown in Figure 13-2.

### 13.1 Timer Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

#### 13.1.1 KEY RESOURCES

- **"Timers"** (DS70362) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 14.0 INPUT CAPTURE

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Input Capture with Dedicated Timer"** (DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The input capture module is useful in applications requiring frequency (period) and pulse measurements. The dsPIC33EPXXXGS70X/80X devices support four input capture channels.

Key features of the input capture module include:

- Hardware-Configurable for 32-Bit Operation in all modes by Cascading Two Adjacent modules
- Synchronous and Trigger modes of Output Compare Operation, with up to 21 User-Selectable Trigger/Sync Sources available
- A 4-Level FIFO Buffer for Capturing and Holding Timer Values for Several Events
- Configurable Interrupt Generation
- Up to Six Clock Sources available for each module, Driving a Separate Internal 16-Bit Counter

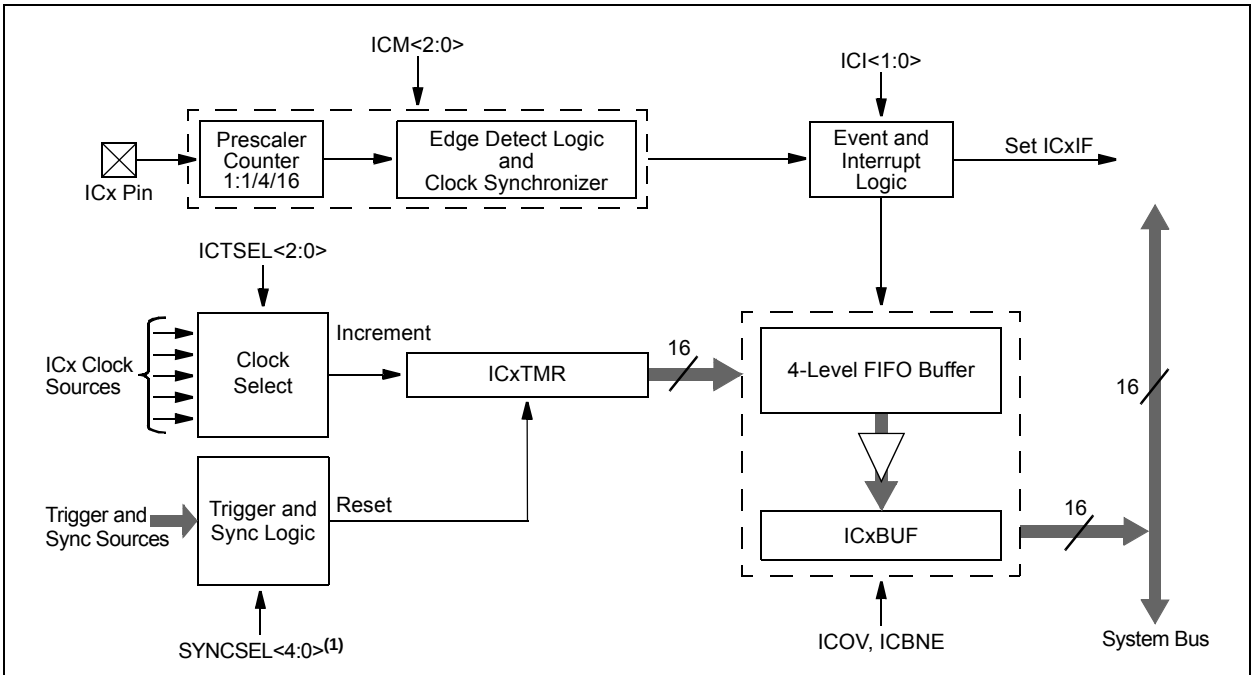
### 14.1 Input Capture Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

#### 14.1.1 KEY RESOURCES

- **"Input Capture with Dedicated Timer"** (DS70000352) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

**FIGURE 14-1: INPUT CAPTURE x MODULE BLOCK DIAGRAM**




**Note 1:** The trigger/sync source is enabled by default and is set to Timer3 as a source. This timer must be enabled for proper ICx module operation or the trigger/sync source must be changed to another source option.

**REGISTER 16-27: PWMCAPx: PWMx PRIMARY TIME BASE CAPTURE REGISTER (x = 1 to 8)**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<12:5>(1,2,3,4) | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| PWMCAP<4:0>(1,2,3,4) | | | | | — | — | — |
| bit 7 | | | | | | | bit 0 |

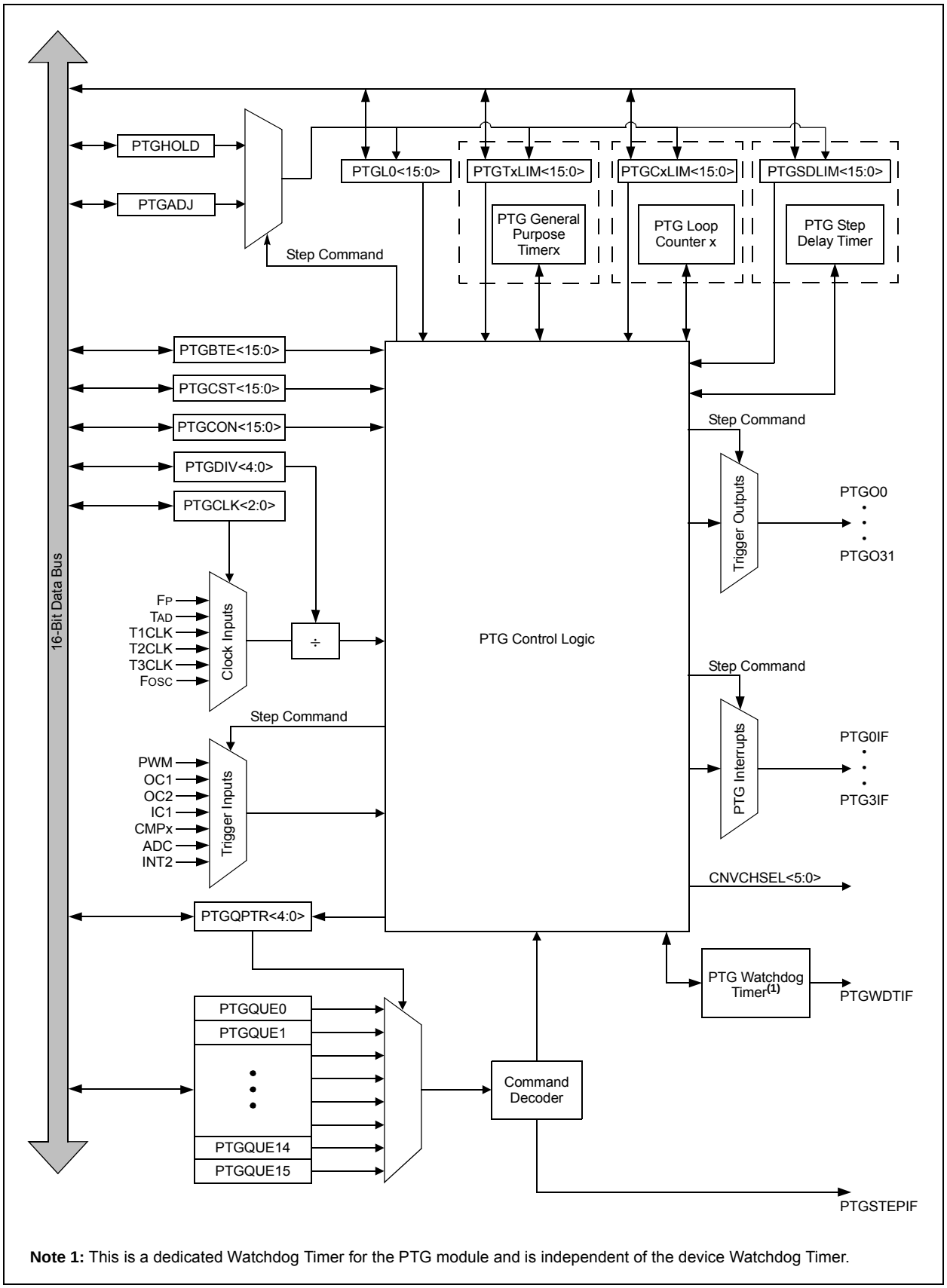
| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-3 **PWMCAP<12:0>:** PWMx Primary Time Base Capture Value bits(1,2,3,4)
The value in this register represents the captured PWMx time base value when a leading edge is detected on the current-limit input.

bit 2-0 **Unimplemented:** Read as '0'

**Note 1:** The capture feature is only available on a primary output (PWMxH).
**2:** This feature is active only after LEB processing on the current-limit input signal is complete.
**3:** The minimum capture resolution is 8.32 ns.
**4:** This feature can be used when the XPRES bit (PWMCONx<1>) is set to '0'.

**FIGURE 17-1: PTG BLOCK DIAGRAM**




**Note 1:** This is a dedicated Watchdog Timer for the PTG module and is independent of the device Watchdog Timer.

**REGISTER 17-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)**

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with Step delay is not executed on exit of command (regardless of PTGCTRL command)
10 = Single level detect with Step delay is executed on exit of command
01 = Continuous edge detect with Step delay is not executed on exit of command (regardless of PTGCTRL command)
00 = Continuous edge detect with Step delay is executed on exit of command

**Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.

**2:** This bit is only used with the PTGCTRL Step command software trigger option.

**REGISTER 17-2: PTGCON: PTG CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGCLK2 | PTGCLK1 | PTGCLK0 | PTGDIV4 | PTGDIV3 | PTGDIV2 | PTGDIV1 | PTGDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGPWD3 | PTGPWD2 | PTGPWD1 | PTGPWD0 | — | PTGWDT2 | PTGWDT1 | PTGWDT0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits
111 = CLC2
110 = CLC1
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be TAD
001 = PTG module clock source will be FOSC
000 = PTG module clock source will be FP

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as ‘0’

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits
111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

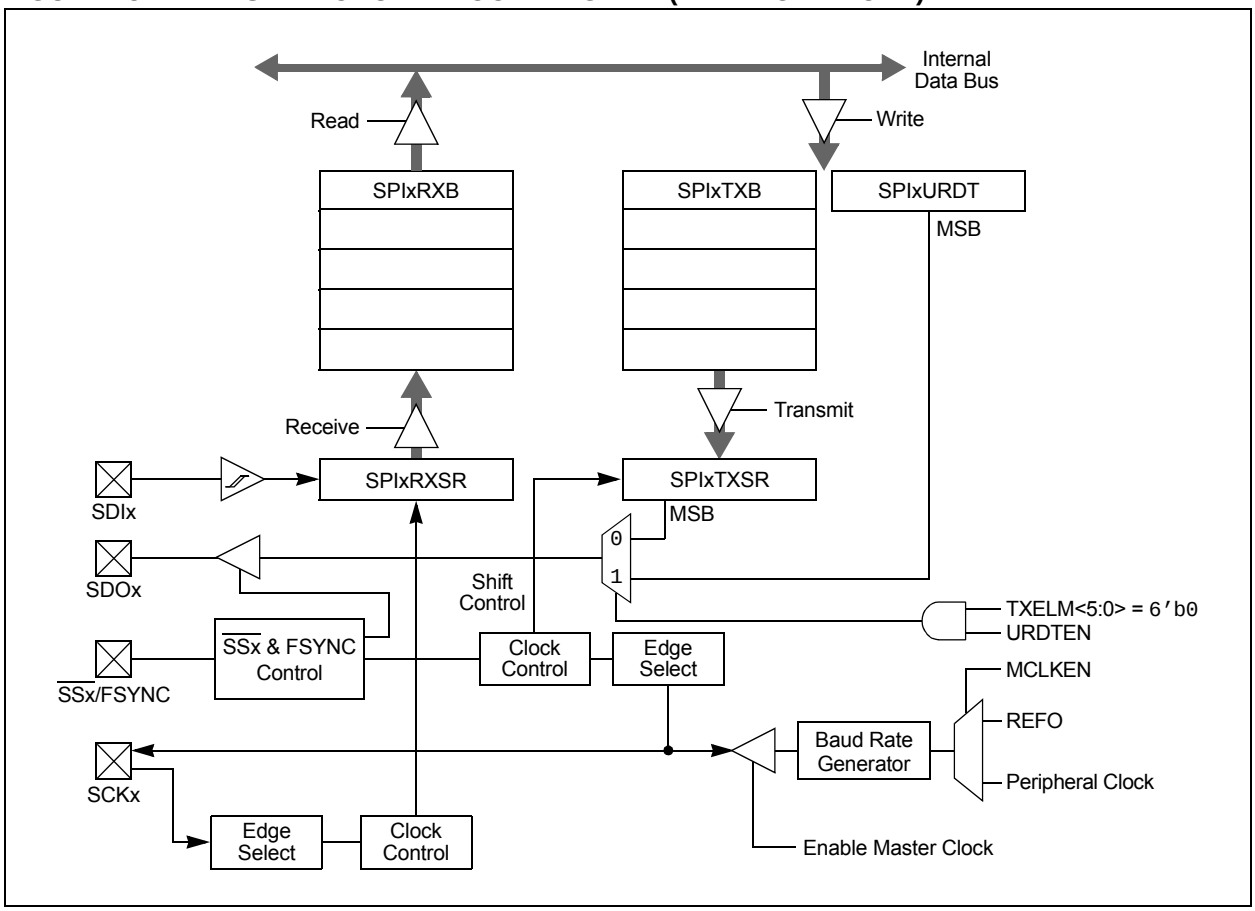
To set up the SPIx module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

**FIGURE 18-2: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)**



**REGISTER 18-7: SPIxIMSKH: SPIx INTERRUPT MASK REGISTER HIGH**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| RXWIEN | — | RXMSK5(1) | RXMSK4(1,4) | RXMSK3(1,3) | RXMSK2(1,2) | RXMSK1(1) | RXMSK0(1) |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TXWIEN | — | TXMSK5(1) | TXMSK4(1,4) | TXMSK3(1,3) | TXMSK2(1,2) | TXMSK1(1) | TXMSK0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **RXWIEN:** Receive Watermark Interrupt Enable bit
1 = Triggers receive buffer element watermark interrupt when RXMSK<5:0> ≤ RXELM<5:0>
0 = Disables receive buffer element watermark interrupt

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **RXMSK<5:0>:** RX Buffer Mask bits(1,2,3,4)
RX mask bits; used in conjunction with the RXWIEN bit.

bit 7 **TXWIEN:** Transmit Watermark Interrupt Enable bit
1 = Triggers transmit buffer element watermark interrupt when TXMSK<5:0> = TXELM<5:0>
0 = Disables transmit buffer element watermark interrupt

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **TXMSK<5:0>:** TX Buffer Mask bits(1,2,3,4)
TX mask bits; used in conjunction with the TXWIEN bit.

**Note 1:** Mask values higher than FIFODEPTH are not valid. The module will not trigger a match for any value in this case.
**2:** RXMSK2 and TXMSK2 bits are only present when FIFODEPTH = 8 or higher.
**3:** RXMSK3 and TXMSK3 bits are only present when FIFODEPTH = 16 or higher.
**4:** RXMSK4 and TXMSK4 bits are only present when FIFODEPTH = 32.

**REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)**

bit 5 **ADDEN:** Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled

bit 4 **RIDLE:** Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active

bit 3 **PERR:** Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected

bit 2 **FERR:** Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected

bit 1 **OERR:** Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receiver buffer and the UxRSR to the empty state

bit 0 **URXDA:** UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

**Note 1:** Refer to **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) in the *"dsPIC33/PIC24 Family Reference Manual"* for information on enabling the UARTx module for transmit operation.

**REGISTER 23-5: CxFIFO: CANx FIFO STATUS REGISTER**

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FBP5 | FBP4 | FBP3 | FBP2 | FBP1 | FBP0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| — | — | FNRB5 | FNRB4 | FNRB3 | FNRB2 | FNRB1 | FNRB0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

**REGISTER 23-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SIDx) = (Message SIDx) or if (Filter SIDx/EIDx) = (Message SIDx/EIDx))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

**REGISTER 23-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

## 23.4 CAN Message Buffers

CAN Message Buffers are part of RAM memory. They are not CAN Special Function Registers. The user application must directly write into the RAM area that is configured for CAN Message Buffers. The location and size of the buffer area is defined by the user application.

**BUFFER 21-1: CANx MESSAGE BUFFER WORD 0**

| U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | SID10 | SID9 | SID8 | SID7 | SID6 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | SRR | IDE |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-13 **Unimplemented:** Read as '0'

bit 12-2 **SID<10:0>:** Standard Identifier bits

bit 1 **SRR:** Substitute Remote Request bit

When IDE = 0:
1 = Message will request remote transmission
0 = Normal message

When IDE = 1:
The SRR bit must be set to '1'.

bit 0 **IDE:** Extended Identifier bit

1 = Message will transmit an Extended Identifier
0 = Message will transmit a Standard Identifier

**BUFFER 21-2: CANx MESSAGE BUFFER WORD 1**

| U-0 | U-0 | U-0 | U-0 | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| — | — | — | — | EID<17:14> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID<13:6> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **EID<17:6>:** Extended Identifier bits

**TABLE 30-48: I2Cx BUS DATA TIMING REQUIREMENTS (SLAVE MODE)**

| AC CHARACTERISTICS | | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic(3)** | | **Min.** | **Max.** | **Units** | **Conditions** |
| IS10 | TLO:SCL | Clock Low Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS11 | THI:SCL | Clock High Time | 100 kHz mode | 4.0 | — | µs | Device must operate at a minimum of 1.5 MHz |
| | | | 400 kHz mode | 0.6 | — | µs | Device must operate at a minimum of 10 MHz |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS20 | TF:SCL | SDAx and SCLx Fall Time | 100 kHz mode | — | 300 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 100 | ns | |
| IS21 | TR:SCL | SDAx and SCLx Rise Time | 100 kHz mode | — | 1000 | ns | CB is specified to be from 10 to 400 pF |
| | | | 400 kHz mode | 20 + 0.1 CB | 300 | ns | |
| | | | 1 MHz mode(1) | — | 300 | ns | |
| IS25 | TSU:DAT | Data Input Setup Time | 100 kHz mode | 250 | — | ns | |
| | | | 400 kHz mode | 100 | — | ns | |
| | | | 1 MHz mode(1) | 100 | — | ns | |
| IS26 | THD:DAT | Data Input Hold Time | 100 kHz mode | 0 | — | µs | |
| | | | 400 kHz mode | 0 | 0.9 | µs | |
| | | | 1 MHz mode(1) | 0 | 0.3 | µs | |
| IS30 | TSU:STA | Start Condition Setup Time | 100 kHz mode | 4.7 | — | µs | Only relevant for Repeated Start condition |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS31 | THD:STA | Start Condition Hold Time | 100 kHz mode | 4.0 | — | µs | After this period, the first clock pulse is generated |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | — | µs | |
| IS33 | TSU:STO | Stop Condition Setup Time | 100 kHz mode | 4.7 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.6 | — | µs | |
| IS34 | THD:STO | Stop Condition Hold Time | 100 kHz mode | 4 | — | µs | |
| | | | 400 kHz mode | 0.6 | — | µs | |
| | | | 1 MHz mode(1) | 0.25 | | µs | |
| IS40 | TAA:SCL | Output Valid from Clock | 100 kHz mode | 0 | 3500 | ns | |
| | | | 400 kHz mode | 0 | 1000 | ns | |
| | | | 1 MHz mode(1) | 0 | 350 | ns | |
| IS45 | TBF:SDA | Bus Free Time | 100 kHz mode | 4.7 | — | µs | Time the bus must be free before a new transmission can start |
| | | | 400 kHz mode | 1.3 | — | µs | |
| | | | 1 MHz mode(1) | 0.5 | — | µs | |
| IS50 | CB | Bus Capacitive Loading | | — | 400 | pF | |
| IS51 | TPGD | Pulse Gobbler Delay | | 65 | 390 | ns | **(Note 2)** |

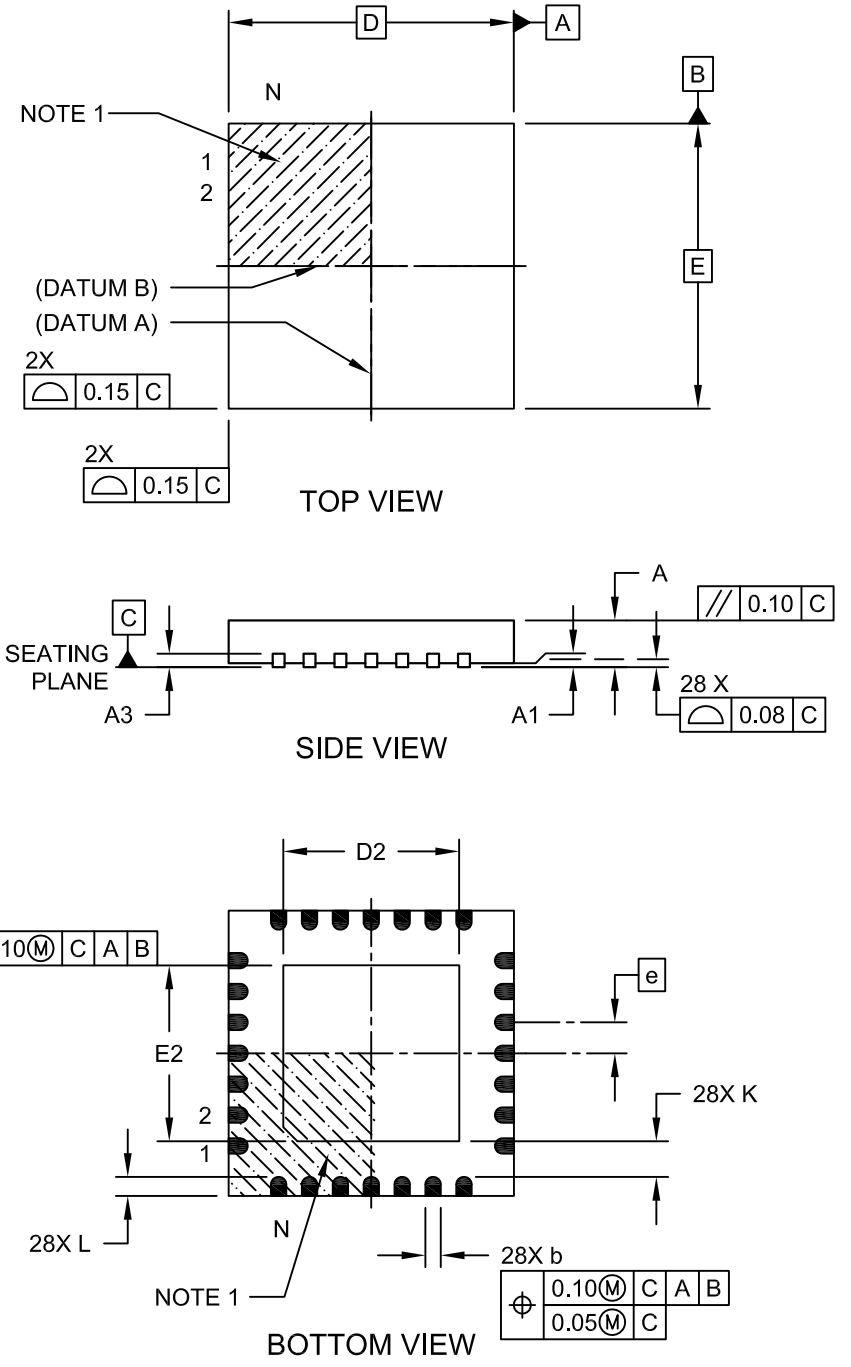
**Note 1:** Maximum Pin Capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

**2:** Typical value for this parameter is 130 ns.

**3:** These parameters are characterized but not tested in manufacturing.

**28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S]**
**With 0.40 mm Terminal Length**

| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|




Microchip Technology Drawing C04-124C Sheet 1 of 2

**NOTES:**