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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	·
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs804-e-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP128GS70X/80X DEVICES

4.2.1 PROGRAM MEMORY ORGANIZATION

The program memory space is organized in wordaddressable blocks. Although it is treated as 24 bits wide, it is more appropriate to think of each address of the program memory as a lower and upper word, with the upper byte of the upper word being unimplemented. The lower word always has an even address, while the upper word has an odd address (Figure 4-5).

Program memory addresses are always word-aligned on the lower word, and addresses are incremented or decremented by two, during code execution. This arrangement provides compatibility with data memory space addressing and makes data in the program memory space accessible.

4.2.2 INTERRUPT AND TRAP VECTORS

All dsPIC33EPXXXGS70X/80X family devices reserve the addresses between 0x000000 and 0x000200 for hard-coded program execution vectors. A hardware Reset vector is provided to redirect code execution from the default value of the PC on device Reset to the actual start of code. A GOTO instruction is programmed by the user application at address, 0x000000, of Flash memory, with the actual address for the start of code at address, 0x000002, of Flash memory.

A more detailed discussion of the Interrupt Vector Tables (IVTs) is provided in **Section 7.1** "Interrupt Vector Table".



FIGURE 4-5: PROGRAM MEMORY ORGANIZATION

5.2 RTSP Operation

The dsPIC33EPXXXGS70X/80X family Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a single page (8 rows or 512 instructions) of memory at a time and to program one row at a time. It is possible to program two instructions at a time as well.

The page erase and single row write blocks are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively. Figure 30-14 in **Section 30.0 "Electrical Characteristics"** lists the typical erase and programming times.

Row programming is performed by loading 192 bytes into data memory and then loading the address of the first byte in that row into the NVMSRCADR register. Once the write has been initiated, the device will automatically load the write latches and increment the NVMSRCADR and the NVMADR(U) registers until all bytes have been programmed. The RPDF bit (NVMCON<9>) selects the format of the stored data in RAM to be either compressed or uncompressed. See Figure 5-2 for data formatting. Compressed data helps to reduce the amount of required RAM by using the upper byte of the second word for the MSB of the second instruction.

The basic sequence for RTSP word programming is to use the TBLWTL and TBLWTH instructions to load two of the 24-bit instructions into the write latches found in configuration memory space. Refer to Figure 4-1 through Figure 4-4 for write latch addresses. Programming is performed by unlocking and setting the control bits in the NVMCON register.

All erase and program operations may optionally use the NVM interrupt to signal the successful completion of the operation. For example, when performing Flash write operations on the Inactive Partition in Dual Partition mode, where the CPU remains running, it is necessary to wait for the NVM interrupt before programming the next block of Flash program memory.

FIGURE 5-2: UNCOMPRESSED/ COMPRESSED FORMAT



5.3 **Programming Operations**

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished. Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of Program Flash Memory at a time on every other word address boundary (0x000000, 0x000004, 0x000008, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change. For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPS.

10.2.1 SLEEP MODE

The following occurs in Sleep mode:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption is reduced to a minimum, provided that no I/O pin is sourcing current.
- The Fail-Safe Clock Monitor does not operate, since the system clock source is disabled.
- The LPRC clock continues to run in Sleep mode if the WDT is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals can continue to operate. This includes items such as the Input Change Notification on the I/O ports or peripherals that use an external clock input.
- Any peripheral that requires the system clock source for its operation is disabled.

The device wakes up from Sleep mode on any of the these events:

- · Any interrupt source that is individually enabled
- · Any form of device Reset
- A WDT time-out

On wake-up from Sleep mode, the processor restarts with the same clock source that was active when Sleep mode was entered.

For optimal power savings, the internal regulator and the Flash regulator can be configured to go into standby when Sleep mode is entered by clearing the VREGS (RCON<8>) and VREGSF (RCON<11>) bits (default configuration).

If the application requires a faster wake-up time, and can accept higher current requirements, the VREGS (RCON<8>) and VREGSF (RCON<11>) bits can be set to keep the internal regulator and the Flash regulator active during Sleep mode.

10.2.2 IDLE MODE

The following occurs in Idle mode:

- The CPU stops executing instructions.
- · The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see Section 10.4 "Peripheral Module Disable").
- If the WDT or FSCM is enabled, the LPRC also remains active.

The device wakes from Idle mode on any of these events:

- · Any interrupt that is individually enabled
- · Any device Reset
- A WDT time-out

On wake-up from Idle mode, the clock is reapplied to the CPU and instruction execution will begin (2-4 clock cycles later), starting with the instruction following the PWRSAV instruction or the first instruction in the ISR.

All peripherals also have the option to discontinue operation when Idle mode is entered to allow for increased power savings. This option is selectable in the control register of each peripheral (for example, the TSIDL bit in the Timer1 Control register (T1CON<13>).

10.2.3 INTERRUPTS COINCIDENT WITH POWER SAVE INSTRUCTIONS

Any interrupt that coincides with the execution of a PWRSAV instruction is held off until entry into Sleep or Idle mode has completed. The device then wakes up from Sleep or Idle mode.

11.5 I/O Port Control Registers

REGISTER 11-1: TRISX: PORTX DATA DIRECTION CONTROL REGISTER⁽¹⁾

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			TRISx	<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			TRIS	x<7:0>			
bit 7							bit 0

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15-8 TRISx<15:0>: PORTx Data Direction Control bits

1 = The pin is an input

0 = The pin is an output

Note 1: See Table 11-1, Table 11-2, Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-2: PORTx: I/O PORTx REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
	PORTx<15:8>									
bit 15	bit 15 bit 8									
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			
			PORT	x<7:0>						
bit 7							bit 0			
Legend:										

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'		
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown	

bit 15-8 **PORTx<15:0>:** I/O PORTx bits

1 = The pin data is '1'

0 = The pin data is '0'

Note 1: See Table 11-1, Table 11-2, Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

U-0	R/W-0						
—	RP57R6	RP57R5	RP57R4	RP57R3	RP57R2	RP57R1	RP57R0
bit 15							bit 8
U-0	R/W-0						
—	RP56R6	RP56R5	RP56R4	RP56R3	RP56R2	RP56R1	RP56R0
bit 7							bit 0
Logondy							

REGISTER 11-47: RPOR14: PERIPHERAL PIN SELECT OUTPUT REGISTER 14

Legend:					
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'			
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

bit 15	Unimplemented: Read as '0'
bit 14-8	RP57R<6:0>: Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-13 for peripheral function numbers)
bit 7	Unimplemented: Read as '0'
bit 6-0	RP56R<6:0>: Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-48: RPOR15: PERIPHERAL PIN SELECT OUTPUT REGISTER 15

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP60R6	RP60R5	RP60R4	RP60R3	RP60R2	RP60R1	RP60R0
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP58R6	RP58R5	RP58R4	RP58R3	RP58R2	RP58R1	RP58R0
bit 7							bit 0
Legend:							
R = Readable	= Readable bit W = Writable bit U = Unimplemented bit, read as '0'			as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			nown

bit 15 Unimplemented: Read as '0'

bit 14-8 **RP60R<6:0>:** Peripheral Output Function is Assigned to RP60 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 Unimplemented: Read as '0'

bit 6-0 **RP58R<6:0>:** Peripheral Output Function is Assigned to RP58 Output Pin bits (see Table 11-13 for peripheral function numbers)



FIGURE 16-2: SIMPLIFIED CONCEPTUAL BLOCK DIAGRAM OF THE HIGH-SPEED PWM

	(A. 1								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0		
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—		
bit 15							bit 8		
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
		BCH ⁽¹⁾	BCL ⁽¹⁾	BPHH	BPHL	BPLH	BPLL		
bit 7							bit 0		
Legend:									
R = Reada	able bit	W = Writable	oit	U = Unimplen	nented bit, read	l as '0'			
-n = Value	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkn	iown		
bit 15		H Rising Edge 1	Frigger Enable	hit					
bit 10	1 = Rising ed	ae of PWMxH v	vill triager the	Leading-Edge [Blanking counte	er			
	0 = Leading-I	Edge Blanking i	gnores the risi	ng edge of PW	MxH				
bit 14	PHF: PWMxH	H Falling Edge	Frigger Enable	bit					
	1 = Falling ec	ge of PWMxH	will trigger the	Leading-Edge	Blanking count	er			
1:1.40	0 = Leading-l	Edge Blanking i	gnores the fall	ing edge of PW	/MxH				
bit 13	PLR: PWMxL		rigger Enable	Dit	looking counts	-			
	0 = Leading-	Edge Blanking i	anores the risi	_eading-Edge E	MxL	:f			
bit 12	PLF: PWMxL	Falling Edge T	rigger Enable	bit					
	1 = Falling ec	lge of PWMxL v	vill trigger the	Leading-Edge I	Blanking counte	er			
	0 = Leading-I	Edge Blanking i	gnores the fall	ing edge of PW	/MxL				
bit 11	FLTLEBEN:	Fault Input Lead	ding-Edge Blai	nking Enable bi	t				
	1 = Leading-	Edge Blanking i Edge Blanking i	s applied to the	e selected Faul	t input Fault input				
bit 10		0 = Leading-Edge Blanking is not applied to the selected Fault input							
	1 = Leading-	Edge Blanking i	s applied to the	e selected curre	ent-limit input				
	0 = Leading-I	Edge Blanking i	s not applied t	o the selected of	current-limit inp	ut			
bit 9-6	Unimplemen	ted: Read as 'd)'						
bit 5	BCH: Blankir	ng in Selected E	lanking Signa	l High Enable b	it ⁽¹⁾				
	1 = State blar 0 = No blanki	nking (of currenting when the se	l-limit and/or F	ault input signa g signal is high	ls) when the se	lected blanking	g signal is high		
bit 4	BCL: Blankin	ig in Selected B	lanking Signal	Low Enable bi	t(1)				
	1 = State blar 0 = No blanki	nking (of curren ing when the se	t-limit and/or F lected blanking	ault input signa g signal is low	als) when the se	elected blanking	g signal is low		
bit 3	BPHH: Blank	ing in PWMxH	High Enable b	it					
	1 = State blar	nking (of curren	t-limit and/or F	ault input signa	als) when the P	WMxH output i	s high		
hit 2				s nign F					
	1 = State blar	nig in EvvivixEl i aking (of curren	Low Enable DI	Sault innut signs	als) when the P	WMxH output i	slow		
	0 = No blanki	ing when the P	VMxH output i	s low			0.000		
Note 1:	The blanking sigr	nal is selected v	ia the BLANK	SEL<3:0> bits i	n the AUXCON	x register.			

REGISTER 16-24: LEBCONX: PWMx LEADING-EDGE BLANKING (LEB) CONTROL REGISTER (x = 1 to 8)

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REGISTER 19-1: I2CxCONL: I2Cx CONTROL REGISTER LOW (CONTINUED)

bit 6	 STREN: SCLx Clock Stretch Enable bit (when operating as I²C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive)
	Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive)
	 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware is clear at the end of the master Acknowledge sequence 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master)
	 1 = Enables Receive mode for I²C; hardware is clear at the end of the eighth bit of the master receive data byte 0 = Receive sequence is not in progress.
bit 2	PEN: Stop Condition Enable bit (when operating as I^2C master)
	 1 = Initiates Stop condition on SDAx and SCLx pins; hardware is clear at the end of the master Stop sequence
	0 = Stop condition is not in progress
bit 1	RSEN: Repeated Start Condition Enable bit (when operating as I ² C master)
	 1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Repeated Start sequence
	0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as I ² C master)
	1 = Initiates Start condition on SDAx and SCLx pins; hardware is clear at the end of the master Start sequence

0 = Start condition is not in progress

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	U-0	R/W-0, HC	R/W-0	R-0	R-1
UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN ⁽¹⁾	UTXBF	TRMT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R-1	R-0	R-0	R/C-0	R-0
URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA
bit 7							bit 0

Legend:	C = Clearable bit	HC = Hardware Clearable bit	t
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15,13 UTXISEL<1:0>: UARTx Transmission Interrupt Mode Selection bits

- 11 = Reserved; do not use
- 10 = Interrupt when a character is transferred to the Transmit Shift Register (TSR), and as a result, the transmit buffer becomes empty
- 01 = Interrupt when the last character is shifted out of the Transmit Shift Register; all transmit operations are completed
- 00 = Interrupt when a character is transferred to the Transmit Shift Register (this implies there is at least one character open in the transmit buffer)
- bit 14 UTXINV: UARTx Transmit Polarity Inversion bit
 - If IREN = 0: 1 = UxTX Idle state is '0'
 - 0 = UxTX Idle state is '1'
 - If IREN = 1:
 - $1 = IrDA^{\textcircled{R}}$ encoded, UxTX Idle state is '1'
 - 0 = IrDA encoded, UxTX Idle state is '0'
- bit 12 Unimplemented: Read as '0'
- bit 11 UTXBRK: UARTx Transmit Break bit
 - 1 = Sends Sync Break on next transmission Start bit, followed by twelve '0' bits, followed by Stop bit; cleared by hardware upon completion
 - 0 = Sync Break transmission is disabled or completed
- bit 10 UTXEN: UARTx Transmit Enable bit⁽¹⁾
 - 1 = Transmit is enabled, UxTX pin is controlled by UARTx
 0 = Transmit is disabled, any pending transmission is aborted and buffer is reset; UxTX pin is controlled
 - by the PORT
- bit 9 UTXBF: UARTx Transmit Buffer Full Status bit (read-only)
 - 1 = Transmit buffer is full
 - 0 = Transmit buffer is not full, at least one more character can be written
- bit 8 TRMT: Transmit Shift Register Empty bit (read-only)
 - 1 = Transmit Shift Register is empty and transmit buffer is empty (the last transmission has completed)
 - 0 = Transmit Shift Register is not empty, a transmission is in progress or queued
- bit 7-6 URXISEL<1:0>: UARTx Receive Interrupt Mode Selection bits
 - 11 = Interrupt is set on UxRSR transfer, making the receive buffer full (i.e., has 4 data characters)
 - 10 = Interrupt is set on UxRSR transfer, making the receive buffer 3/4 full (i.e., has 3 data characters)
 - 0x = Interrupt is set when any character is received and transferred from the UxRSR to the receive buffer; receive buffer has one or more characters
- **Note 1:** Refer to "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/ PIC24 Family Reference Manual" for information on enabling the UARTx module for transmit operation.



	D\$x<2:0>	Signal Source
	000	CLCINA
	001	System Clock
Δ	010	Timer1 Match
5:0	011	PWM1H
S1	ö 011 100	PWM5L
	101	High-Speed PWM Clock
	110	Timer2 Match
	111	Timer3 Match
	000	CLCINB
	001	CLC2 Out
Δ	010	CMP1 Out
5:0	011	UART1 TX Out
S2•	100	ADC End-of-Conversion
Δ	101	DMA Channel 0 Interrupt
	110	PWM1L
	111	PWM5H
	000	CLCINA
	001	CLC1 Out
A	010	CMP2 Out
\$5	011	SPI1 SDO Out
23	100	UART1 RX
Δ	101	PWM2H
	110	PWM6L
	111	OCMP2
	000	CLCINB
	001	CLC2 Out
	010	CMP3 Out
5:0	011	SDI1
S4<	100	PTG
Δ	101	ECAN1
	110	PWM2L
	111	PWM6H

TABLE 21-1: CLC1 MULTIPLEXER INPUT SOURCES

REGISTER 22-32: ADCMPxENL: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER LOW (x = 0 or 1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CMPEN	N<15:8>			
bit 15							bit 8
R/W/0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			CMPE	N<7:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **CMPEN<15:0>:** Comparator Enable for Corresponding Input Channels bits

0 = Conversion result for corresponding channel is not used by the comparator

REGISTER 22-33: ADCMPxENH: ADC DIGITAL COMPARATOR x CHANNEL ENABLE REGISTER HIGH (x = 0 or 1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—			CMPEN	<21:16>		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	d as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-6 Unimplemented: Read as '0'

bit 5-0

CMPEN<21:16>: Comparator Enable for Corresponding Input Channels bits

1 = Conversion result for corresponding channel is used by the comparator

0 = Conversion result for corresponding channel is not used by the comparator

^{1 =} Conversion result for corresponding channel is used by the comparator

REGISTER 23-2: CxCTRL2: CANx CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	_		—	—	—
bit 15							bit 8
U-0	U-0	U-0	R-0	R-0	R-0	R-0	R-0
	—	—			DNCNT<4:0>		
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplemented bit, read as '0'			
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown	
bit 15-5	Unimplemen	ted: Read as '	0'				
bit 4-0	DNCNT<4:0>	: DeviceNet™	Filter Bit Num	ber bits			
	10010-11111	1 = Invalid sele	ction				
	10001 = Com	npare up to Dat	a Byte 3, bit 6	ծ with EID<17>	•		
	•						
	•						
	•	noro un to Dot	o Duto 1 bit 7				
	00001 - Con	ot compare da	a byte 1, bit 7 ita hytes				
	- D01000 - D01	ior compare ua					

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0	
bit 15							bit 8	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0	
bit 7							bit 0	
Legend:								
R = Readable	bit	W = Writable bit		U = Unimplemented bit, read as '0'				
-n = Value at I	POR	'1' = Bit is set		'0' = Bit is cleared		x = Bit is unknown		
bit 15-14	F7MSK<1:0>	. Mask Source	for Filter 7 bi	ts				
	11 = Reserve	ed						
	10 = Accepta	ance Mask 2 reg	gisters contair	n mask				
	01 = Accepta 00 = Accepta	ince Mask Tre	gisters contair	n mask n mask				
bit 13-12	F6MSK<1:0>	. Mask Source	for Filter 6 bi	ts (same value	s as bits 15-14)			
bit 11-10	F5MSK<1:0>	. Mask Source	for Filter 5 bi	bits (same values as bits 15-14)				
bit 9-8	F4MSK<1:0>: Mask Source for Filter 4 bits (same values as bits 15-14)							
bit 7-6	F3MSK<1:0>	. Mask Source	for Filter 3 bi	ts (same value	s as bits 15-14)			
bit 5-4	F2MSK<1:0>	. Mask Source	for Filter 2 bi	ts (same value	s as bits 15-14)			
bit 3-2	F1MSK<1:0>	F1MSK<1:0>: Mask Source for Filter 1 bits (same values as bits 15-14)						

REGISTER 23-18: CxFMSKSEL1: CANx FILTERS 7-0 MASK SELECTION REGISTER 1

bit 1-0	FOMSK<1:0>: Mask Source for Filter 0 bits (same values as bits 15-14)

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{}	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m></n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator Write-Back Destination Address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) $\in \{015\}$
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x00000x1FFF}
lit1	1-bit unsigned literal $\in \{0,1\}$
lit4	4-bit unsigned literal ∈ {015}
lit5	5-bit unsigned literal $\in \{031\}$
lit8	8-bit unsigned literal \in {0255}
lit10	10-bit unsigned literal $\in \{0255\}$ for Byte mode, $\{0:1023\}$ for Word mode
lit14	14-bit unsigned literal $\in \{016384\}$
lit16	16-bit unsigned literal $\in \{065535\}$
lit23	23-bit unsigned literal \in {08388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512511}
Slit16	16-bit signed literal ∈ {-3276832767}
Slit6	6-bit signed literal \in {-1616}
Wb	Base W register ∈ {W0W15}
Wd	Destination W register \in { Wd, [Wd], [Wd++], [Wd], [++Wd], [Wd] }
Wdo	Destination W register ∈
	{ Wnd, [Wnd], [Wnd++], [Wnd], [++Wnd], [Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (Direct Addressing)

TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS



FIGURE 30-25: SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING CHARACTERISTICS^(1,2)

TABLE 30-52: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Op (unless othe Operating ter	erating Co erwise stat mperature	pnditions: 3.0V to 3.6V ed) ⁽⁵⁾ $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial $-40^{\circ}C \le TA \le +125^{\circ}C$ for Extended							
Param No.	Symbol	Characteristics	Min.	Typical	Max.	Units	Conditions					
Device Supply												
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	_	Lesser of: VDD + 0.3 or 3.6	V	Within 300 mV of VDD at all times, including device power-up					
AD02	AVss	Module Vss Supply	Vss	—	Vss + 0.3	V						
Reference Inputs												
AD06	Vrefl	Reference Voltage Low	_	AVss	—	V	(Note 1)					
AD07	Vref	Absolute Reference Voltage (VREFH – VREFL)	2.7	—	AVDD	V	(Note 3)					
AD08	IREF	Reference Input Current		5	10	μA	ADC operating or in standby					
Analog Input												
AD12	VINH-VINL	Full-Scale Input Span	AVss	—	AVdd	V						
AD14	Vin	Absolute Input Voltage	AVss – 0.3	—	AVDD + 0.3	V						
AD17	Rin	Recommended Impedance of Analog Voltage Source	—	100	_	Ω	For minimum sampling time (Note 1)					
AD66	Vbg	Internal Voltage Reference Source	_	1.2	—	V						
	-	ADC Ac	curacy: Pseu	udodiffere	ntial Input	-						
AD20a	Nr	Resolution		12		bits						
AD21a	INL	Integral Nonlinearity	> -3	—	< 3	LSb	AVss = 0V, AVDD = 3.3V					
AD22a	DNL	Differential Nonlinearity	> -1	—	< 1	LSb	AVss = 0V, AVDD = 3.3V (Note 2)					
AD23a	Gerr	Gain Error (Dedicated Core)	> 0	8	< 15	LSb	AVss = 0V, AVDD = 3.3V					
		Gain Error (Shared Core)	> 5	15	< 22	LSb						
AD24a	EOFF	Offset Error (Dedicated Core)	> 0	5	< 10	LSb	AVss = 0V, AVDD = 3.3V					
		Offset Error (Shared Core)	> 2	8	< 13	LSb						
AD25a	—	Monotonicity	_	—	—	_	Guaranteed					

Note 1: These parameters are not characterized or tested in manufacturing.

2: No missing codes, limits based on characterization results.

3: These parameters are characterized but not tested in manufacturing.

4: Characterized with a 15 kHz sine wave.

5: The ADC module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is ensured, but not characterized.

31.0 DC AND AC DEVICE CHARACTERISTICS GRAPHS

Note: The graphs provided following this note are a statistical summary based on a limited number of samples and are provided for design guidance purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.



28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	Limits	MIN	NOM	MAX	
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	X2			4.75	
Optional Center Pad Length	Y2			4.75	
Contact Pad Spacing	C1		6.00		
Contact Pad Spacing	C2		6.00		
Contact Pad Width (X28)	X1			0.35	
Contact Pad Length (X28)	Y1			0.80	
Corner Anchor (X4)	X3			1.00	
Corner Anchor (X4)	Y3			1.00	
Corner Anchor Chamfer (X4)	X4			0.35	
Corner Anchor Chamfer (X4)	Y4			0.35	
Contact Pad to Pad (X28)	G1	0.20			
Contact Pad to Center Pad (X28)	G2	0.20			
Thermal Via Diameter	V		0.33		
Thermal Via Pitch	EV		1.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2385B

Note: Corner anchor pads are not connected internally and are designed as mechanical features when the package is soldered to the PCB.