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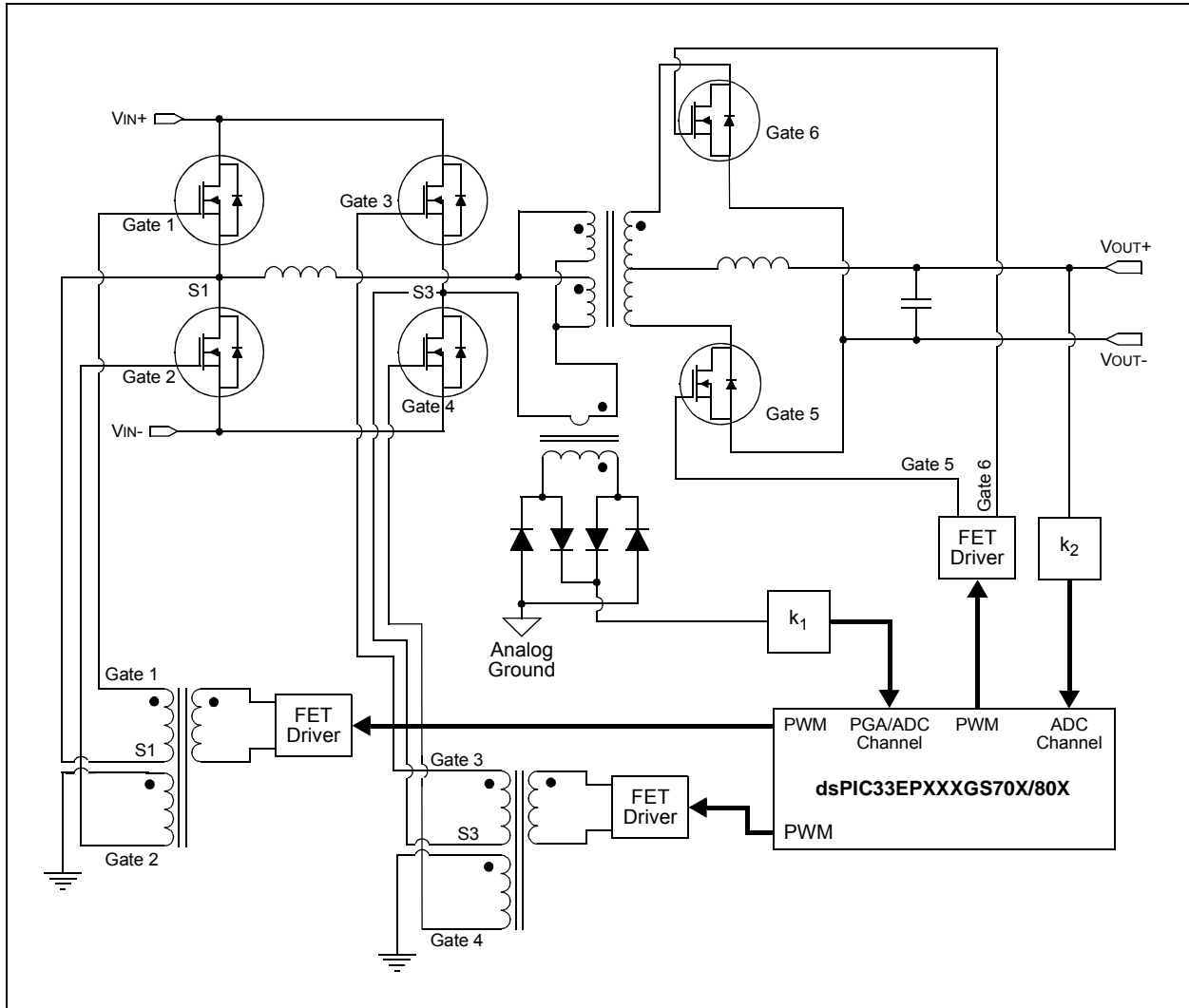
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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs804-e-pt

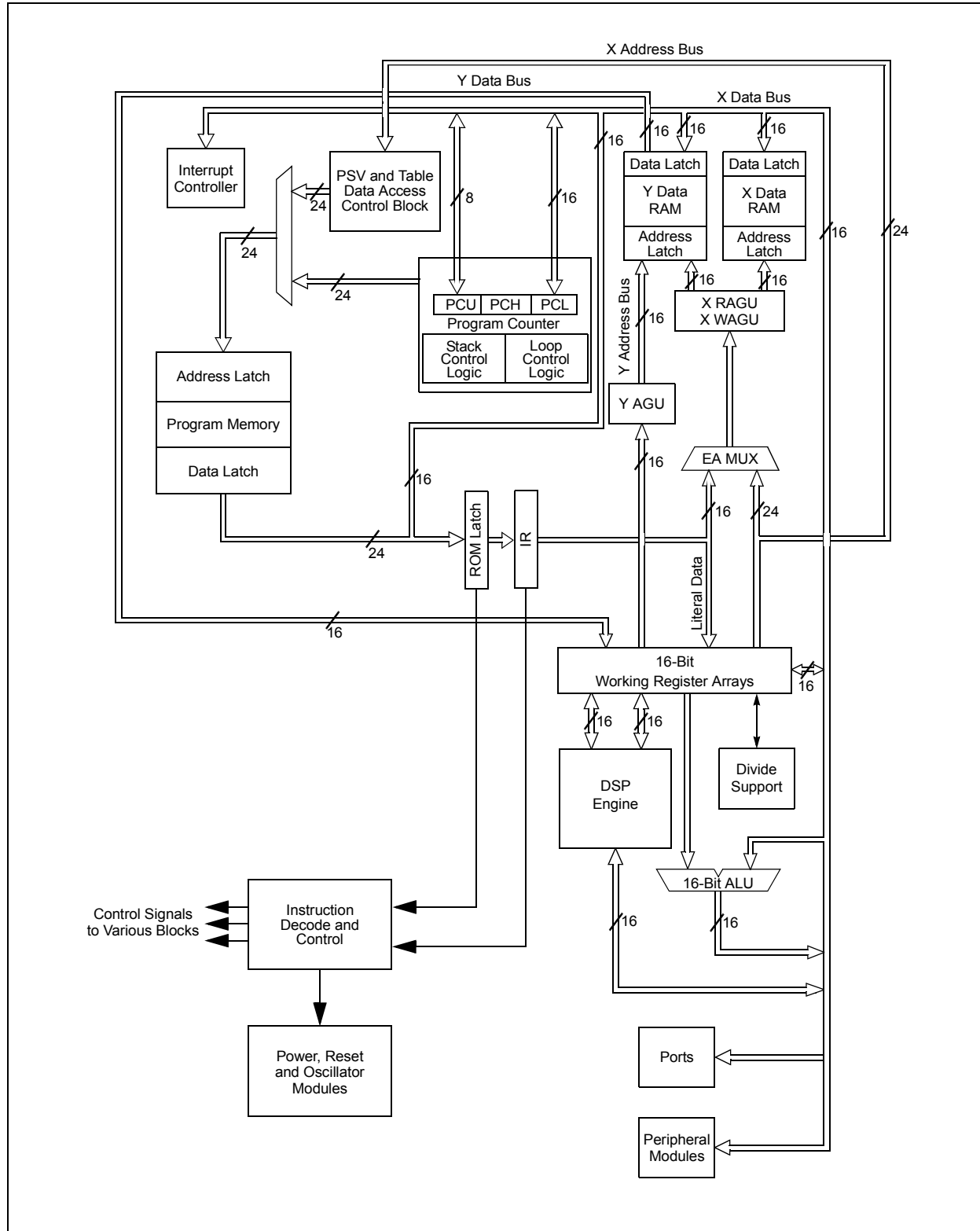
dsPIC33EPXXXGS70X/80X FAMILY

FIGURE 2-5: PHASE-SHIFTED FULL-BRIDGE CONVERTER



dsPIC33EPXXXGS70X/80X FAMILY

FIGURE 3-1: dsPIC33EPXXXGS70X/80X FAMILY CPU BLOCK DIAGRAM



dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5	IPL<2:0> : CPU Interrupt Priority Level Status bits ^(1,2) 111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled 110 = CPU Interrupt Priority Level is 6 (14) 101 = CPU Interrupt Priority Level is 5 (13) 100 = CPU Interrupt Priority Level is 4 (12) 011 = CPU Interrupt Priority Level is 3 (11) 010 = CPU Interrupt Priority Level is 2 (10) 001 = CPU Interrupt Priority Level is 1 (9) 000 = CPU Interrupt Priority Level is 0 (8)
bit 4	RA : REPEAT Loop Active bit 1 = REPEAT loop is in progress 0 = REPEAT loop is not in progress
bit 3	N : MCU ALU Negative bit 1 = Result was negative 0 = Result was non-negative (zero or positive)
bit 2	OV : MCU ALU Overflow bit This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred
bit 1	Z : MCU ALU Zero bit 1 = An operation that affects the Z bit has set it at some time in the past 0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)
bit 0	C : MCU ALU Carry/Borrow bit 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

- Note 1:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 2:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.
- 3:** A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

dsPIC33EPXXXGS70X/80X FAMILY

6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

6.1.1 KEY RESOURCES

- **“Reset”** (DS70602) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

dsPIC33EPXXXGS70X/80X FAMILY

FIGURE 7-1: dsPIC33EPXXXGS70X/80X FAMILY INTERRUPT VECTOR TABLE

The diagram illustrates the Interrupt Vector Table (IVT) for the dsPIC33EPXXXGS70X/80X family. A vertical arrow on the left indicates 'Decreasing Natural Order Priority' from top to bottom. The table lists various interrupt vectors and their corresponding addresses. A bracket on the right side of the table, labeled 'IVT', spans from the first 'Interrupt Vector 0' entry to the 'START OF CODE' entry. Two arrows point from the text 'See Table 7-1 for Interrupt Vector Details' to the first and last entries of the IVT range.

Reset – GOTO Instruction	0x000000
Reset – GOTO Address	0x000002
Oscillator Fail Trap Vector	0x000004
Address Error Trap Vector	0x000006
Generic Hard Trap Vector	0x000008
Stack Error Trap Vector	0x00000A
Math Error Trap Vector	0x00000C
Reserved	0x00000E
Generic Soft Trap Vector	0x000010
Reserved	0x000012
Interrupt Vector 0	0x000014
Interrupt Vector 1	0x000016
:	:
:	:
:	:
Interrupt Vector 52	0x00007C
Interrupt Vector 53	0x00007E
Interrupt Vector 54	0x000080
:	:
:	:
:	:
Interrupt Vector 116	0x0000FC
Interrupt Vector 117	0x0000FE
Interrupt Vector 118	0x000100
Interrupt Vector 119	0x000102
Interrupt Vector 120	0x000104
:	:
:	:
:	:
Interrupt Vector 244	0x0001FC
Interrupt Vector 245	0x0001FE
START OF CODE	0x000200

Note: In Dual Partition Flash modes, each partition has a dedicated Interrupt Vector Table.

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 9-7: LFSR: LINEAR FEEDBACK SHIFT REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	LFSR<14:8>						
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LFSR<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15

Unimplemented: Read as '0'

bit 14-0

LFSR<14:0>: Pseudorandom Data bits

11.6 Peripheral Pin Select (PPS)

A major challenge in general purpose devices is providing the largest possible set of peripheral features, while minimizing the conflict of features on I/O pins. The challenge is even greater on low pin count devices. In an application where more than one peripheral needs to be assigned to a single pin, inconvenient work arounds in application code, or a complete redesign, may be the only option.

Peripheral Pin Select configuration provides an alternative to these choices by enabling peripheral set selection and placement on a wide range of I/O pins. By increasing the pinout options available on a particular device, users can better tailor the device to their entire application, rather than trimming the application to fit the device.

The Peripheral Pin Select configuration feature operates over a fixed subset of digital I/O pins. Users may independently map the input and/or output of most digital peripherals to any one of these I/O pins. Hardware safeguards are included that prevent accidental or spurious changes to the peripheral mapping once it has been established.

11.6.1 AVAILABLE PINS

The number of available pins is dependent on the particular device and its pin count. Pins that support the Peripheral Pin Select feature include the label, “RPn”, in their full pin designation, where “n” is the remappable pin number. “RP” is used to designate pins that support both remappable input and output functions.

11.6.2 AVAILABLE PERIPHERALS

The peripherals managed by the Peripheral Pin Select are all digital only peripherals. These include general serial communications (UART and SPI), general purpose timer clock inputs, timer-related peripherals (input capture and output compare) and interrupt-on-change inputs.

In comparison, some digital only peripheral modules are never included in the Peripheral Pin Select feature. This is because the peripheral's function requires special I/O circuitry on a specific port and cannot be easily connected to multiple pins. One example includes I²C modules. A similar requirement excludes all modules with analog inputs, such as the ADC Converter.

A key difference between remappable and non-remappable peripherals is that remappable peripherals are not associated with a default I/O pin. The peripheral must always be assigned to a specific I/O pin before it can be used. In contrast, non-remappable peripherals are always available on a default pin, assuming that the peripheral is active and not conflicting with another peripheral.

When a remappable peripheral is active on a given I/O pin, it takes priority over all other digital I/Os and digital communication peripherals associated with the pin. Priority is given regardless of the type of peripheral that is mapped. Remappable peripherals never take priority over any analog functions associated with the pin.

11.6.3 CONTROLLING PERIPHERAL PIN SELECT

Peripheral Pin Select features are controlled through two sets of SFRs: one to map peripheral inputs and one to map outputs. Because they are separately controlled, a particular peripheral's input and output (if the peripheral has both) can be placed on any selectable function pin without constraint.

The association of a peripheral to a peripheral-selectable pin is handled in two different ways, depending on whether an input or output is being mapped.

dsPIC33EPXXXGS70X/80X FAMILY

11.7 I/O Helpful Tips

1. In some cases, certain pins, as defined in Table 30-11 under “Injection Current”, have internal protection diodes to VDD and VSS. The term, “Injection Current”, is also referred to as “Clamp Current”. On designated pins, with sufficient external current-limiting precautions by the user, I/O pin input voltages are allowed to be greater or less than the data sheet absolute maximum ratings, with respect to the VSS and VDD supplies. Note that when the user application forward biases either of the high or low-side internal input clamp diodes, that the resulting current being injected into the device, that is clamped internally by the VDD and VSS power rails, may affect the ADC accuracy by four to six counts.
2. I/O pins that are shared with any analog input pin (i.e., ANx) are always analog pins, by default, after any Reset. Consequently, configuring a pin as an analog input pin automatically disables the digital input pin buffer and any attempt to read the digital input level by reading PORTx or LATx will always return a ‘0’, regardless of the digital logic level on the pin. To use a pin as a digital I/O pin on a shared ANx pin, the user application needs to configure the Analog Pin Configuration registers (i.e., ANSELx) in the I/O ports module by setting the appropriate bit that corresponds to that I/O port pin to a ‘0’.

Note: Although it is not possible to use a digital input pin when its analog function is enabled, it is possible to use the digital I/O output function, TRISx = 0x0, while the analog function is also enabled. However, this is not recommended, particularly if the analog input is connected to an external analog voltage source, which would create signal contention between the analog signal and the output pin driver.

3. Most I/O pins have multiple functions. Referring to the device pin diagrams in this data sheet, the priorities of the functions allocated to any pins are indicated by reading the pin name from left-to-right. The left most function name takes precedence over any function to its right in the naming convention. For example: AN16/T2CK/T7CK/RC1; this indicates that AN16 is the highest priority in this example and will supersede all other functions to its right in the list. Those other functions to its right, even if enabled, would not work as long as any other function to its left was enabled. This rule applies to all of the functions listed for a given pin.
4. Each pin has an internal weak pull-up resistor and pull-down resistor that can be configured using the CNPux and CNPDx registers, respectively. These resistors eliminate the need for external resistors in certain applications. The internal pull-up is up to $\sim(VDD - 0.8)$, not VDD. This value is still above the minimum VIH of CMOS and TTL devices.
5. When driving LEDs directly, the I/O pin can source or sink more current than what is specified in the VOH/IOH and VOL/IOL DC characteristics specification. The respective IOH and IOL current rating only applies to maintaining the corresponding output at or above the VOH, and at or below the VOL levels. However, for LEDs, unlike digital inputs of an externally connected device, they are not governed by the same minimum VIH/VIL levels. An I/O pin output can safely sink or source any current less than that listed in the Absolute Maximum Ratings in **Section 30.0 “Electrical Characteristics”** of this data sheet. For example:

$$VOH = 2.4V @ IOH = -8 \text{ mA and } VDD = 3.3V$$

The maximum output current sourced by any 8 mA I/O pin = 12 mA.

LED source current < 12 mA is technically permitted. Refer to the VOH/IOH graphs in **Section 31.0 “DC and AC Device Characteristics Graphs”** for additional information.

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 11-31: RPINR45: PERIPHERAL PIN SELECT INPUT REGISTER 45

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINAR7	CLCINAR6	CLCINAR5	CLCINAR4	CLCINAR3	CLCINAR2	CLCINAR1	CLCINAR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **CLCINAR<7:0>**: Assign CLC Input A (CLCINA) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **Unimplemented**: Read as '0'

REGISTER 11-32: RPINR46: PERIPHERAL PIN SELECT INPUT REGISTER 46

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLCINBR7	CLCINBR6	CLCINBR5	CLCINBR4	CLCINBR3	CLCINBR2	CLCINBR1	CLCINBR0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented**: Read as '0'

bit 7-0 **CLCINBR<7:0>**: Assign CLC Input B (CLCINB) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 11-57: RPOR24: PERIPHERAL PIN SELECT OUTPUT REGISTER 24

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP177R6	RP177R5	RP177R4	RP177R3	RP177R2	RP177R1	RP177R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP176R6	RP176R5	RP176R4	RP176R3	RP176R2	RP176R1	RP176R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'
bit 14-8 **RP177R<6:0>:** Peripheral Output Function is Assigned to RP177 Output Pin bits
(see Table 11-13 for peripheral function numbers)
bit 7 **Unimplemented:** Read as '0'
bit 6-0 **RP176R<6:0>:** Peripheral Output Function is Assigned to RP176 Output Pin bits
(see Table 11-13 for peripheral function numbers)

REGISTER 11-58: RPOR25: PERIPHERAL PIN SELECT OUTPUT REGISTER 25

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP179R6	RP179R5	RP179R4	RP179R3	RP179R2	RP179R1	RP179R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP178R6	RP178R5	RP178R4	RP178R3	RP178R2	RP178R1	RP178R0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'
bit 14-8 **RP179R<6:0>:** Peripheral Output Function is Assigned to RP179 Output Pin bits
(see Table 11-13 for peripheral function numbers)
bit 7 **Unimplemented:** Read as '0'
bit 6-0 **RP178R<6:0>:** Peripheral Output Function is Assigned to RP178 Output Pin bits
(see Table 11-13 for peripheral function numbers)

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 16-12: PWMCONx: PWMx CONTROL REGISTER (x = 1 to 8) (CONTINUED)

bit 7-6	DTC<1:0> : Dead-Time Control bits 11 = Reserved 10 = Dead-time function is disabled 01 = Negative dead time is actively applied for Complementary Output mode 00 = Positive dead time is actively applied for all Output modes
bit 5-4	Unimplemented : Read as '0'
bit 3	MTBS : Master Time Base Select bit 1 = PWMx generator uses the secondary master time base for synchronization and the clock source for the PWMx generation logic (if secondary time base is available) 0 = PWMx generator uses the primary master time base for synchronization and the clock source for the PWMx generation logic
bit 2	CAM : Center-Aligned Mode Enable bit ^(2,3,4) 1 = Center-Aligned mode is enabled 0 = Edge-Aligned mode is enabled
bit 1	XPRES : External PWMx Reset Control bit ⁽⁵⁾ 1 = Current-limit source resets the time base for this PWMx generator if it is in Independent Time Base mode 0 = External pins do not affect the PWMx time base
bit 0	IUE : Immediate Update Enable bit 1 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are immediate 0 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are synchronized to the local PWMx time base

- Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
- 2:** The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- 3:** These bits should not be changed after the PWMx is enabled by setting PTEN (PTCON<15>) = 1.
- 4:** Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
- 5:** Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 16-16: SPHASE_x: PWM_x SECONDARY PHASE-SHIFT REGISTER (x = 1 to 8)^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASE _x <15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASE _x <7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **SPHASE_x<15:0>**: Secondary Phase Offset for PWM_xL Output Pin bits
(used in Independent PWM mode only)

Note 1: If PWMCON_x<9> = 0, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11), PHASE_x<15:0> = Phase-shift value for PWM_xL only

2: If PWMCON_x<9> = 1, the following applies based on the mode of operation:

- Complementary, Redundant and Push-Pull Output mode (IOCON_x<11:10> = 00, 01 or 10);
SPHASE_x<15:0> = Not used
- True Independent Output mode (IOCON_x<11:10> = 11); PHASE_x<15:0> = Independent time base period value for PWM_xL only
- When the PHASE_x/SPHASE_x registers provide the local period, the valid range of values is 0x0010-0xFFFF8

dsPIC33EPXXXGS70X/80X FAMILY

19.0 INTER-INTEGRATED CIRCUIT (I²C)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Inter-Integrated Circuit (I²C)**” (DS70000195) in the “*dsPIC33/PIC24 Family Reference Manual*”, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family of devices contains two Inter-Integrated Circuit (I²C) modules: I2C1 and I2C2.

The I²C module provides complete hardware support for both Slave and Multi-Master modes of the I²C serial communication standard, with a 16-bit interface.

The I²C module has a 2-pin interface:

- The SCLx/ASCLx pin is clock
- The SDAx/ASDAx pin is data

The I²C module offers the following key features:

- I²C Interface supporting both Master and Slave modes of Operation
- I²C Slave mode Supports 7 and 10-Bit Addressing
- I²C Master mode Supports 7 and 10-Bit Addressing
- I²C Port allows Bidirectional Transfers between Master and Slaves
- Serial Clock Synchronization for I²C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control)
- I²C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly
- System Management Bus (SMBus) Support
- Alternate I²C Pin Mapping (ASCLx/ASDAx)

19.1 I²C Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

19.1.1 KEY RESOURCES

- “**Inter-Integrated Circuit (I²C)**” (DS70000195) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

dsPIC33EPXXXGS70X/80X FAMILY

REGISTER 22-4: ADCON2H: ADC CONTROL REGISTER 2 HIGH

R-0, HSC	R-0, HSC	r-0	r-0	r-0	r-0	R/W-0	R/W-0
REFRDY	REFERR	—	—	—	—	SHRSAMC9	SHRSAMC8
bit 15						bit 8	

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SHRSAMC7	SHRSAMC6	SHRSAMC5	SHRSAMC4	SHRSAMC3	SHRSAMC2	SHRSAMC1	SHRSAMC0
bit 7						bit 0	

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

bit 15 **REFRDY:** Band Gap and Reference Voltage Ready Flag bit

1 = Band gap is ready
0 = Band gap is not ready

bit 14 **REFERR:** Band Gap or Reference Voltage Error Flag bit

1 = Band gap was removed after the ADC module was enabled (ADON = 1)
0 = No band gap error was detected

bit 13-10 **Reserved:** Maintain as '0'

bit 9-0 **SHRSAMC<9:0>:** Shared ADC Core Sample Time Selection bits

These bits specify the number of shared ADC Core Clock Periods (TADCORE) for the shared ADC core sample time.

1111111111 = 1025 TADCORE

•
•
•

0000000001 = 3 TADCORE

0000000000 = 2 TADCORE

dsPIC33EPXXXGS70X/80X FAMILY

24.3 Module Applications

This module provides a means for the SMPS dsPIC[®] DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 12-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWMx Signal (current limit)
- Truncate the PWMx Period (current minimum)
- Disable the PWMx Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) generate an interrupt, 2) have the ADC take a sample and convert it, and 3) truncate the PWMx output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

24.4 Digital-to-Analog Comparator (DAC)

Each analog comparator has a dedicated 12-bit DAC that is used to program the comparator threshold voltage via the CMPxDAC register. The DAC voltage reference source is selected using the EXTREF and RANGE bits in the CMPxCON register.

The EXTREF bit selects either the external voltage reference, EXTREFx, or an internal source as the voltage reference source. The EXTREFx input enables users to connect to a voltage reference that better suits their application. The RANGE bit enables AVDD as the voltage reference source for the DAC when an internal voltage reference is selected.

Note: EXTREF2 is not available on all devices.

Each DACx has an output enable bit, DACOE, in the CMPxCON register that enables the DACx reference voltage to be routed to an external output pin (DACOUTx). Refer to Figure 24-1 for connecting the DACx output voltage to the DACOUTx pins.

Note 1: Ensure that multiple DACOE bits are not set in software. The output on the DACOUTx pin will be indeterminate if multiple comparators enable the DACx output.

2: DACOUT2 is not available on all devices.

24.5 Pulse Stretcher and Digital Logic

The analog comparator can respond to very fast transient signals. After the comparator output is given the desired polarity, the signal is passed to a pulse stretching circuit. The pulse stretching circuit has an asynchronous set function and a delay circuit that ensures the minimum pulse width is three system clock cycles wide to allow the attached circuitry to properly respond to a narrow pulse event.

The pulse stretcher circuit is followed by a digital filter. The digital filter is enabled via the FLTREN bit in the CMPxCON register. The digital filter operates with the clock specified via the FCLKSEL bit in the CMPxCON register. The comparator signal must be stable in a high or low state, for at least three of the selected clock cycles, for it to pass through the digital filter.

dsPIC33EPXXXGS70X/80X FAMILY

25.0 PROGRAMMABLE GAIN AMPLIFIER (PGA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to “**Programmable Gain Amplifier (PGA)**” (DS70005146) in the “dsPIC33/PIC24 Family Reference Manual”, which is available from the Microchip web site (www.microchip.com).

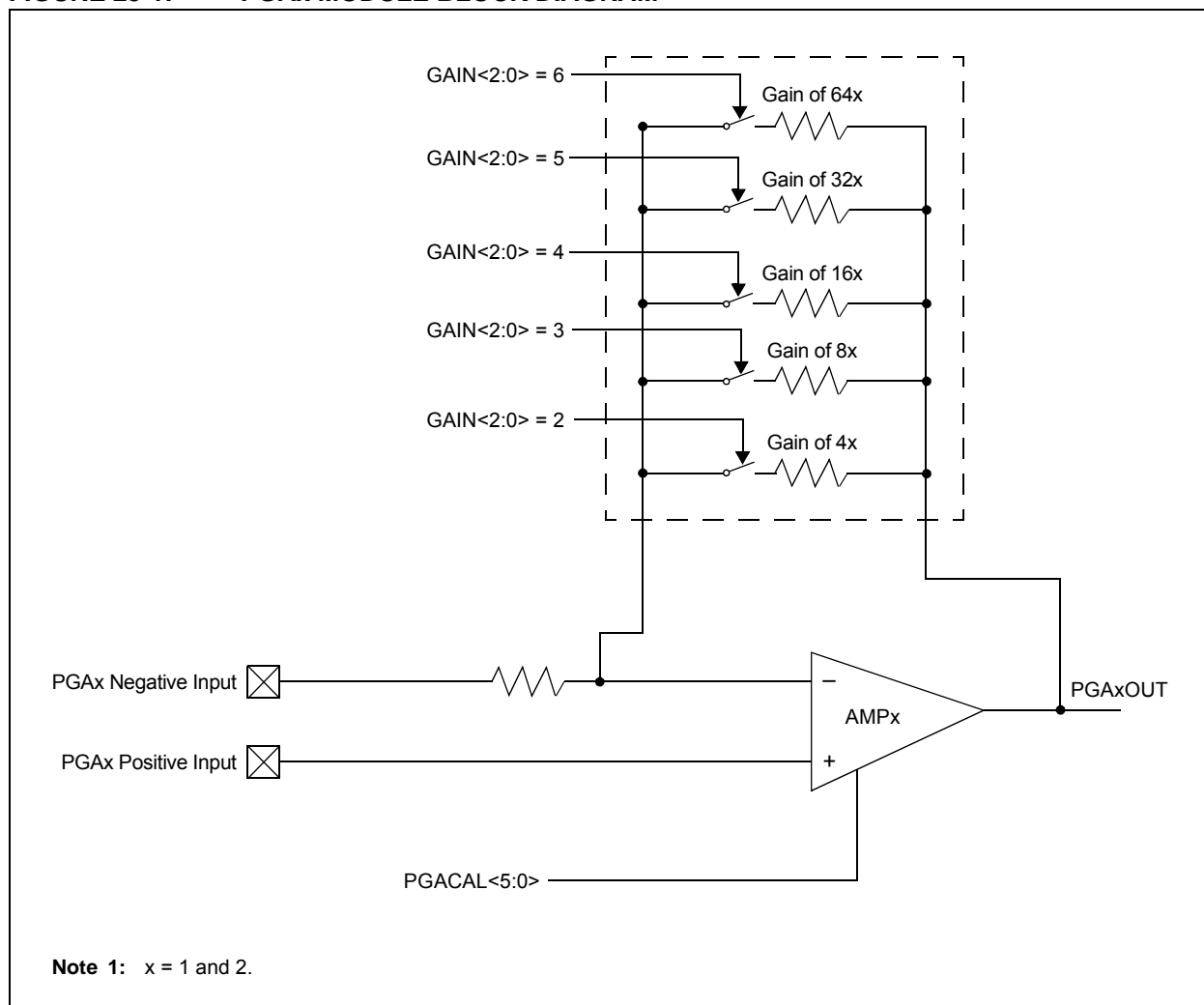
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family devices have two Programmable Gain Amplifiers (PGA1, PGA2). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x, 32x and 64x
- High Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

FIGURE 25-1: PGAx MODULE BLOCK DIAGRAM



dsPIC33EPXXXGS70X/80X FAMILY

FIGURE 30-27: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (MASTER MODE)

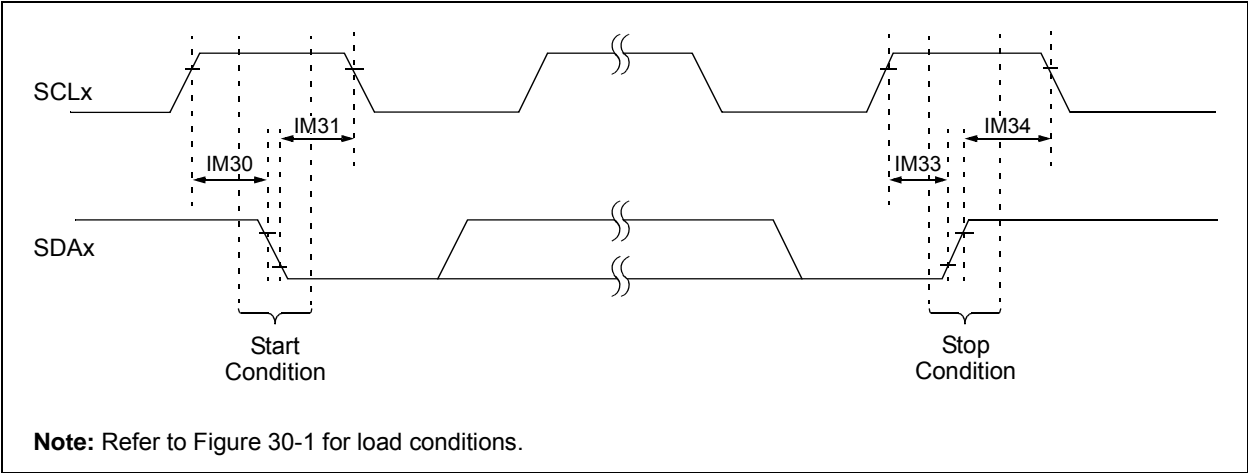
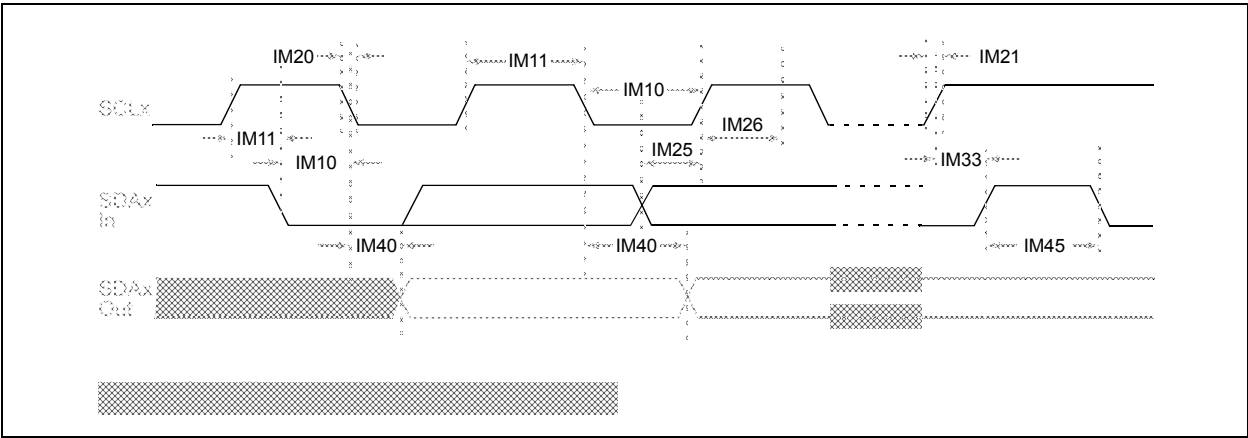


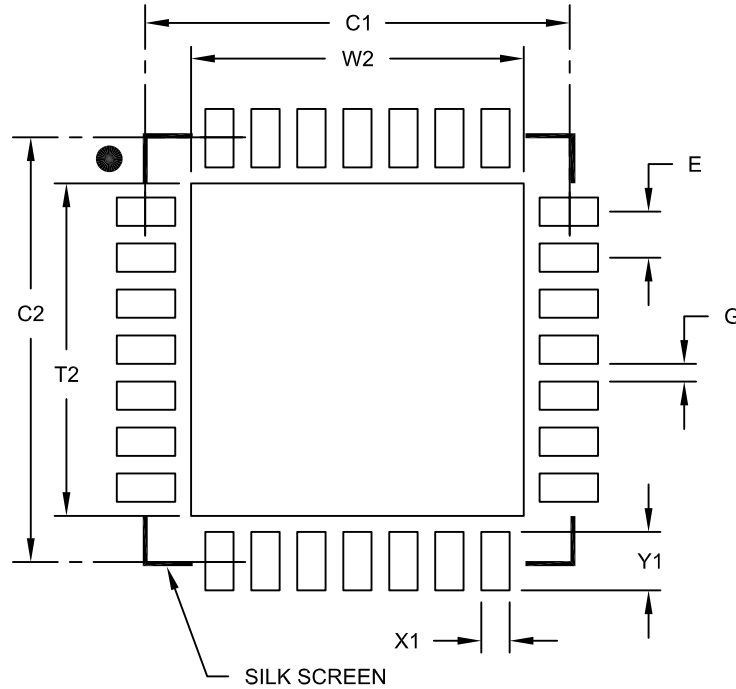
FIGURE 30-28: I2Cx BUS DATA TIMING CHARACTERISTICS (MASTER MODE)



dsPIC33EPXXXGS70X/80X FAMILY

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (Y28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

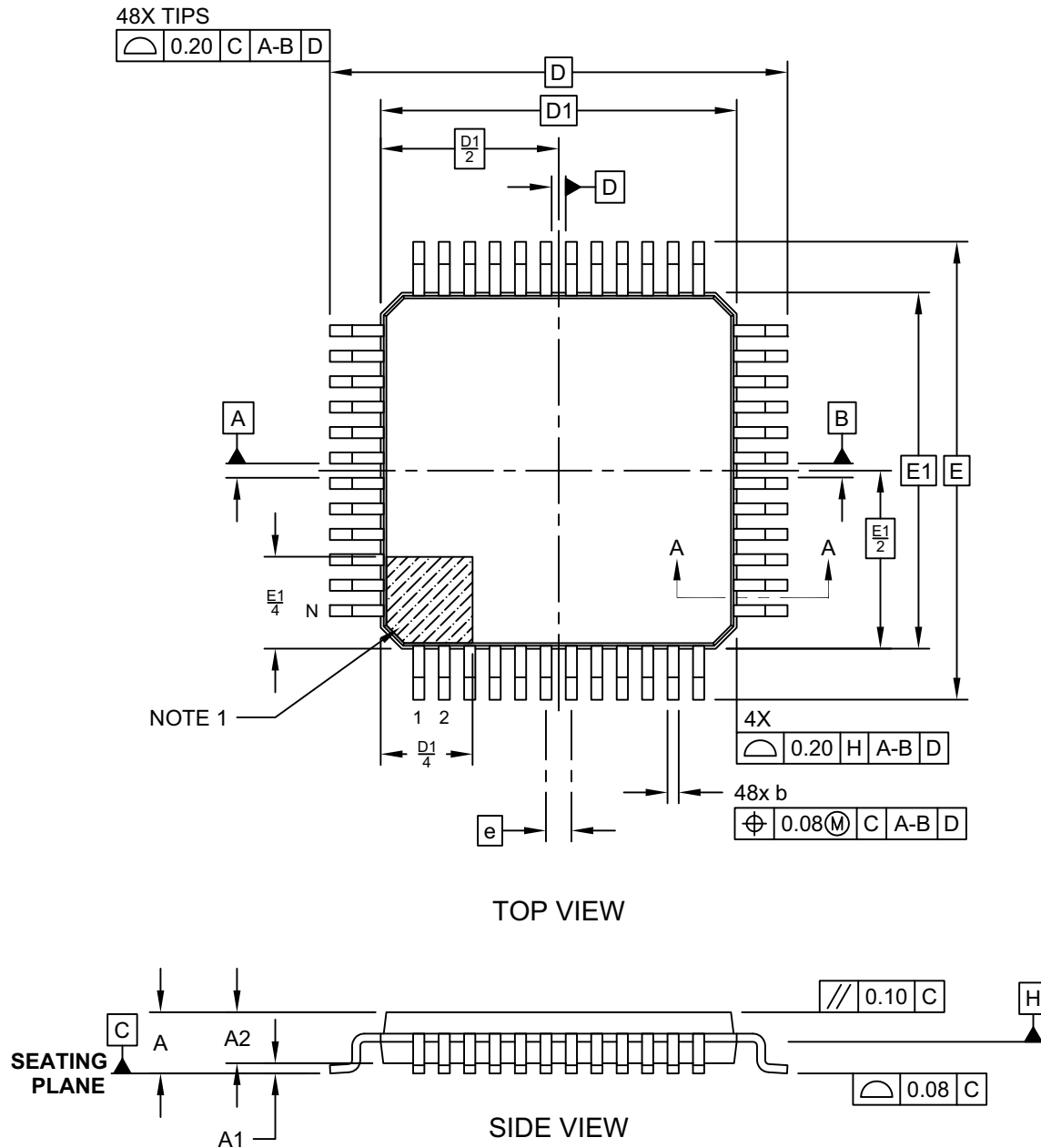
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A

dsPIC33EPXXXGS70X/80X FAMILY

48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-300-PT Rev A Sheet 1 of 2