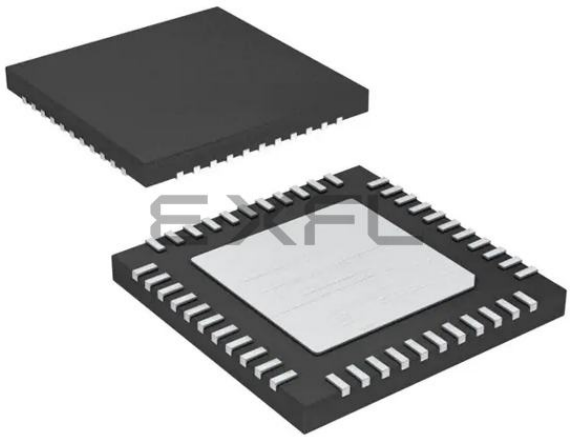
Microchip Technology - DSPIC33EP128GS804T-I/ML Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	33
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 17x12b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep128gs804t-i-ml

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, MPLAB ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site.

- *"Using MPLAB® ICD 3 In-Circuit Debugger"* (poster) (DS51765)
- *"Development Tools Design Advisory"* (DS51764)
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide" (*DS51616)
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) (DS51749)

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

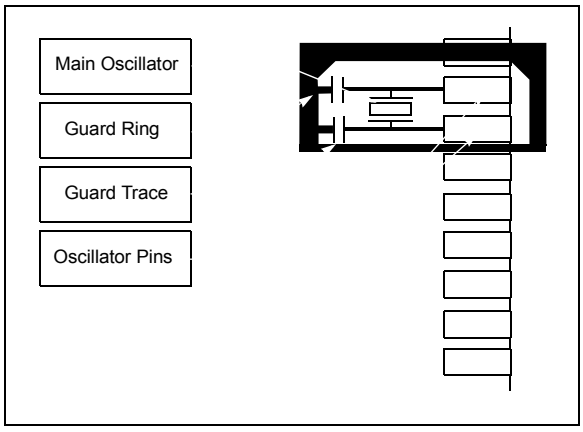


TABLE 4-4: SFR BLOCK 200h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
I2C1 and I2C2			U1STA	222	0000000010010000	SPI1BRGH	252	0000000000000000
I2C1CONL	200	0001000000000000	U1TXREG	224	0000000xxxxxxxxx	SPI1IMSKL	254	0000000000000000
I2C1CONH	202	0000000000000000	U1RXREG	226	0000000000000000	SPI1IMSKH	256	0000000000000000
I2C1STAT	204	0000000000000000	U1BRG	228	0000000000000000	SPI1URDTL	258	0000000000000000
I2C1ADD	206	0000000000000000	U2MODE	230	0000000000000000	SPI1URDTH	25A	0000000000000000
I2C1MSK	208	0000000000000000	U2STA	232	0000000010010000	SPI2CON1L	260	0000000000000000
I2C1BRG	20A	0000000000000000	U2TXREG	234	0000000xxxxxxxxx	SPI2CON1H	262	0000000000000000
I2C1TRN	20C	0000000011111111	U2RXREG	236	0000000000000000	SPI2CON2L	264	0000000000000000
I2C1RCV	20E	0000000000000000	U2BRG	238	0000000000000000	SPI2CON2H	266	0000000000000000
I2C2CON1	210	0001000000000000	**SPI**			SPI2STATL	268	0000000000101000
I2C2CON2	212	0000000000000000	SPI1CON1L	240	0000000000000000	SPI2STATH	26A	0000000000000000
I2C2STAT	214	0000000000000000	SPI1CON1H	242	0000000000000000	SPI2BUFL	26C	0000000000000000
I2C2ADD	216	0000000000000000	SPI1CON2L	244	0000000000000000	SPI2BUFH	26E	0000000000000000
I2C2MSK	218	0000000000000000	SPI1CON2H	246	0000000000000000	SPI3STAT	270	000xxxxxxxxxxxx
I2C2BRG	21A	0000000000000000	SPI1STATL	248	0000000000101000	SPI2BRGH	272	0000000000000000
I2C2TRN	21C	0000000011111111	SPI1STATH	24A	0000000000000000	SPI2IMSKL	274	0000000000000000
I2C2RCV	21E	0000000000000000	SPI1BUFL	24C	0000000000000000	SPI2IMSKH	276	0000000000000000
UART1 and UART2			SPI1BUFH	24E	0000000000000000	SPI2URDTL	278	0000000000000000
U1MODE	220	0000000000000000	SPI1BRGL	250	000xxxxxxxxxxxx	SPI2URDTH	27A	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-5: SFR BLOCK 300h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
ADC			ADCMP0ENH	33A	0000000000000000	ADTRIG4L	390	0000000000000000
ADCON1L	300	0000000000000000	ADCMP0LO	33C	0000000000000000	ADTRIG4H	392	0000000000000000
ADCON1H	302	0000000001100000	ADCMP0HI	33E	0000000000000000	ADCMP0CON	3A0	0000000000000000
ADCON2L	304	0000000000000000	ADCMP1ENL	340	0000000000000000	ADCMP1CON	3A4	0000000000000000
ADCON2H	306	0000000000000000	ADCMP1ENH	342	0000000000000000	ADBASE	3C0	0000000000000000
ADCON3L	308	0000000000000000	ADCMP1LO	344	0000000000000000	ADLVLTRGL	3D0	0000000000000000
ADCON3H	30A	0000000000000000	ADCMP1HI	346	0000000000000000	ADLVLTRGH	3D2	0000000000000000
ADCON4L	30C	0000000000000000	ADFL0DAT	368	0000000000000000	ADCORE0L	3D4	0000000000000000
ADCON4H	30E	0000000000000000	ADFL0CON	36A	0000000000000000	ADCORE0H	3D6	0000001100000000
ADMOD0L	310	0000000000000000	ADFL1DAT	36C	0000000000000000	ADCORE1L	3D8	0000000000000000
ADMOD0H	312	0000000000000000	ADFL1CON	36E	0000000000000000	ADCORE1H	3DA	0000001100000000
ADMOD1L	314	0000000000000000	ADTRIG0L	380	0000000000000000	ADCORE2L	3DC	0000000000000000
ADIEL	320	0000000000000000	ADTRIG0H	382	0000000000000000	ADCORE2H	3DE	0000001100000000
ADIEH	322	0000000000000000	ADTRIG1L	384	0000000000000000	ADCORE3L	3E0	0000000000000000
ADCSS1L	328	0000000000000000	ADTRIG1H	386	0000000000000000	ADCORE3H	3E2	0000001100000000
ADCSS1H	32A	0000000000000000	ADTRIG2L	388	0000000000000000	ADEIEL	3F0	0000000000000000
ADSTATL	330	0000000000000000	ADTRIG2H	38A	0000000000000000	ADEIEH	3F2	0000000000000000
ADSTATH	332	0000000000000000	ADTRIG3L	38C	0000000000000000	ADEISTATL	3F8	0000000000000000
ADCMP0ENL	338	0000000000000000	ADTRIG3H	38E	0000000000000000	ADEISTATH	3FA	0000000000000000

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Interrupts"** (DS70000600) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGS70X/80X family CPU.

The interrupt controller has the following features:

- Six Processor Exceptions and Software Traps
- Seven User-Selectable Priority Levels
- Interrupt Vector Table (IVT) with a Unique Vector for each Interrupt or Exception Source
- Fixed Priority within a Specified User Priority Level
- Fixed Interrupt Entry and Return Latencies
- Alternate Interrupt Vector Table (AIVT) for Debug Support

7.1 Interrupt Vector Table

The dsPIC33EPXXXGS70X/80X family Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location, 000004h. The IVT contains six non-maskable trap vectors and up to 246 sources of interrupts. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.1.1 ALTERNATE INTERRUPT VECTOR TABLE

The Alternate Interrupt Vector Table (AIVT), shown in Figure 7-2, is available only when the Boot Segment is defined and the AIVT has been enabled. To enable the Alternate Interrupt Vector Table, the Configuration bit, AIVTDIS in the FSEC register, must be programmed and the AIVTEN bit must be set (INTCON2<8> = 1). When the AIVT is enabled, all interrupt and exception processes use the alternate vectors instead of the default vectors. The AIVT begins at the start of the last page of the Boot Segment, defined by BSLIM<12:0>. The second half of the page is no longer usable space. The Boot Segment must be at least 2 pages to enable the AIVT.

Note: Although the Boot Segment must be enabled in order to enable the AIVT, application code does not need to be present inside of the Boot Segment. The AIVT (and IVT) will inherit the Boot Segment code protection.

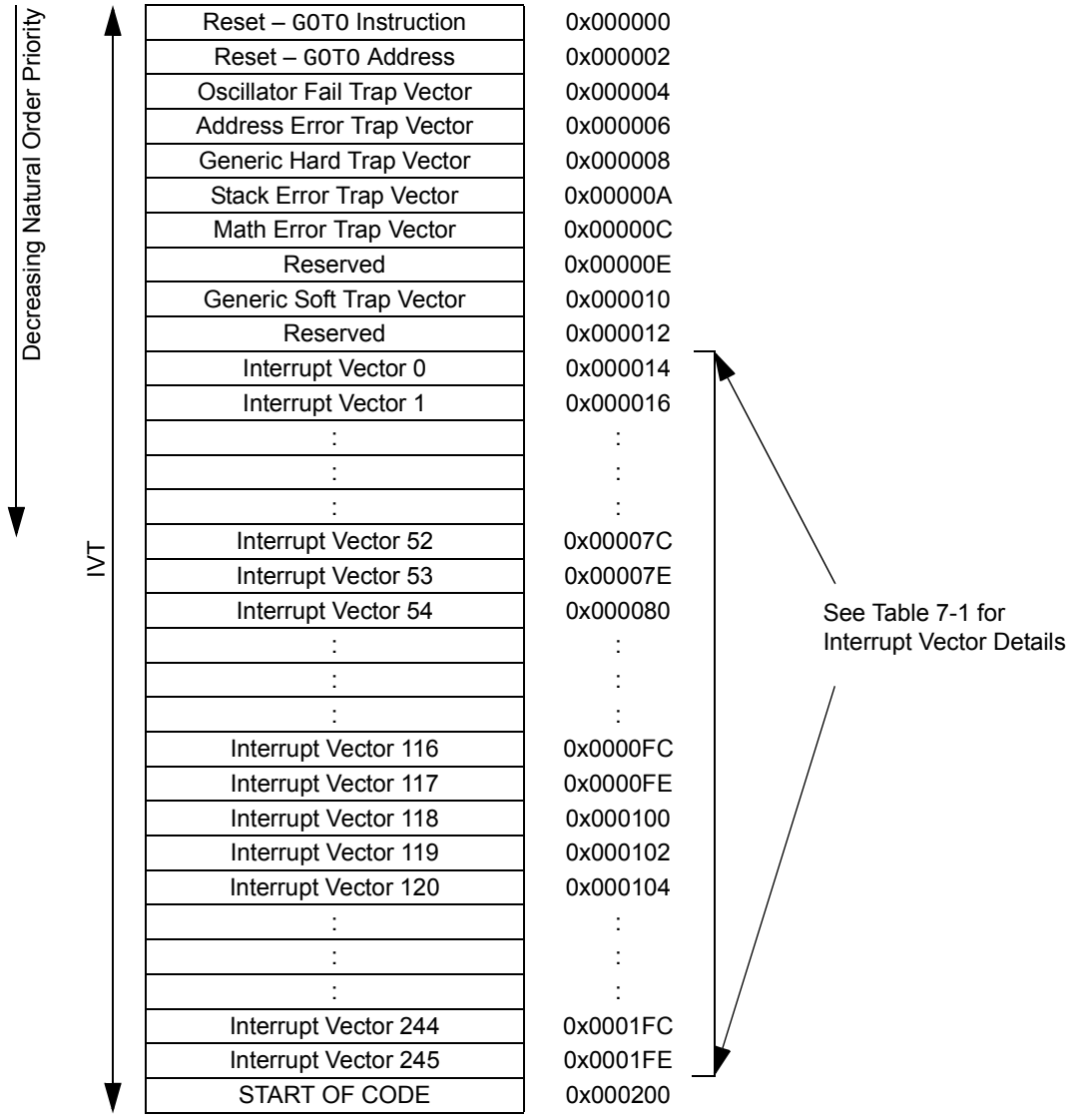
The AIVT supports debugging by providing a means to switch between an application and a support environment without requiring the interrupt vectors to be reprogrammed. This feature also enables switching between applications for evaluation of different software algorithms at run time.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGS70X/80X family devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

FIGURE 7-1: dsPIC33EPXXXGS70X/80X FAMILY INTERRUPT VECTOR TABLE



Note: In Dual Partition Flash modes, each partition has a dedicated Interrupt Vector Table.

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
AN17 Conversion Done	168	160	0x000154	IFS10<0> AN17IF	IEC10<0> AN17IE	IPC40<2:0> AN17IP<2:0>
AN18 Conversion Done	169	161	0x000156	IFS10<1> AN18IF	IEC10<1> AN18IE	IPC40<6:4> AN18IP<2:0>
AN19 Conversion Done	170	162	0x000158	IFS10<2> AN19IF	IEC10<2> AN19IE	IPC40<10:8> AN19IP<2:0>
AN20 Conversion Done	171	163	0x00015A	IFS10<3> AN20IF	IEC10<3> AN20IE	IPC40<14:12> AN20IP<2:0>
AN21 Conversion Done	172	164	0x00015C	IFS10<4> AN21IF	IEC10<4> AN21IE	IPC41<2:0> AN21IP<2:0>
Reserved	173-180	165-172	0x00015C-0x00016C	—	—	—
I2C1 – I2C1 Bus Collision	181	173	0x00016E	IFS10<13> I2C1IF	IEC10<13> I2C1IE	IPC43<6:4> I2C1IP<2:0>
I2C2 – I2C2 Bus Collision	182	174	0x000170	IFS10<14> I2C2IF	IEC10<14> I2C2IE	IPC43<10:8> I2C2IP<2:0>
Reserved	183-184	175-176	0x000172-0x000174	—	—	—
ADCMP0 – ADC Digital Comparator 0	185	177	0x000176	IFS11<1> ADCMP0IF	IEC11<1> ADCMP0IE	IPC44<6:4> ADCMP0IP<2:0>
ADCMP1 – ADC Digital Comparator 1	186	178	0x000178	IFS11<2> ADCMP1IF	IEC11<2> ADCMP1IE	IPC44<10:8> ADCMP1IP<2:0>
ADFLTR0 – ADC Filter 0	187	179	0x00017A	IFS11<3> ADFLTR0IF	IEC11<3> ADFLTR0IE	IPC44<14:12> ADFLTR0IP<2:0>
ADFLTR1 – ADC Filter 1	188	180	0x00017C	IFS11<4> ADFLTR1IF	IEC11<4> ADFLTR1IE	IPC45<2:0> ADFLTR1IP<2:0>
Reserved	189-253	181-245	0x00017E-0x000192	—	—	—

8.1 DMA Controller Registers

Each DMA Controller Channel x (where x = 0 through 3) contains the following registers:

- 16-Bit DMA Channel x Control Register (DMAxCON)
- 16-Bit DMA Channel x IRQ Select Register (DMAxREQ)
- 32-Bit DMA Channel x Start Address Register A (DMAxSTAL/H)
- 32-Bit DMA Channel x Start Address Register B (DMAxSTBL/H)
- 16-Bit DMA Channel x Peripheral Address Register (DMAxPAD)
- 14-Bit DMA Channel x Transfer Count Register (DMAxCNT)

Additional status registers (DMAPWC, DMARQC, DMAPPS, DMALCA and DSADRL/H) are common to all DMA Controller channels. These status registers provide information on write and request collisions, as well as on last address and channel access information.

The interrupt flags (DMAxIF) are located in an IFSx register in the interrupt controller. The corresponding interrupt enable control bits (DMAxIE) are located in an IECx register in the interrupt controller and the corresponding interrupt priority control bits (DMAxIP) are located in an IPCx register in the interrupt controller.

REGISTER 8-1: DMAxCON: DMA CHANNEL x CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CHEN	SIZE	DIR	HALF	NULLW	—	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0
—	—	AMODE1	AMODE0	—	—	MODE1	MODE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **CHEN:** DMA Channel Enable bit
1 = Channel is enabled
0 = Channel is disabled

bit 14 **SIZE:** DMA Data Transfer Size bit
1 = Byte
0 = Word

bit 13 **DIR:** Transfer Direction bit (source/destination bus select)
1 = Reads from RAM address, writes to peripheral address
0 = Reads from peripheral address, writes to RAM address

bit 12 **HALF:** Block Transfer Interrupt Select bit
1 = Initiates interrupt when half of the data has been moved
0 = Initiates interrupt when all of the data has been moved

bit 11 **NULLW:** Null Data Peripheral Write Mode Select bit
1 = Null data write to peripheral in addition to RAM write (DIR bit must also be clear)
0 = Normal operation

bit 10-6 **Unimplemented:** Read as ‘0’

bit 5-4 **AMODE<1:0>:** DMA Channel Addressing Mode Select bits
11 = Reserved
10 = Peripheral Indirect mode
01 = Register Indirect without Post-Increment mode
00 = Register Indirect with Post-Increment mode

bit 3-2 **Unimplemented:** Read as ‘0’

bit 1-0 **MODE<1:0>:** DMA Channel Operating Mode Select bits
11 = One-Shot, Ping-Pong modes are enabled (one block transfer from/to each DMA buffer)
10 = Continuous, Ping-Pong modes are enabled
01 = One-Shot, Ping-Pong modes are disabled
00 = Continuous, Ping-Pong modes are disabled

REGISTER 8-14: DMAPPS: DMA PING-PONG STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	PPST3	PPST2	PPST1	PPST0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **PPST3:** Channel 3 Ping-Pong Mode Status Flag bit
1 = DMA3STB register is selected
0 = DMA3STA register is selected

bit 2 **PPST2:** Channel 2 Ping-Pong Mode Status Flag bit
1 = DMA2STB register is selected
0 = DMA2STA register is selected

bit 1 **PPST1:** Channel 1 Ping-Pong Mode Status Flag bit
1 = DMA1STB register is selected
0 = DMA1STA register is selected

bit 0 **PPST0:** Channel 0 Ping-Pong Mode Status Flag bit
1 = DMA0STB register is selected
0 = DMA0STA register is selected

REGISTER 9-6: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3(1)	RODIV2(1)	RODIV1(1)	RODIV0(1)
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROON:** Reference Oscillator Output Enable bit
1 = Reference oscillator output is enabled on the RPn pin(2)
0 = Reference oscillator output is disabled

bit 14 **Unimplemented:** Read as '0'

bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
1 = Reference oscillator output continues to run in Sleep
0 = Reference oscillator output is disabled in Sleep

bit 12 **ROSEL:** Reference Oscillator Source Select bit
1 = Oscillator crystal is used as the reference clock
0 = System clock is used as the reference clock

bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits(1)
1111 = Reference clock divided by 32,768
1110 = Reference clock divided by 16,384
1101 = Reference clock divided by 8,192
1100 = Reference clock divided by 4,096
1011 = Reference clock divided by 2,048
1010 = Reference clock divided by 1,024
1001 = Reference clock divided by 512
1000 = Reference clock divided by 256
0111 = Reference clock divided by 128
0110 = Reference clock divided by 64
0101 = Reference clock divided by 32
0100 = Reference clock divided by 16
0011 = Reference clock divided by 8
0010 = Reference clock divided by 4
0001 = Reference clock divided by 2
0000 = Reference clock

bit 7-0 **Unimplemented:** Read as '0'

Note 1: The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
2: This pin is remappable. See **Section 11.6 "Peripheral Pin Select (PPS)"** for more information.

TABLE 11-8: PORTC REGISTER MAP(1)

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISC	TRISC<15:12>				—	TRISC<10:0>										
PORTC	RC<15:12>				—	RC<10:0>										
LATC	LATC<15:12>				—	LATC<10:0>										
ODCC	ODCC<15:12>				—	ODCC<10:0>										
CNENC	CNIEC<15:12>				—	CNIEC<10:0>										
CNPUC	CNPUC<15:12>				—	CNPUC<10:0>										
CNPDC	CNPDC<15:12>				—	CNPDC<10:0>										
ANSELC	—	—	—	ANSC12	—	ANSC<10:9>		—	—	ANSC<6:4>			—	ANSC<2:1>		—

Legend: — = unimplemented, read as '0'.

Note 1: Refer to Table 11-3 for bit availability on each pin count variant.

TABLE 11-9: PORTD REGISTER MAP(1)

File Name	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TRISD	TRISD<15:0>															
PORTD	RD<15:0>															
LATD	LATD<15:0>															
ODCD	ODCD<15:0>															
CNEND	CNIED<15:0>															
CNPUD	CNPUD<15:0>															
CNPDD	CNPDD<15:0>															
ANSELD	—	—	ANSD13	—	—	—	—	ANSD<8:7>		—	ANSD5	—	—	ANSD2	—	—

Legend: — = unimplemented, read as '0'.

Note 1: Refer to Table 11-4 for bit availability on each pin count variant.

REGISTER 11-3: LATx: PORTx DATA LATCH REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LATx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LATx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **LATx<15:0>:** PORTx Data Latch bits
1 = The latch content is '1'
0 = The latch content is '0'

Note 1: See Table 11-1, Table 11-2, Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-4: ODCx: PORTx OPEN-DRAIN CONTROL REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ODCx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **PORTx<15:0>:** PORTx Open-Drain Control bits
1 = The pin acts as an open-drain output pin if TRISx is '0'
0 = The pin acts as a normal pin

Note 1: See Table 11-1, Table 11-2, Table 11-3, Table 11-4 and Table 11-5 for individual bit availability in this register.

REGISTER 11-11: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1CKR7	T1CKR6	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **T1CKR<7:0>:** Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 11-12: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T3CKR7	T3CKR6	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2CKR7	T2CKR6	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **T3CKR<7:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **T2CKR<7:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)

bit 3-0 **SEVTPS<3:0>:** PWMx Special Event Trigger Output Postscaler Select bits(1)
1111 = 1:16 postscaler generates a Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 postscaler generates a Special Event Trigger on every second compare match event
0000 = 1:1 postscaler generates a Special Event Trigger on every compare match event

Note 1: These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

REGISTER 16-2: PTCON2: PWMx CLOCK DIVIDER SELECT REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)
111 = Reserved
110 = Divide-by-64, maximum PWM timing resolution
101 = Divide-by-32, maximum PWM timing resolution
100 = Divide-by-16, maximum PWM timing resolution
011 = Divide-by-8, maximum PWM timing resolution
010 = Divide-by-4, maximum PWM timing resolution
001 = Divide-by-2, maximum PWM timing resolution
000 = Divide-by-1, maximum PWM timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-26: AUXCONx: PWMx AUXILIARY CONTROL REGISTER (x = 1 to 8)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
HRPDIS	HRDDIS	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **HRPDIS:** High-Resolution PWMx Period Disable bit
1 = High-resolution PWMx period is disabled to reduce power consumption
0 = High-resolution PWMx period is enabled

bit 14 **HRDDIS:** High-Resolution PWMx Duty Cycle Disable bit
1 = High-resolution PWMx duty cycle is disabled to reduce power consumption
0 = High-resolution PWMx duty cycle is enabled

bit 13-12 **Unimplemented:** Read as ‘0’

bit 11-8 **BLANKSEL<3:0>:** PWMx State Blank Source Select bits
The selected state blank signal will block the current-limit and/or Fault input signals (if enabled via the BCH and BCL bits in the LEBCONx register).
1001 = Reserved
1000 = PWM8H is selected as the state blank source
0111 = PWM7H is selected as the state blank source
0110 = PWM6H is selected as the state blank source
0101 = PWM5H is selected as the state blank source
0100 = PWM4H is selected as the state blank source
0011 = PWM3H is selected as the state blank source
0010 = PWM2H is selected as the state blank source
0001 = PWM1H is selected as the state blank source
0000 = No state blanking

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-2 **CHOPSEL<3:0>:** PWMx Chop Clock Source Select bits
The selected signal will enable and disable (chop) the selected PWMx outputs.
1001 = Reserved
1000 = PWM8H is selected as the chop clock source
0111 = PWM7H is selected as the chop clock source
0110 = PWM6H is selected as the chop clock source
0101 = PWM5H is selected as the chop clock source
0100 = PWM4H is selected as the chop clock source
0011 = PWM3H is selected as the chop clock source
0010 = PWM2H is selected as the chop clock source
0001 = PWM1H is selected as the chop clock source
0000 = Chop clock generator is selected as the chop clock source

bit 1 **CHOPHEN:** PWMxH Output Chopping Enable bit
1 = PWMxH chopping function is enabled
0 = PWMxH chopping function is disabled

bit 0 **CHOPLEN:** PWMxL Output Chopping Enable bit
1 = PWMxL chopping function is enabled
0 = PWMxL chopping function is disabled

TABLE 17-1: PTG STEP COMMAND FORMAT (CONTINUED)

bit 3-0	Step Command	OPTION<3:0>	Option Description
	PTGCTRL(1)	0000	Reserved
		0001	Reserved
		0010	Disable PTG Step Delay Timer (PTGSD)
		0011	Reserved
		0100	Reserved
		0101	Reserved
		0110	Enable PTG Step Delay Timer (PTGSD)
		0111	Reserved
		1000	Start and wait for the PTG Timer0 to match the PTG Timer0 Limit register
		1001	Start and wait for the PTG Timer1 to match the PTG Timer1 Limit register
		1010	Reserved
		1011	Wait for software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1)
		1100	Copy contents of the PTG Counter 0 register to the CNVCHSEL<5:0> bits (ADCON3L<5:0>)
		1101	Copy contents of the PTG Counter 1 register to the CNVCHSEL<5:0> bits (ADCON3L<5:0>)
		1110	Copy contents of the PTG Literal 0 register to the CNVCHSEL<5:0> bits (ADCON3L<5:0>)
		1111	Generate the triggers indicated in the PTG Broadcast Trigger Enable register (PTGBTE)
	PTGADD(1)	0000	Add contents of PTGADJ register to the PTG Counter 0 Limit register (PTGC0LIM)
		0001	Add contents of PTGADJ register to the PTG Counter 1 Limit register (PTGC1LIM)
		0010	Add contents of PTGADJ register to the PTG Timer0 Limit register (PTGT0LIM)
		0011	Add contents of PTGADJ register to the PTG Timer1 Limit register (PTGT1LIM)
		0100	Add contents of PTGADJ register to the PTG Step Delay Limit register (PTGSDLIM)
		0101	Add contents of PTGADJ register to the PTG Literal 0 register (PTGL0)
		0110	Reserved
		0111	Reserved
	PTGCOPY(1)	1000	Copy contents of PTGHOLD register to the PTG Counter 0 Limit register (PTGC0LIM)
		1001	Copy contents of PTGHOLD register to the PTG Counter 1 Limit register (PTGC1LIM)
		1010	Copy contents of PTGHOLD register to the PTG Timer0 Limit register (PTGT0LIM)
		1011	Copy contents of PTGHOLD register to the PTG Timer1 Limit register (PTGT1LIM)
		1100	Copy contents of PTGHOLD register to the PTG Step Delay Limit register (PTGSDLIM)
		1101	Copy contents of PTGHOLD register to the PTG Literal 0 register (PTGL0)
		1110	Reserved
		1111	Reserved

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 17-2 for the trigger output descriptions.

REGISTER 19-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and ACK is generated for a received address/data byte, ignoring the state of the I2COV only if the RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled
If the rising edge of SCLx and SDAx is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte, the SCLREL (I2CxCONL<12>) bit will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte, the slave hardware clears the SCLREL (I2CxCONL<12>) bit and SCLx is held low
0 = Data holding is disabled

REGISTER 21-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G2D4T	G2D4N	G2D3T	G2D3N	G2D2T	G2D2N	G2D1T	G2D1N
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
G1D4T	G1D4N	G1D3T	G1D3N	G1D2T	G1D2N	G1D1T	G1D1N
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **G2D4T:** Gate 2 Data Source 4 True Enable bit
1 = Data Source 4 non-inverted signal is enabled for Gate 2
0 = Data Source 4 non-inverted signal is disabled for Gate 2

bit 14 **G2D4N:** Gate 2 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 2
0 = Data Source 4 inverted signal is disabled for Gate 2

bit 13 **G2D3T:** Gate 2 Data Source 3 True Enable bit
1 = Data Source 3 non-inverted signal is enabled for Gate 2
0 = Data Source 3 non-inverted signal is disabled for Gate 2

bit 12 **G2D3N:** Gate 2 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 2
0 = Data Source 3 inverted signal is disabled for Gate 2

bit 11 **G2D2T:** Gate 2 Data Source 2 True Enable bit
1 = Data Source 2 non-inverted signal is enabled for Gate 2
0 = Data Source 2 non-inverted signal is disabled for Gate 2

bit 10 **G2D2N:** Gate 2 Data Source 2 Negated Enable bit
1 = Data Source 2 inverted signal is enabled for Gate 2
0 = Data Source 2 inverted signal is disabled for Gate 2

bit 9 **G2D1T:** Gate 2 Data Source 1 True Enable bit
1 = Data Source 1 non-inverted signal is enabled for Gate 2
0 = Data Source 1 non-inverted signal is disabled for Gate 2

bit 8 **G2D1N:** Gate 2 Data Source 1 Negated Enable bit
1 = Data Source 1 inverted signal is enabled for Gate 2
0 = Data Source 1 inverted signal is disabled for Gate 2

bit 7 **G1D4T:** Gate 1 Data Source 4 True Enable bit
1 = Data Source 4 non-inverted signal is enabled for Gate 1
0 = Data Source 4 non-inverted signal is disabled for Gate 1

bit 6 **G1D4N:** Gate 1 Data Source 4 Negated Enable bit
1 = Data Source 4 inverted signal is enabled for Gate 1
0 = Data Source 4 inverted signal is disabled for Gate 1

bit 5 **G1D3T:** Gate 1 Data Source 3 True Enable bit
1 = Data Source 3 non-inverted signal is enabled for Gate 1
0 = Data Source 3 non-inverted signal is disabled for Gate 1

bit 4 **G1D3N:** Gate 1 Data Source 3 Negated Enable bit
1 = Data Source 3 inverted signal is enabled for Gate 1
0 = Data Source 3 inverted signal is disabled for Gate 1

REGISTER 22-8: ADCON4H: ADC CONTROL REGISTER 4 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C3CHS1	C3CHS0	C2CHS1	C2CHS0	C1CHS1	C1CHS0	C0CHS1	C0CHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-6 **C3CHS<1:0>:** Dedicated ADC Core 3 Input Channel Selection bits
1x = Reserved
01 = AN15 (differential negative input when DIFF3 (ADMOD0L<7>) = 1)
00 = AN3

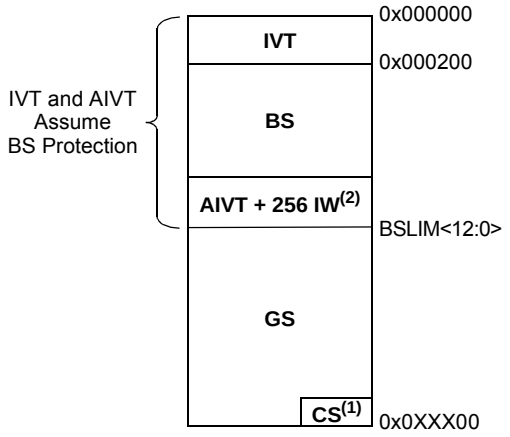
bit 5-4 **C2CHS<1:0>:** Dedicated ADC Core 2 Input Channel Selection bits
11 = Reserved
10 = VREF band gap
01 = AN11 (differential negative input when DIFF2 (ADMOD0L<5>) = 1)
00 = AN2

bit 3-2 **C1CHS<1:0>:** Dedicated ADC Core 1 Input Channel Selection bits
11 = AN1ALT
10 = PGA2
01 = AN18 (differential negative input when DIFF1 (ADMOD0L<3>) = 1)
00 = AN1

bit 1-0 **C0CHS<1:0>:** Dedicated ADC Core 0 Input Channel Selection bits
11 = AN0ALT
10 = PGA1
01 = AN7 (differential negative input when DIFF0 (ADMOD0L<1>) = 1)
00 = AN0

The different device security segments are shown in Figure 27-3. Here, all three segments are shown but are not required. If only basic code protection is required, then GS can be enabled independently or combined with CS, if desired.

FIGURE 27-3: SECURITY SEGMENTS EXAMPLE FOR dsPIC33EPXXXGS70X/80X DEVICES



Note 1: If CS is write-protected, the last page (GS + CS) of program memory will be protected from an erase condition.

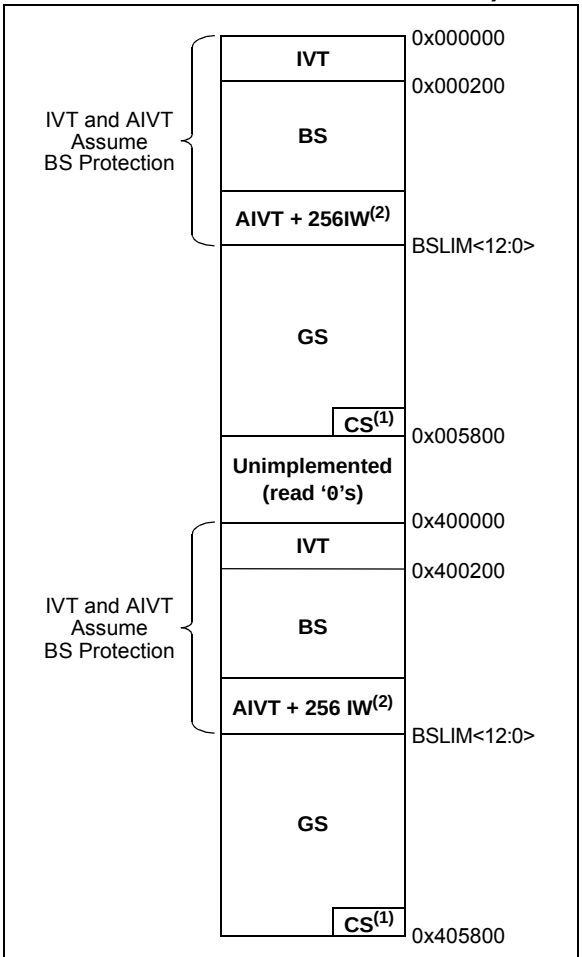
2: The last half (256 IW) of the last page of BS is unusable program memory.

dsPIC33EPXXXGS70X/80X family devices can be operated in Dual Partition mode, where security is required for each partition. When operating in Dual Partition mode, the Active and Inactive Partitions both contain unique copies of the Reset vector, Interrupt Vector Tables (IVT and AIVT, if enabled) and the Flash Configuration Words. Both partitions have the three security segments described previously. Code may not be executed from the Inactive Partition, but it may be programmed by, and read from, the Active Partition, subject to defined code protection. Figure 27-4 and Figure 27-5 show the different security segments for devices operating in Dual Partition mode.

The device may also operate in a Protected Dual Partition mode or in Privileged Dual Partition mode. In Protected Dual Partition mode, Partition 1 is permanently erase/write-protected. This implementation allows for a “Factory Default” mode, which provides a fail-safe backup image to be stored in Partition 1. For example, a fail-safe bootloader can be placed in Partition 1, along with a fail-safe backup code image, which can be used or rewritten into Partition 2 in the event of a failed Flash update to Partition 2.

Privileged Dual Partition mode performs the same function as Protected Dual Partition mode, except additional constraints are applied in an effort to prevent code in the Boot Segment and General Segment from being used against each other.

FIGURE 27-4: SECURITY SEGMENTS EXAMPLE FOR dsPIC33EP64GS70X/80X DEVICES (DUAL PARTITION MODES)



Note 1: If CS is write-protected, the last page (GS + CS) of program memory will be protected from an erase condition.

2: The last half (256 IW) of the last page of BS is unusable program memory.

TABLE 30-23: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SY00	TPU	Power-up Period	—	400	600	μs	
SY10	TOST	Oscillator Start-up Time	—	1024 TOSC	—	—	TOSC = OSC1 period
SY12	TWDT	Watchdog Timer Time-out Period	0.81	—	1.22	ms	WDTPRE = 0, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-21) at +85°C
			3.25	—	4.88	ms	WDTPRE = 1, WDTPOST<3:0> = 0000, using LPRC tolerances indicated in F21 (see Table 30-21) at +85°C
SY13	TIOZ	I/O High-Impedance from $\overline{\text{MCLR}}$ Low or Watchdog Timer Reset	0.68	0.72	1.2	μs	
SY20	TMCLR	$\overline{\text{MCLR}}$ Pulse Width (low)	2	—	—	μs	
SY30	TBOR	BOR Pulse Width (low)	1	—	—	μs	
SY35	TFSCM	Fail-Safe Clock Monitor Delay	—	500	900	μs	-40°C to +85°C
SY36	TVREG	Voltage Regulator Standby-to-Active mode Transition Time	—	—	30	μs	
SY37	TOSCDFRC	FRC Oscillator Start-up Delay	—	48	—	μs	
SY38	TOSCDLPRC	LPRC Oscillator Start-up Delay	—	—	70	μs	

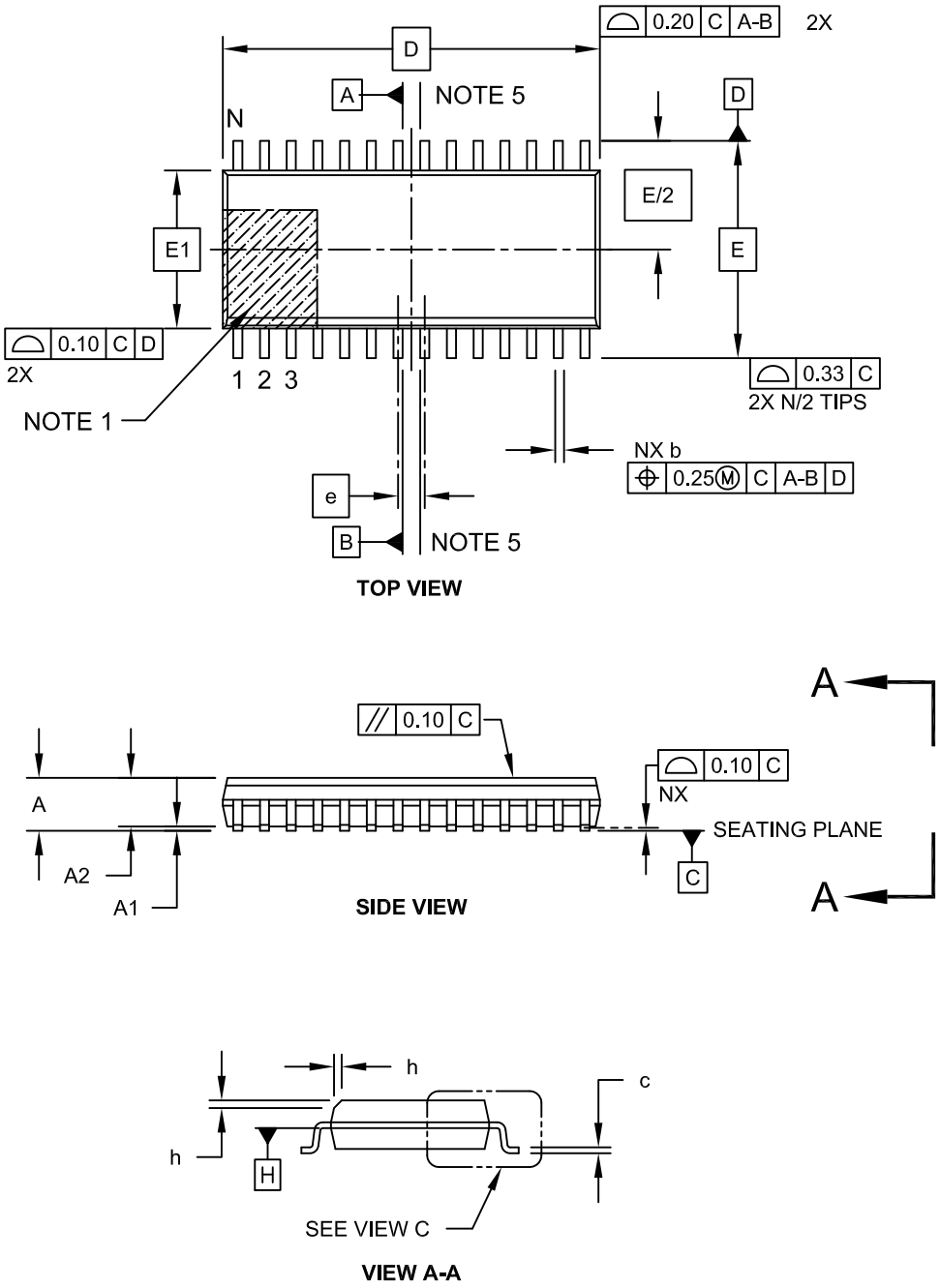
Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ." column is at 3.3V, +25°C unless otherwise stated.

32.2 Package Details

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-052C Sheet 1 of 2