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Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs708-i-pt

4.6 Instruction Addressing Modes

The addressing modes shown in Table 4-17 form the basis of the addressing modes optimized to support the specific features of individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.6.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.6.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

```
Operand 3 = Operand 1 <function> Operand 2
```

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can either be a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

TABLE 4-17: FUNDAMENTAL ADDRESSING MODES SUPPORTED

Addressing Mode	Description
File Register Direct	The address of the file register is specified explicitly.
Register Direct	The contents of a register are accessed directly.
Register Indirect	The contents of Wn form the Effective Address (EA).
Register Indirect Post-Modified	The contents of Wn form the EA. Wn is post-modified (incremented or decremented) by a constant value.
Register Indirect Pre-Modified	Wn is pre-modified (incremented or decremented) by a signed constant value to form the EA.
Register Indirect with Register Offset (Register Indexed)	The sum of Wn and Wb forms the EA.
Register Indirect with Literal Offset	The sum of Wn and a literal forms the EA.

REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits
Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMADRU<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

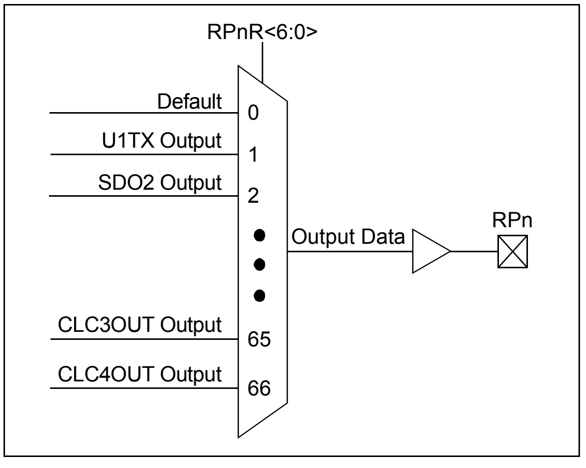
bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits
Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

11.6.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-33 through Register 11-56). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-13 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUTS FOR RPn



11.6.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings, across any or all of the RPn pins, is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs, and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

REGISTER 11-11: RPINR2: PERIPHERAL PIN SELECT INPUT REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T1CKR7	T1CKR6	T1CKR5	T1CKR4	T1CKR3	T1CKR2	T1CKR1	T1CKR0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **T1CKR<7:0>:** Assign Timer1 External Clock (T1CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 11-12: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T3CKR7	T3CKR6	T3CKR5	T3CKR4	T3CKR3	T3CKR2	T3CKR1	T3CKR0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T2CKR7	T2CKR6	T2CKR5	T2CKR4	T2CKR3	T2CKR2	T2CKR1	T2CKR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **T3CKR<7:0>:** Assign Timer3 External Clock (T3CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **T2CKR<7:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

REGISTER 16-12: PWMCONx: PWMx CONTROL REGISTER (x = 1 to 8) (CONTINUED)

bit 7-6 **DTC<1:0>:** Dead-Time Control bits
11 = Reserved
10 = Dead-time function is disabled
01 = Negative dead time is actively applied for Complementary Output mode
00 = Positive dead time is actively applied for all Output modes

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **MTBS:** Master Time Base Select bit
1 = PWMx generator uses the secondary master time base for synchronization and the clock source for the PWMx generation logic (if secondary time base is available)
0 = PWMx generator uses the primary master time base for synchronization and the clock source for the PWMx generation logic

bit 2 **CAM:** Center-Aligned Mode Enable bit(2,3,4)
1 = Center-Aligned mode is enabled
0 = Edge-Aligned mode is enabled

bit 1 **XPRES:** External PWMx Reset Control bit(5)
1 = Current-limit source resets the time base for this PWMx generator if it is in Independent Time Base mode
0 = External pins do not affect the PWMx time base

bit 0 **IUE:** Immediate Update Enable bit
1 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are immediate
0 = Updates to the active Duty Cycle, Phase Offset, Dead-Time and local Time Base Period registers are synchronized to the local PWMx time base

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
3: These bits should not be changed after the PWMx is enabled by setting PTEN (PTCON<15>) = 1.
4: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.
5: Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

REGISTER 16-15: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER (x = 1 to 8)(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** PWMx Phase-Shift Value or Independent Time Base Period for the PWMx Generator bits

Note 1: If PWMCONx<9> = `0`, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = `00`, `01` or `10`); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
- True Independent Output mode (IOCONx<11:10> = `11`); PHASEx<15:0> = Phase-shift value for PWMxH only
- When the PHASEx/SPHASEx registers provide the phase shift with respect to the master time base; therefore, the valid range is 0x0000 through period

2: If PWMCONx<9> = `1`, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = `00`, `01` or `10`); PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL
- True Independent Output mode (IOCONx<11:10> = `11`); PHASEx<15:0> = Independent time base period value for PWMxH only
- When the PHASEx/SPHASEx registers provide the local period, the valid range is 0x0000-0xFFF8

REGISTER 16-20: IOCONx: PWMx I/O CONTROL REGISTER (x = 1 to 8) (CONTINUED)

bit 3-2 **CLDAT<1:0>:** State for PWMxH and PWMxL Pins if CLMOD is Enabled bits(2)

IFLTMOD (FCLCONx<15>) = 0: Normal Fault mode:
If current limit is active, then CLDAT1 provides the state for the PWMxH pin.
If current limit is active, then CLDAT0 provides the state for the PWMxL pin.

IFLTMOD (FCLCONx<15>) = 1: Independent Fault mode:
CLDAT<1:0> bits are ignored.

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit

1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit

1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWMx time base
0 = Output overrides via the OVRDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: State represents the active/inactive state of the PWMx depending on the POLH and POLL bits settings.

REGISTER 16-21: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER (x = 1 to 8)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
TRGCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **TRGCMP<12:0>:** Trigger Compare Value bits

When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

bit 2-0 **Unimplemented:** Read as ‘0’

REGISTER 16-22: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (x = 1 to 8) (CONTINUED)

bit 7-3 **FLTSRC<4:0>:** Fault Control Signal Source Select for PWMx Generator bits
11111 = Reserved
10001 = Reserved
10000 = Analog Comparator 4
01111 = Analog Comparator 3
01110 = Analog Comparator 2
01101 = Analog Comparator 1
01100 = Fault 12
01011 = Fault 11
01010 = Fault 10
01001 = Fault 9
01000 = Fault 8
00111 = Fault 7
00110 = Fault 6
00101 = Fault 5
00100 = Fault 4
00011 = Fault 3
00010 = Fault 2
00001 = Fault 1
00000 = Reserved

bit 2 **FLTPOL:** Fault Polarity for PWMx Generator bit(1)
1 = The selected Fault source is active-low
0 = The selected Fault source is active-high

bit 1-0 **FLTMOD<1:0>:** Fault Mode for PWMx Generator bits
11 = Fault input is disabled
10 = Reserved
01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (cycle)
00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (latched condition)

Note 1: These bits should be changed only when PTEN = 0 (PTCON<15>).

REGISTER 16-23: STRIGx: PWMx SECONDARY TRIGGER COMPARE VALUE REGISTER (x = 1 to 8)(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STRGCMP<12:5>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
STRGCMP<4:0>					—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **STRGCMP<12:0>:** Secondary Trigger Compare Value bits
When the secondary PWMx functions in the local time base, this register contains the compare values that can trigger the ADC module.

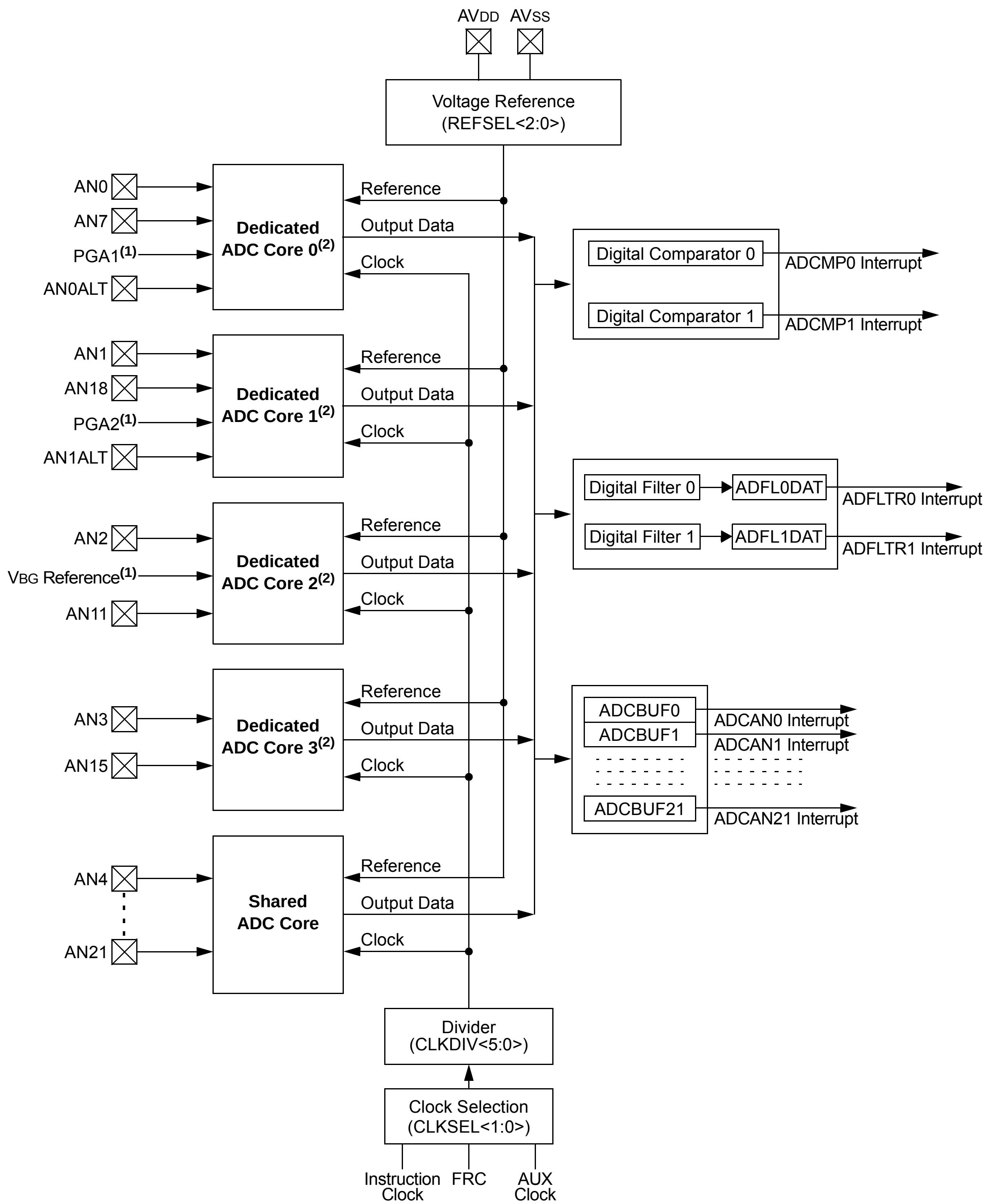
bit 2-0 **Unimplemented:** Read as ‘0’

Note 1: STRIGx cannot generate the PWM trigger interrupts.

REGISTER 21-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3	**G1D2T:** Gate 1 Data Source 2 True Enable bit 1 = Data Source 2 non-inverted signal is enabled for Gate 1 0 = Data Source 2 non-inverted signal is disabled for Gate 1
bit 2	**G1D2N:** Gate 1 Data Source 2 Negated Enable bit 1 = Data Source 2 inverted signal is enabled for Gate 1 0 = Data Source 2 inverted signal is disabled for Gate 1
bit 1	**G1D1T:** Gate 1 Data Source 1 True Enable bit 1 = Data Source 1 non-inverted signal is enabled for Gate 1 0 = Data Source 1 non-inverted signal is disabled for Gate 1
bit 0	**G1D1N:** Gate 1 Data Source 1 Negated Enable bit 1 = Data Source 1 inverted signal is enabled for Gate 1 0 = Data Source 1 inverted signal is disabled for Gate 1

FIGURE 22-1: ADC MODULE BLOCK DIAGRAM



Note 1: PGA1, PGA2 and the Band Gap Reference (VBG) are internal analog inputs and are not available on device pins.

2: If the dedicated core uses an alternate channel, then shared core function cannot be used.

REGISTER 22-6: ADCON3H: ADC CONTROL REGISTER 3 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CLKSEL1	CLKSEL0	CLKDIV5	CLKDIV4	CLKDIV3	CLKDIV2	CLKDIV1	CLKDIV0
bit 15							bit 8

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
SHREN	—	—	—	C3EN	C2EN	C1EN	C0EN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **CLKSEL<1:0>:** ADC Module Clock Source Selection bits
11 = APLL
10 = FRC
01 = FOSC (System Clock x 2)
00 = FSYS (System Clock)

bit 13-8 **CLKDIV<5:0>:** ADC Module Clock Source Divider bits
The divider forms a TCORESRC clock used by all ADC cores (shared and dedicated) from the TSRC ADC module clock source selected by the CLKSEL<1:0> bits. Then, each ADC core individually divides the TCORESRC clock to get a core-specific TADCORE clock using the ADCS<6:0> bits in the ADCORExH register or the SHRADCS<6:0> bits in the ADCON2L register.
111111 = 64 Source Clock Periods
•
•
•
000011 = 4 Source Clock Periods
000010 = 3 Source Clock Periods
000001 = 2 Source Clock Periods
000000 = 1 Source Clock Period

bit 7 **SHREN:** Shared ADC Core Enable bit
1 = Shared ADC core is enabled
0 = Shared ADC core is disabled

bit 6-4 **Unimplemented:** Read as ‘0’

bit 3 **C3EN:** Dedicated ADC Core 3 Enable bits
1 = Dedicated ADC Core 3 is enabled
0 = Dedicated ADC Core 3 is disabled

bit 2 **C2EN:** Dedicated ADC Core 2 Enable bits
1 = Dedicated ADC Core 2 is enabled
0 = Dedicated ADC Core 2 is disabled

bit 1 **C1EN:** Dedicated ADC Core 1 Enable bits
1 = Dedicated ADC Core 1 is enabled
0 = Dedicated ADC Core 1 is disabled

bit 0 **C0EN:** Dedicated ADC Core 0 Enable bits
1 = Dedicated ADC Core 0 is enabled
0 = Dedicated ADC Core 0 is disabled

REGISTER 22-19: ADMOD0L: ADC INPUT MODE CONTROL REGISTER 0 LOW

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF7	SIGN7	DIFF6	SIGN6	DIFF5	SIGN5	DIFF4	SIGN4
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF3	SIGN3	DIFF2	SIGN2	DIFF1	SIGN1	DIFF0	SIGN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1(odd) **DIFF<7:0>:** Differential-Mode for Corresponding Analog Inputs bits
1 = Channel is differential
0 = Channel is single-ended

bit 14-0 (even) **SIGN<7:0>:** Output Data Sign for Corresponding Analog Inputs bits
1 = Channel output data is signed
0 = Channel output data is unsigned

REGISTER 22-20: ADMOD0H: ADC INPUT MODE CONTROL REGISTER 0 HIGH

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF15	SIGN15	DIFF14	SIGN14	DIFF13	SIGN13	DIFF12	SIGN12
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIFF11	SIGN11	DIFF10	SIGN10	DIFF9	SIGN9	DIFF8	SIGN8
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-1(odd) **DIFF<15:8>:** Differential-Mode for Corresponding Analog Inputs bits
1 = Channel is differential
0 = Channel is single-ended

bit 14-0 (even) **SIGN<15:8>:** Output Data Sign for Corresponding Analog Inputs bits
1 = Channel output data is signed
0 = Channel output data is unsigned

25.0 PROGRAMMABLE GAIN AMPLIFIER (PGA)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to **"Programmable Gain Amplifier (PGA)"** (DS70005146) in the *"dsPIC33/PIC24 Family Reference Manual"*, which is available from the Microchip web site (www.microchip.com).

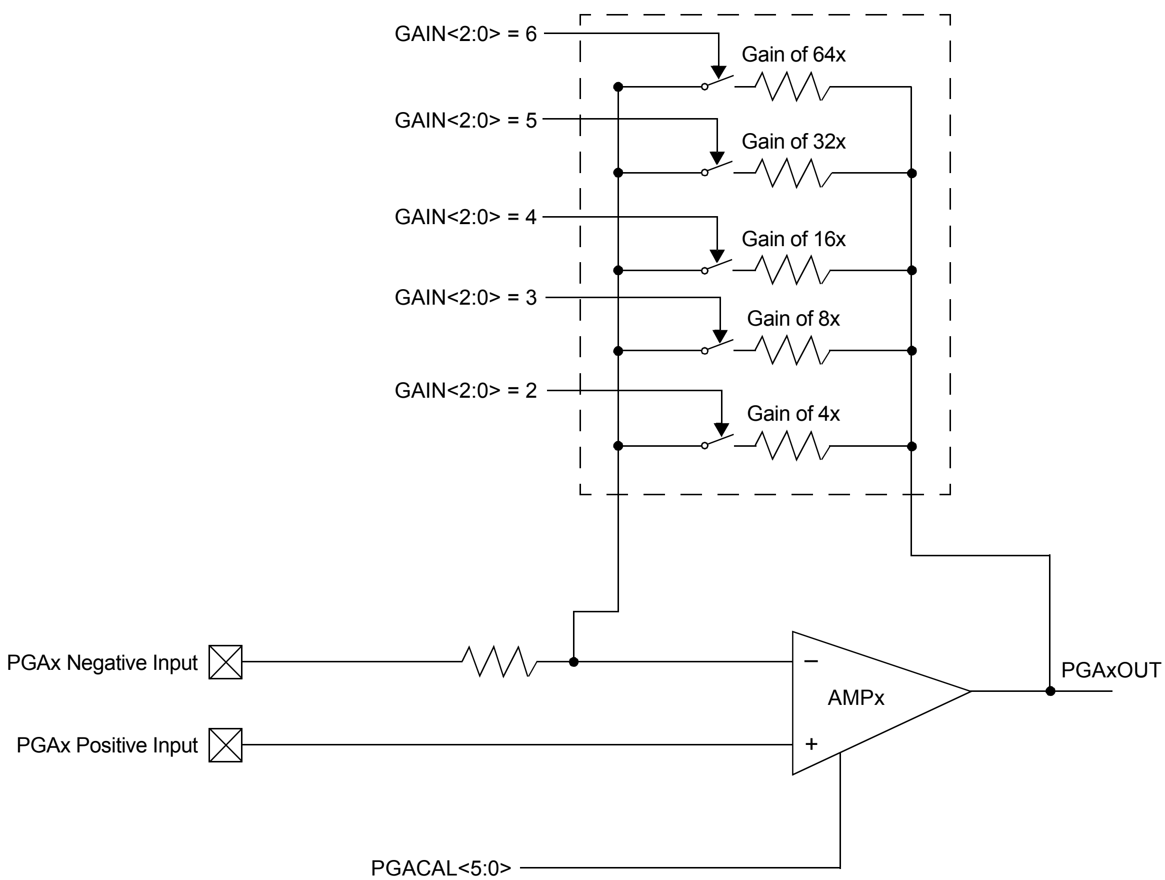
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGS70X/80X family devices have two Programmable Gain Amplifiers (PGA1, PGA2). The PGA is an op amp-based, non-inverting amplifier with user-programmable gains. The output of the PGA can be connected to a number of dedicated Sample-and-Hold inputs of the Analog-to-Digital Converter and/or to the high-speed analog comparator module. The PGA has five selectable gains and may be used as a ground referenced amplifier (single-ended) or used with an independent ground reference point.

Key features of the PGA module include:

- Single-Ended or Independent Ground Reference
- Selectable Gains: 4x, 8x, 16x, 32x and 64x
- High Gain Bandwidth
- Rail-to-Rail Output Voltage
- Wide Input Voltage Range

FIGURE 25-1: PGAx MODULE BLOCK DIAGRAM



Note 1: x = 1 and 2.

25.2 PGA Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

25.2.1 KEY RESOURCES

- **"Programmable Gain Amplifier (PGA)"** (DS70005146) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

REGISTER 25-1: PGAxCON: PGAx CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	GAIN2	GAIN1	GAIN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **PGAEN:** PGAx Enable bit
1 = PGAx module is enabled
0 = PGAx module is disabled (reduces power consumption)

bit 14 **PGAOEN:** PGAx Output Enable bit
1 = PGAx output is connected to the DACOUTx pin
0 = PGAx output is not connected to the DACOUTx pin

bit 13-11 **SELPI<2:0>:** PGAx Positive Input Selection bits
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = PGAxP4
010 = PGAxP3
001 = PGAxP2
000 = PGAxP1

bit 10-8 **SELNI<2:0>:** PGAx Negative Input Selection bits
111 = Reserved
110 = Reserved
101 = Reserved
100 = Reserved
011 = Ground (Single-Ended mode)
010 = PGAxN3
001 = PGAxN2
000 = Ground (Single-Ended mode)

bit 7-3 **Unimplemented:** Read as '0'

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	V_{OL}	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	V_{DD} = 3.3V, I_{OL} ≤ 6 mA, -40°C ≤ T_A ≤ +85°C, I_{OL} ≤ 5 mA, +85°C < T_A ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins(3)	—	—	0.4	V	V_{DD} = 3.3V, I_{OL} ≤ 12 mA, -40°C ≤ T_A ≤ +85°C, I_{OL} ≤ 8 mA, +85°C < T_A ≤ +125°C
DO20	V_{OH}	**Output High Voltage** 4x Source Driver Pins(2)	2.4	—	—	V	I_{OH} ≥ -10 mA, V_{DD} = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	2.4	—	—	V	I_{OH} ≥ -15 mA, V_{DD} = 3.3V
DO20A	V_{OH1}	**Output High Voltage** 4x Source Driver Pins(2)	1.5(1)	—	—	V	I_{OH} ≥ -14 mA, V_{DD} = 3.3V
			2.0(1)	—	—		I_{OH} ≥ -12 mA, V_{DD} = 3.3V
			3.0(1)	—	—		I_{OH} ≥ -7 mA, V_{DD} = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	1.5(1)	—	—	V	I_{OH} ≥ -22 mA, V_{DD} = 3.3V
			2.0(1)	—	—		I_{OH} ≥ -18 mA, V_{DD} = 3.3V
			3.0(1)	—	—		I_{OH} ≥ -10 mA, V_{DD} = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes RA0-RA2, RB0-RB1, RB9, RC1-RC2, RC9-RC10, RC12, RD7, RD8, RE4-RE5, RE8-RE9 and RE12-RE13 pins.

3: Includes all I/O pins that are not 4x driver pins (see **Note 2**).

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ T_A ≤ +85°C for Industrial -40°C ≤ T_A ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.(2)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	V_{BOR}	BOR Event on V_{DD} Transition High-to-Low	2.65	—	2.95	V	V_{DD} **(Notes 2** and **3)**

Note 1: Device is functional at V_{BORMIN} < V_{DD} < V_{DDMIN}, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, PGAs and comparators) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The V_{BOR} specification is relative to V_{DD}.

TABLE 30-20: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
Internal FRC Accuracy @ FRC Frequency = 7.37 MHz(1)							
F20a	FRC	-2	0.5	+2	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-0.9	0.5	+0.9	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F20b	FRC	-2	1	+2	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: Frequency is calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

TABLE 30-21: INTERNAL LPRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended					
Param No.	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**	
LPRC @ 32.768 kHz(1)							
F21a	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ -10°C	VDD = 3.0-3.6V
		-20	—	+20	%	-10°C ≤ TA ≤ +85°C	VDD = 3.0-3.6V
F21b	LPRC	-30	—	+30	%	+85°C ≤ TA ≤ +125°C	VDD = 3.0-3.6V

Note 1: This is the change of the LPRC frequency as VDD changes.

FIGURE 30-9: HIGH-SPEED PWMx MODULE FAULT TIMING CHARACTERISTICS

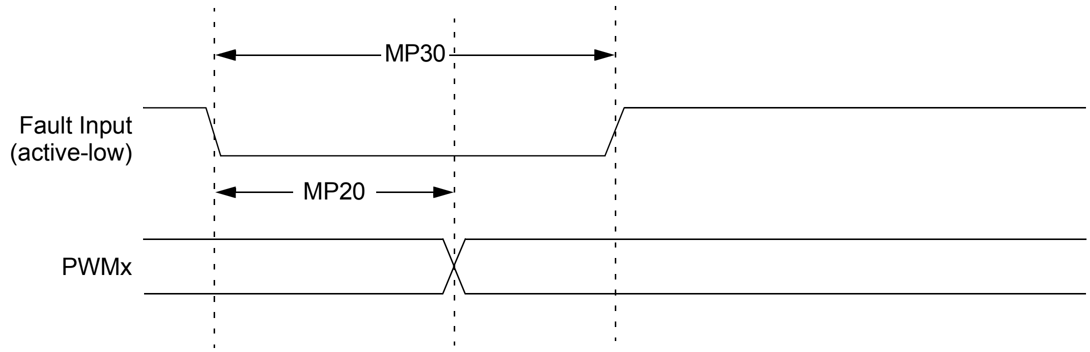
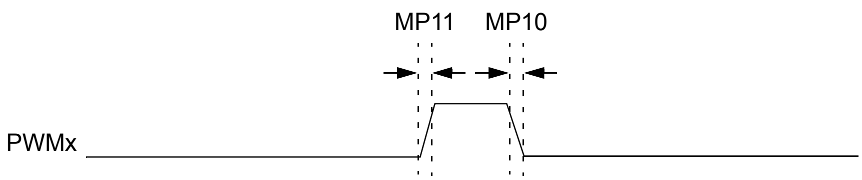


FIGURE 30-10: HIGH-SPEED PWMx MODULE TIMING CHARACTERISTICS



Note: Refer to Figure 30-1 for load conditions.

TABLE 30-30: HIGH-SPEED PWMx MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic[1]**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
MP10	TFPWM	PWMx Output Fall Time	—	—	—	ns	See Parameter DO32
MP11	TRPWM	PWMx Output Rise Time	—	—	—	ns	See Parameter DO31
MP20	TFD	Fault Input ↓ to PWMx I/O Change	—	—	15	ns	
MP30	TFH	Fault Input Pulse Width	15	—	—	ns	

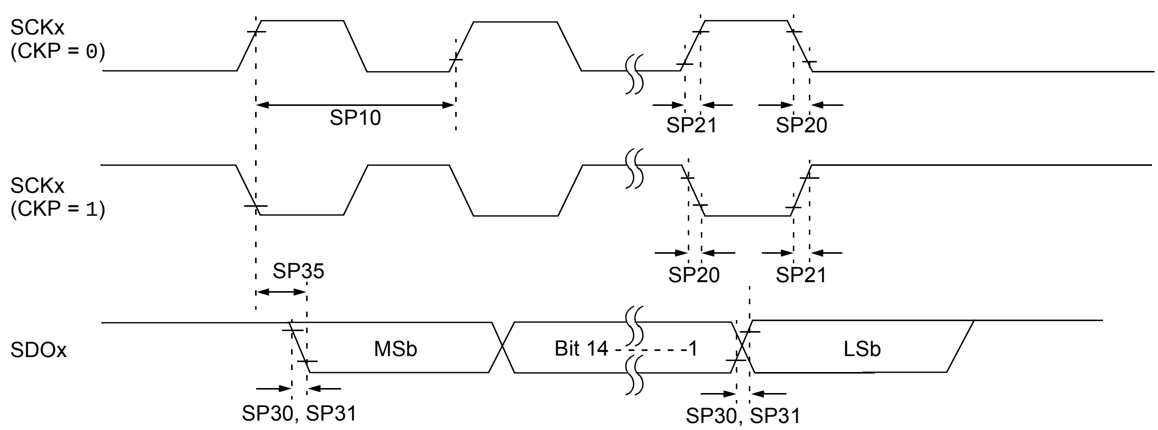
Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-31: SPI1, SPI2 AND SPI3 MAXIMUM DATA/CLOCK RATE SUMMARY(1)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Maximum Data Rate	**Master Transmit Only (Half-Duplex)**	**Master Transmit/Receive (Full-Duplex)**	**Slave Transmit/Receive (Full-Duplex)**	**CKE**	**CKP**	**SMP**
15 MHz	Table 30-32	—	—	0,1	0,1	0,1
9 MHz	—	Table 30-33	—	1	0,1	1
9 MHz	—	Table 30-34	—	0	0,1	1
15 MHz	—	—	Table 30-35	1	0	0
11 MHz	—	—	Table 30-36	1	1	0
15 MHz	—	—	Table 30-37	0	1	0
11 MHz	—	—	Table 30-38	0	0	0

Note 1: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

FIGURE 30-11: SPI1, SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS(1,2)



Note 1: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

2: Refer to Figure 30-1 for load conditions.

TABLE 30-57: PGAx MODULE SPECIFICATIONS

AC/DC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)[1] Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**		**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
PA01	VIN	Input Voltage Range		AVSS – 0.3	—	AVDD + 0.3	V	
PA02	VCM	Common-Mode Input Voltage Range		AVSS	—	AVDD – 1.6	V	
PA03	VOS	Input Offset Voltage		-10	—	10	mV	
PA04	VOS	Input Offset Voltage Drift with Temperature		—	±15	—	μV/°C	
PA05	RIN+	Input Impedance of Positive Input		—	>1M || 7 pF	—	Ω|| pF	
PA06	RIN-	Input Impedance of Negative Input		—	10K || 7 pF	—	Ω|| pF	
PA07	GERR	Gain Error		-2	—	2	%	Gain = 4x, 8x
				-3	—	3	%	Gain = 16x
				-4	—	4	%	Gain = 32x, 64x
PA08	LERR	Gain Nonlinearity Error		—	—	0.5	%	% of full scale, Gain = 16x
PA09	IDD	Current Consumption		—	2.0	—	mA	Module is enabled with a 2-volt P-P output voltage swing
PA10a	BW	Small Signal Bandwidth (-3 dB)	G = 4x	—	10	—	MHz	
PA10b			G = 8x	—	5	—	MHz	
PA10c			G = 16x	—	2.5	—	MHz	
PA10d			G = 32x	—	1.25	—	MHz	
PA10e			G = 64x	—	0.625	—	MHz	
PA11	OST	Output Settling Time to 1% of Final Value		—	0.4	—	μs	Gain = 16x, 100 mV input step change
PA12	SR	Output Slew Rate		—	40	—	V/μs	Gain = 16x
PA13	TGSEL	Gain Selection Time		—	1	—	μs	
PA14	TON	Module Turn On/Setting Time		—	—	10	μs	

Note 1: The PGAx module is functional at VBORMIN < VDD < VDDMIN, but with degraded performance. Unless otherwise stated, module functionality is tested, but not characterized.

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