Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs708t-i-pt

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name(1)	Pin Type	Buffer Type	PPS	Description
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
BCLK2	O	ST	Yes	UART2 IrDA baud clock output.
SCK1	I/O	ST	Yes	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	Yes	SPI1 data in.
SDO1	O	—	Yes	SPI1 data out.
SS1	I/O	ST	Yes	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes(3)	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.
FLT1-FLT8	I	ST	Yes	PWM Fault Inputs 1 through 8.
FLT9-FLT12	I	ST	No	PWM Fault Inputs 9 through 12.
PWM1L-PWM3L	O	—	No	PWM Low Outputs 1 through 3.
PWM1H-PWM3H	O	—	No	PWM High Outputs 1 through 3.
PWM4L-PWM8L(2)	O	—	Yes	PWM Low Outputs 4 through 8.
PWM4H-PWM8H(2)	O	—	Yes	PWM High Outputs 4 through 8.
SYNCI1, SYNCI2	I	ST	Yes	PWM Synchronization Inputs 1 and 2.
SYNCO1, SYNCO2	O	—	Yes	PWM Synchronization Outputs 1 and 2.

Legend: CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

1: Not all pins are available in all package variants. See the **"Pin Diagrams"** section for pin availability.

2: PWM4H/L through PWM8H/L are fixed on dsPIC33EPXXXGS708/808 devices. PWM4H/L through PWM6H/L are fixed on dsPIC33EPXXXGS706/806 devices.

3: The SCK3 pin is fixed on dsPIC33EPXXXGS706/806 and dsPIC33EPXXXGS708/808 devices.

4: PPS is available on dsPIC33EPXXXGS702 devices only.

TABLE 4-8: SFR BLOCK 600h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
SPI			RPOR8	678	0000000000000000	RPINR7	6AE	0000000000000000
SPI3CON1L	600	0000000000000000	RPOR9	67A	0000000000000000	RPINR8	6B0	0000000000000000
SPI3CON1H	602	0000000000000000	RPOR10	67C	0000000000000000	RPINR11	6B6	0000000000000000
SPI3CON2L	604	0000000000000000	RPOR11	67E	0000000000000000	RPINR12	6B8	0000000000000000
SPI3CON2H	606	0000000000000000	RPOR12	680	0000000000000000	RPINR13	6BA	0000000000000000
SPI3STATL	608	0000000000101000	RPOR13	682	0000000000000000	RPINR18	6C4	0000000000000000
SPI3STATH	60A	0000000000000000	RPOR14	684	0000000000000000	RPINR19	6C6	0000000000000000
SPI3BUFL	60C	0000000000000000	RPOR15	686	0000000000000000	RPINR20	6C8	0000000000000000
SPI3BUFH	60E	0000000000000000	RPOR17	68A	0000000000000000	RPINR21	6CA	0000000000000000
SPI3BRGL	610	000xxxxxxxxxxxx	RPOR18	68C	0000000000000000	RPINR22	6CC	0000000000000000
SPI3BRGH	612	0000000000000000	RPOR19	68E	0000000000000000	RPINR23	6CE	0000000000000000
SPI3IMSKL	614	0000000000000000	RPOR20	690	0000000000000000	RPINR26	6D4	0000000000000000
SPI3IMSKH	616	0000000000000000	RPOR21	692	0000000000000000	RPINR29	6DA	0000000000000000
SPI3URDTL	618	0000000000000000	RPOR22	694	0000000000000000	RPINR30	6DC	0000000000000000
SPI3URDTH	61A	0000000000000000	RPOR23	696	0000000000000000	RPINR37	6EA	0000000000000000
RPOR0	668	0000000000000000	RPOR24	698	0000000000000000	RPINR38	6EC	0000000000000000
RPOR1	66A	0000000000000000	RPOR25	69A	0000000000000000	RPINR42	6F4	0000000000000000
RPOR2	66C	0000000000000000	RPOR26	69C	0000000000000000	RPINR43	6F6	0000000000000000
RPOR3	66E	0000000000000000	RPINR0	6A0	0000000000000000	RPINR45	6FA	0000000000000000
RPOR4	670	0000000000000000	RPINR1	6A2	0000000000000000	RPINR46	6FC	0000000000000000
RPOR5	672	0000000000000000	RPINR2	6A4	0000000000000000			
RPOR6	674	0000000000000000	RPINR3	6A6	0000000000000000			

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

TABLE 4-9: SFR BLOCK 700h

Register	Address	All Resets	Register	Address	All Resets	Register	Address	All Resets
NVM			C2INTF	78A	0000000000000000	C2RXF1SID	7C4	xxxxxxxxxxxxxxxx
NVMCON	728	0000000000000000	C2INTE	78C	0000000000000000	C2RXF1EID	7C6	xxxxxxxxxxxxxxxx
NVMADR	72A	0000000000000000	C2EC	78E	0000000000000000	C2RXF2SID	7C8	xxxxxxxxxxxxxxxx
NVMADRU	72C	0000000000000000	C2CFG1	790	0000000000000000	C2RXF2EID	7CA	xxxxxxxxxxxxxxxx
NVMKEY	72E	0000000000000000	C2CFG2	792	0x000xxxxxxxxxxx	C2RXF3SID	7CC	xxxxxxxxxxxxxxxx
NVMSRCADR	730	0000000000000000	C2FEN1	794	1111111111111111	C2RXF3EID	7CE	xxxxxxxxxxxxxxxx
NVMSRCADRH	732	0000000000000000	C2FMSKSEL1	798	0000000000000000	C2RXF4SID	7D0	xxxxxxxxxxxxxxxx
System Control			C2FMSKSEL2	79A	0000000000000000	C2RXF4EID	7D2	xxxxxxxxxxxxxxxx
RCON	740	0x00x0x01x0xxxxx	**CAN (WIN (C1CTR1<0>) = 0)**			C2RXF5SID	7D4	xxxxxxxxxxxxxxxx
OSCCON	742	0000000000000000	C2RXFUL1	7A0	0000000000000000	C2RXF5EID	7D6	xxxxxxxxxxxxxxxx
CLKDIV	744	0000000000000000	C2RXFUL2	7A2	0000000000000000	C2RXF6SID	7D8	xxxxxxxxxxxxxxxx
PLLFBD	746	0000000000000000	C2RXOVF1	7A8	0000000000000000	C2RXF6EID	7DA	xxxxxxxxxxxxxxxx
OSCTUN	748	0000000000000000	C2RXOVF2	7AA	0000000000000000	C2RXF7SID	7DC	xxxxxxxxxxxxxxxx
LFSR	74C	0000000000000000	C2TR01CON	7B0	0000000000000000	C2RXF7EID	7DE	xxxxxxxxxxxxxxxx
REFOCON	74E	0000000000000000	C2TR23CON	7B2	0000000000000000	C2RXF8SID	7E0	xxxxxxxxxxxxxxxx
ACLKCON	750	0000000000000000	C2TR45CON	7B4	0000000000000000	C2RXF8EID	7E2	xxxxxxxxxxxxxxxx
PMD			C2TR67CON	7B6	xxxxxxxxxxxxxxxx	C2RXF9SID	7E4	xxxxxxxxxxxxxxxx
PMD1	760	0000000000000000	C2RXD	7C0	xxxxxxxxxxxxxxxx	C2RXF9EID	7E6	xxxxxxxxxxxxxxxx
PMD2	762	0000000000000000	C2TXD	7C2	xxxxxxxxxxxxxxxx	C2RXF10SID	7E8	xxxxxxxxxxxxxxxx
PMD3	764	0000000000000000	**CAN (WIN (C1CTR1<0>) = 1)**			C2RXF10EID	7EA	xxxxxxxxxxxxxxxx
PMD4	766	0000000000000000	C2BUFPNT1	7A0	0000000000000000	C2RXF11SID	7EC	xxxxxxxxxxxxxxxx
PMD6	76A	0000000000000000	C2BUFPNT2	7A2	0000000000000000	C2RXF11EID	7EE	xxxxxxxxxxxxxxxx
PMD7	76C	0000000000000000	C2BUFPNT3	7A4	0000000000000000	C2RXF12SID	7F0	xxxxxxxxxxxxxxxx
PMD8	76E	0000000000000000	C2BUFPNT4	7A6	0000000000000000	C2RXF12EID	7F2	xxxxxxxxxxxxxxxx
CAN (WIN (C1CTR1<0>) = 0 or 1)			C2RXM0SID	7B0	xxxxxxxxxxxxxxxx	C2RXF13SID	7F4	xxxxxxxxxxxxxxxx
C2CTRL1	780	0000010010000000	C2RXM0EID	7B2	xxxxxxxxxxxxxxxx	C2RXF13EID	7F6	xxxxxxxxxxxxxxxx
C2CTRL2	782	0000000000000000	C2RXM1SID	7B4	xxxxxxxxxxxxxxxx	C2RXF14SID	7F8	xxxxxxxxxxxxxxxx
C2VEC	784	0000000001000000	C2RXM1EID	7B6	xxxxxxxxxxxxxxxx	C2RXF14EID	7FA	xxxxxxxxxxxxxxxx
C2FCTRL	786	0000000000000000	C2RXM2SID	7B8	xxxxxxxxxxxxxxxx	C2RXF15SID	7FC	xxxxxxxxxxxxxxxx
C2FIFO	788	0000000000000000	C2RXM2EID	7BA	xxxxxxxxxxxxxxxx	C2RXF15EID	7FE	xxxxxxxxxxxxxxxx

Legend: x = unknown or indeterminate value. Address values are in hexadecimal. Reset values are in binary.

REGISTER 7-5: INTCON3: INTERRUPT CONTROL REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	NAE
bit 15							bit 8

U-0	U-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0
—	—	—	DOOVR	—	—	—	APLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **NAE:** NVM Address Error Soft Trap Status bit
1 = NVM address error soft trap has occurred
0 = NVM address error soft trap has not occurred

bit 7-5 **Unimplemented:** Read as '0'

bit 4 **DOOVR:** DO Stack Overflow Soft Trap Status bit
1 = DO stack overflow soft trap has occurred
0 = DO stack overflow soft trap has not occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **APLL:** Auxiliary PLL Loss of Lock Soft Trap Status bit
1 = APLL lock soft trap has occurred
0 = APLL lock soft trap has not occurred

REGISTER 7-6: INTCON4: INTERRUPT CONTROL REGISTER 4

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SGHT
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-1 **Unimplemented:** Read as '0'

bit 0 **SGHT:** Software Generated Hard Trap Status bit
1 = Software generated hard trap has occurred
0 = Software generated hard trap has not occurred

REGISTER 11-27: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCI1R7	SYNCI1R6	SYNCI1R5	SYNCI1R4	SYNCI1R3	SYNCI1R2	SYNCI1R1	SYNCI1R0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **SYNCI1R<7:0>:** Assign PWM Synchronization Input 1 (SYNCI1) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

bit 7-0 **Unimplemented:** Read as ‘0’

REGISTER 11-28: RPINR38: PERIPHERAL PIN SELECT INPUT REGISTER 38

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SYNCI2R7	SYNCI2R6	SYNCI2R5	SYNCI2R4	SYNCI2R3	SYNCI2R2	SYNCI2R1	SYNCI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **SYNCI2R<7:0>:** Assign PWM Synchronization Input 2 (SYNCI2) to the Corresponding RPn Pin bits
See Table 11-11 which contains a list of remappable inputs for the index value.

REGISTER 11-39: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP40R6	RP40R5	RP40R4	RP40R3	RP40R2	RP40R1	RP40R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP39R6	RP39R5	RP39R4	RP39R3	RP39R2	RP39R1	RP39R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP40R<6:0>:** Peripheral Output Function is Assigned to RP40 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP39R<6:0>:** Peripheral Output Function is Assigned to RP39 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-40: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP43R6	RP43R5	RP43R4	RP43R3	RP43R2	RP43R1	RP43R0
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	RP41R6	RP41R5	RP41R4	RP41R3	RP41R2	RP41R1	RP41R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **RP43R<6:0>:** Peripheral Output Function is Assigned to RP43 Output Pin bits (see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **RP41R<6:0>:** Peripheral Output Function is Assigned to RP41 Output Pin bits (see Table 11-13 for peripheral function numbers)

12.2 Timer1 Control Register

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON(1)	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	—	TSYNC(1)	TCS(1)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timer1 On bit(1)
1 = Starts 16-bit Timer1
0 = Stops 16-bit Timer1

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timer1 Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timer1 Gated Time Accumulation Enable bit
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timer1 Input Clock Prescale Select bits
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3 **Unimplemented:** Read as '0'

bit 2 **TSYNC:** Timer1 External Clock Input Synchronization Select bit(1)
When TCS = 1:
1 = Synchronizes external clock input
0 = Does not synchronize external clock input
When TCS = 0:
This bit is ignored.

bit 1 **TCS:** Timer1 Clock Source Select bit(1)
1 = External clock is from pin, T1CK (on the rising edge)
0 = Internal clock (FP)

bit 0 **Unimplemented:** Read as '0'

Note 1: When Timer1 is enabled in External Synchronous Counter mode (TCS = 1, TSYNC = 1, TON = 1), any attempts by user software to write to the TMR1 register are ignored.

15.2 Output Compare Control Registers

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
—	—	OCSIDL	OCTSEL2	OCTSEL1	OCTSEL0	—	—
bit 15							bit 8

R/W-0	U-0	U-0	R/W-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0
ENFLTA	—	—	OCFLTA	TRIGMODE	OCM2	OCM1	OCM0
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **OCSIDL:** Output Compare x Stop in Idle Mode Control bit
- 1 = Output Compare x halts in CPU Idle mode
- 0 = Output Compare x continues to operate in CPU Idle mode

bit 12-10 **OCTSEL<2:0>:** Output Compare x Clock Select bits
- 111 = Peripheral clock (FP)
- 110 = Reserved
- 101 = Reserved
- 100 = T1CLK is the clock source of the OCx (only the synchronous clock is supported)
- 011 = T5CLK is the clock source of the OCx
- 010 = T4CLK is the clock source of the OCx
- 001 = T3CLK is the clock source of the OCx
- 000 = T2CLK is the clock source of the OCx

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **ENFLTA:** Fault A Input Enable bit
- 1 = Output Compare Fault A input (OCFA) is enabled
- 0 = Output Compare Fault A input (OCFA) is disabled

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **OCFLTA:** PWM Fault A Condition Status bit
- 1 = PWM Fault A condition on the OCFA pin has occurred
- 0 = No PWM Fault A condition on the OCFA pin has occurred

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
- 1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
- 0 = TRIGSTAT is cleared only by software

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

REGISTER 16-12: PWMCONx: PWMx CONTROL REGISTER (x = 1 to 8)

R-0, HSC	R-0, HSC	R-0, HSC	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT(1)	CLSTAT(1)	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB(3)	MDCS(3)
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	—	—	MTBS	CAM(2,3,4)	XPRES(5)	IUE
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTSTAT:** Fault Interrupt Status bit(1)
1 = Fault interrupt is pending
0 = No Fault interrupt is pending
This bit is cleared by setting FLTIEN = 0.

bit 14 **CLSTAT:** Current-Limit Interrupt Status bit(1)
1 = Current-limit interrupt is pending
0 = No current-limit interrupt is pending
This bit is cleared by setting CLIEN = 0.

bit 13 **TRGSTAT:** Trigger Interrupt Status bit
1 = Trigger interrupt is pending
0 = No trigger interrupt is pending
This bit is cleared by setting TRGIEN = 0.

bit 12 **FLTIEN:** Fault Interrupt Enable bit
1 = Fault interrupt is enabled
0 = Fault interrupt is disabled and the FLTSTAT bit is cleared

bit 11 **CLIEN:** Current-Limit Interrupt Enable bit
1 = Current-limit interrupt is enabled
0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared

bit 10 **TRGIEN:** Trigger Interrupt Enable bit
1 = A trigger event generates an interrupt request
0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared

bit 9 **ITB:** Independent Time Base Mode bit(3)
1 = PHASEx/SPHASEx registers provide the time base period for this PWMx generator
0 = PTPER register provides timing for this PWMx generator

bit 8 **MDCS:** Master Duty Cycle Register Select bit(3)
1 = MDC register provides duty cycle information for this PWMx generator
0 = PDCx and SDCx registers provide duty cycle information for this PWMx generator

Note 1: Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.

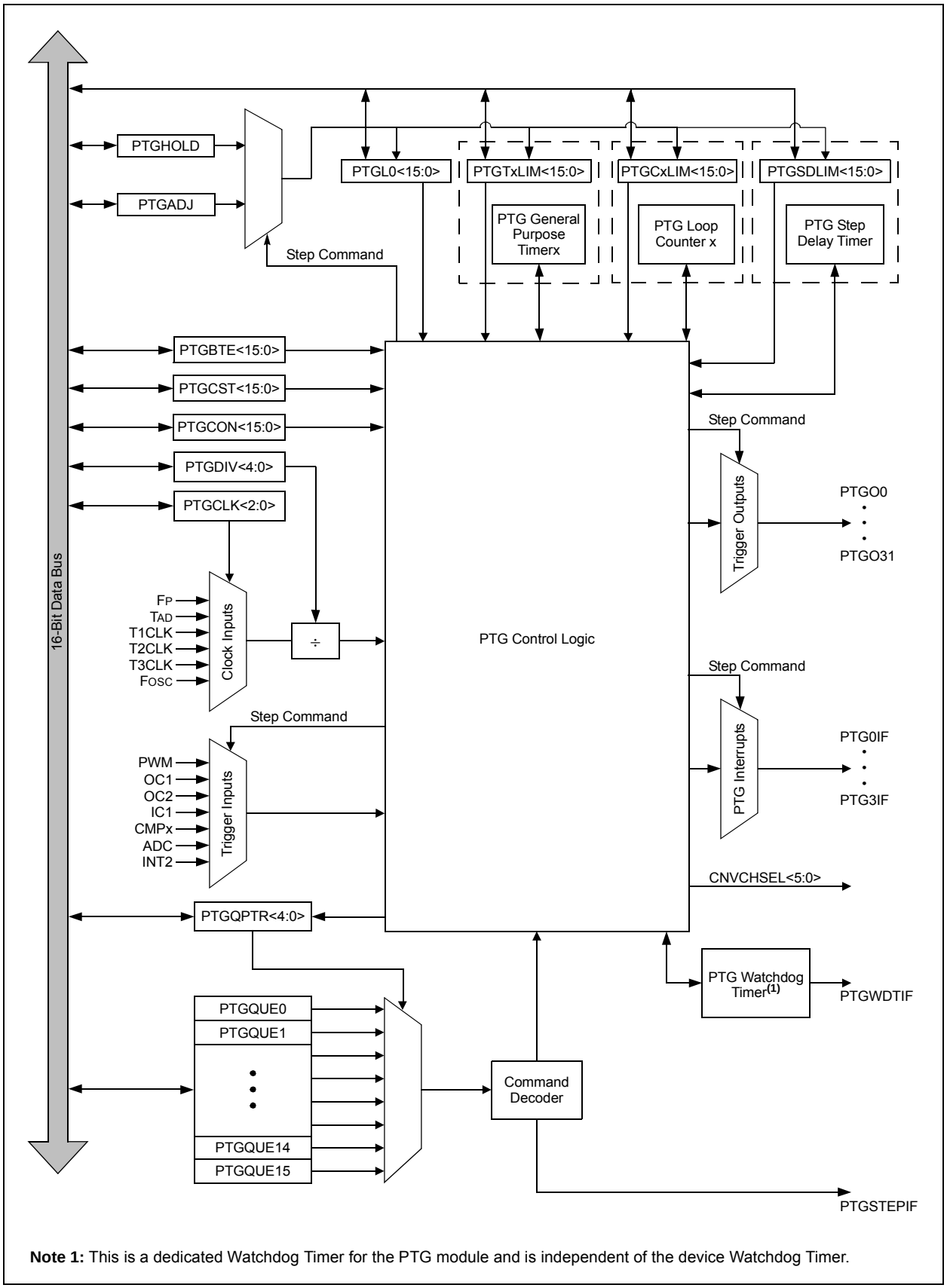
2: The Independent Time Base mode (ITB = 1) must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.

3: These bits should not be changed after the PWMx is enabled by setting PTEN (PTCON<15>) = 1.

4: Center-Aligned mode ignores the Least Significant 3 bits of the Duty Cycle, Phase and Dead-Time registers. The highest Center-Aligned mode resolution available is 8.32 ns with the clock prescaler set to the fastest clock.

5: Configure CLMOD (FCLCONx<8>) = 0 and ITB (PWMCONx<9>) = 1 to operate in External Period Reset mode.

FIGURE 17-1: PTG BLOCK DIAGRAM



Note 1: This is a dedicated Watchdog Timer for the PTG module and is independent of the device Watchdog Timer.

To set up the SPIx module for Audio mode:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   a) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with AUDEN (SPIxCON1H<15>) = 1.
4. Clear the SPIROV bit (SPIxSTATL<6>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

REGISTER 18-1: SPIxCON1L: SPIx CONTROL REGISTER 1 LOW

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPIEN	—	SPISIDL	DISSDO	MODE32(1,4)	MODE16(1,4)	SMP	CKE(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SSEN(2)	CKP	MSTEN	DISSDI	DISSCK	MCLKEN(3)	SPIFE	ENHBUF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **SPIEN:** SPIx On bit
1 = Enables module
0 = Turns off and resets module, disables clocks, disables interrupt event generation, allows SFR modifications

bit 14 **Unimplemented:** Read as '0'

bit 13 **SPISIDL:** SPIx Stop in Idle Mode bit
1 = Halts in CPU Idle mode
0 = Continues to operate in CPU Idle mode

bit 12 **DISSDO:** Disable SDOx Output Port bit
1 = SDOx pin is not used by the module; pin is controlled by port function
0 = SDOx pin is controlled by the module

bit 11-10 **MODE32** and **MODE16:** Serial Word Length Select bits(1,4)

MODE32	MODE16	AUDEN	Communication
1	x	0	32-Bit
0	1		16-Bit
0	0		8-Bit
1	1	1	24-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame
1	0		32-Bit Data, 32-Bit FIFO, 32-Bit Channel/64-Bit Frame
0	1		16-Bit Data, 16-Bit FIFO, 32-Bit Channel/64-Bit Frame
0	0		16-Bit FIFO, 16-Bit Channel/32-Bit Frame

Note 1: When AUDEN (SPIxCON1H<15>) = 1, this module functions as if CKE = 0, regardless of its actual value.
2: When FRMEN = 1, SSEN is not used.
3: MCLKEN can only be written when the SPIEN bit = 0.
4: This channel is not meaningful for DSP/PCM mode as LRC follows FRMSYPW.

REGISTER 19-2: I2CxCONH: I2Cx CONTROL REGISTER HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **PCIE:** Stop Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Stop condition
0 = Stop detection interrupts are disabled

bit 5 **SCIE:** Start Condition Interrupt Enable bit (I^2C Slave mode only)
1 = Enables interrupt on detection of Start or Restart conditions
0 = Start detection interrupts are disabled

bit 4 **BOEN:** Buffer Overwrite Enable bit (I^2C Slave mode only)
1 = I2CxRCV is updated and ACK is generated for a received address/data byte, ignoring the state of the I2COV only if the RBF bit = 0
0 = I2CxRCV is only updated when I2COV is clear

bit 3 **SDAHT:** SDAx Hold Time Selection bit
1 = Minimum of 300 ns hold time on SDAx after the falling edge of SCLx
0 = Minimum of 100 ns hold time on SDAx after the falling edge of SCLx

bit 2 **SBCDE:** Slave Mode Bus Collision Detect Enable bit (I^2C Slave mode only)
1 = Enables slave bus collision interrupts
0 = Slave bus collision interrupts are disabled
If the rising edge of SCLx and SDAx is sampled low when the module is in a high state, the BCL bit is set and the bus goes Idle. This Detection mode is only valid during data and ACK transmit sequences.

bit 1 **AHEN:** Address Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a matching received address byte, the SCLREL (I2CxCONL<12>) bit will be cleared and SCLx will be held low
0 = Address holding is disabled

bit 0 **DHEN:** Data Hold Enable bit (I^2C Slave mode only)
1 = Following the 8th falling edge of SCLx for a received data byte, the slave hardware clears the SCLREL (I2CxCONL<12>) bit and SCLx is held low
0 = Data holding is disabled

TABLE 21-1: CLC1 MULTIPLEXER INPUT SOURCES

DSx<2:0>		Signal Source
DS1<2:0>	000	CLCINA
	001	System Clock
	010	Timer1 Match
	011	PWM1H
	100	PWM5L
	101	High-Speed PWM Clock
	110	Timer2 Match
	111	Timer3 Match
DS2<2:0>	000	CLCINB
	001	CLC2 Out
	010	CMP1 Out
	011	UART1 TX Out
	100	ADC End-of-Conversion
	101	DMA Channel 0 Interrupt
	110	PWM1L
	111	PWM5H
DS3<2:0>	000	CLCINA
	001	CLC1 Out
	010	CMP2 Out
	011	SPI1 SDO Out
	100	UART1 RX
	101	PWM2H
	110	PWM6L
	111	OCMP2
DS4<2:0>	000	CLCINB
	001	CLC2 Out
	010	CMP3 Out
	011	SDI1
	100	PTG
	101	ECAN1
	110	PWM2L
	111	PWM6H

REGISTER 22-8: ADCON4H: ADC CONTROL REGISTER 4 HIGH

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C3CHS1	C3CHS0	C2CHS1	C2CHS0	C1CHS1	C1CHS0	C0CHS1	C0CHS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-6 **C3CHS<1:0>:** Dedicated ADC Core 3 Input Channel Selection bits
1x = Reserved
01 = AN15 (differential negative input when DIFF3 (ADMOD0L<7>) = 1)
00 = AN3

bit 5-4 **C2CHS<1:0>:** Dedicated ADC Core 2 Input Channel Selection bits
11 = Reserved
10 = VREF band gap
01 = AN11 (differential negative input when DIFF2 (ADMOD0L<5>) = 1)
00 = AN2

bit 3-2 **C1CHS<1:0>:** Dedicated ADC Core 1 Input Channel Selection bits
11 = AN1ALT
10 = PGA2
01 = AN18 (differential negative input when DIFF1 (ADMOD0L<3>) = 1)
00 = AN1

bit 1-0 **C0CHS<1:0>:** Dedicated ADC Core 0 Input Channel Selection bits
11 = AN0ALT
10 = PGA1
01 = AN7 (differential negative input when DIFF0 (ADMOD0L<1>) = 1)
00 = AN0

29.2 MPLAB XC Compilers

The MPLAB XC Compilers are complete ANSI C compilers for all of Microchip's 8, 16 and 32-bit MCU and DSC devices. These compilers provide powerful integration capabilities, superior code optimization and ease of use. MPLAB XC Compilers run on Windows, Linux or MAC OS X.

For easy source level debugging, the compilers provide debug information that is optimized to the MPLAB X IDE.

The free MPLAB XC Compiler editions support all devices and commands, with no time or memory restrictions, and offer sufficient code optimization for most applications.

MPLAB XC Compilers include an assembler, linker and utilities. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. MPLAB XC Compiler uses the assembler to produce its object file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

29.3 MPASM Assembler

The MPASM Assembler is a full-featured, universal macro assembler for PIC10/12/16/18 MCUs.

The MPASM Assembler generates relocatable object files for the MPLINK Object Linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contain source lines and generated machine code, and COFF files for debugging.

The MPASM Assembler features include:

- Integration into MPLAB X IDE projects
- User-defined macros to streamline assembly code
- Conditional assembly for multipurpose source files
- Directives that allow complete control over the assembly process

29.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK Object Linker combines relocatable objects created by the MPASM Assembler. It can link relocatable objects from precompiled libraries, using directives from a linker script.

The MPLIB Object Librarian manages the creation and modification of library files of precompiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

29.5 MPLAB Assembler, Linker and Librarian for Various Device Families

MPLAB Assembler produces relocatable machine code from symbolic assembly language for PIC24, PIC32 and dsPIC DSC devices. MPLAB XC Compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire device instruction set
- Support for fixed-point and floating-point data
- Command-line interface
- Rich directive set
- Flexible macro language
- MPLAB X IDE compatibility

30.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of the dsPIC33EPXXXGS70X/80X family electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGS70X/80X family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these, or any other conditions above the parameters indicated in the operation listings of this specification, is not implied.

Absolute Maximum Ratings(1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +150°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS}(3) ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$(3) ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$(3) ..... -0.3V to +3.6V
Maximum current out of V_{SS} pin ..... 300 mA
Maximum current into V_{DD} pin(2) ..... 300 mA
Maximum current sunk/sourced by any 4x I/O pin ..... 15 mA
Maximum current sunk/sourced by any 8x I/O pin ..... 25 mA
Maximum current sunk by all ports(2) ..... 200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those, or any other conditions above those indicated in the operation listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 30-2).

3: See the **“Pin Diagrams”** section for the 5V tolerant pins.

TABLE 30-12: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins(3)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	**Output High Voltage** 4x Source Driver Pins(2)	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** 4x Source Driver Pins(2)	1.5(1)	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(3)	1.5(1)	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0(1)	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0(1)	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Parameters are characterized but not tested.

2: Includes RA0-RA2, RB0-RB1, RB9, RC1-RC2, RC9-RC10, RC12, RD7, RD8, RE4-RE5, RE8-RE9 and RE12-RE13 pins.

3: Includes all I/O pins that are not 4x driver pins (see **Note 2**).

TABLE 30-13: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)(1) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.(2)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.65	—	2.95	V	VDD **(Notes 2** and **3)**

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules (ADC, PGAs and comparators) may have degraded performance.

2: Parameters are for design guidance only and are not tested in manufacturing.

3: The VBOR specification is relative to VDD.

TABLE 30-37: SPI1, SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0) TIMING REQUIREMENTS(5)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCKx Input Frequency	—	—	15	MHz	**(Note 3)**
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4**
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

5: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

F

Filter Capacitor (CEFC) Specifications 377
Flash Program Memory 61
  and Table Instructions 61
  Control Registers 64
  Dual Partition Flash Configuration 63
  Operations 62
  Resources 63
  RTSP Operation 62
Flexible Configuration 347

G

Getting Started Guidelines 15
  Connection Requirements 15
  CPU Logic Filter Capacitor Connection (VCAP) 16
  Decoupling Capacitors 15
  External Oscillator Pins 17
  ICSP Pins 17
  Master Clear ($\overline{MCLR}$) Pin 16
  Oscillator Value Conditions on Start-up 18
  Targeted Applications 18
  Unused I/Os 18

H

High-Speed Analog Comparator
  Applications 335
  Description 334
  Digital-to-Analog Comparator (DAC) 335
  Features Overview 333
  Hysteresis 336
  Pulse Stretcher and Digital Logic 335
  Resources 336
High-Speed PWM
  Features 187
  Resources 188
  Write-Protected Registers 188
High-Speed, 12-Bit Analog-to-Digital Converter (ADC) 273
  Control Registers 276
  Features Overview 273
  Resources 276

I

I/O Ports 125
  Configuring Analog/Digital Port Pins 130
  Control Registers 131
  Helpful Tips 140
  Open-Drain Configuration 130
  Parallel I/O (PIO) 125
  Register Maps 127
    PORTA 127
    PORTB 127
    PORTC 128
    PORTD 128
    PORTE 129
  Resources 141
  Write/Read Timing 130
In-Circuit Debugger 357
  MPLAB ICD 3 373
  PICkit 3 Programmer 373
In-Circuit Emulation 347
In-Circuit Serial Programming (ICSP) 347, 357
Input Capture 177
  Control Registers 178
  Resources 177
Input Change Notification (ICN) 130
Instruction Addressing Modes 53
  File Register Instructions 53
  Fundamental Modes Supported 53
  MAC Instructions 54
  MCU Instructions 53
  Move and Accumulator Instructions 54
  Other Instructions 54
Instruction Set Summary 361
  Overview 364
  Symbols Used in Opcode Descriptions 362
Instruction-Based Power-Saving Modes 115
  Idle 116
  Sleep 116
Inter-Integrated Circuit (I^2C) 245
  Control Registers 247
  Resources 245
Inter-Integrated Circuit. *See* I^2C.
Internet Address 474
Interrupt Controller
  Alternate Interrupt Vector Table (AIVT) 73
  Control and Status Registers 81
    INTCON1 81
    INTCON2 81
    INTCON3 81
    INTCON4 81
    INTTREG 81
  Interrupt Vector Details 76
  Interrupt Vector Table (IVT) 73
  Reset Sequence 73
  Resources 81
Interrupts Coincident with Power Save Instructions 116

J

JTAG Boundary Scan Interface 347
JTAG Interface 357

L

Leading-Edge Blanking (LEB) 187
LPRC Oscillator
  Use with WDT 356

M

Memory Organization 31
  Resources 39
  Special Function Register Maps 40
Microchip Internet Web Site 474
Modulo Addressing 55
  Applicability 56
  Operation Example 55
  Start and End Address 55
  W Address Register Selection 55
MPLAB REAL ICE In-Circuit Emulator System 373
MPLAB X Integrated Development
  Environment Software 371
MPLINK Object Linker/MPLIB Object Librarian 372
Multiplexer Input Sources
  CLC1 265
  CLC2 266
  CLC3 267
  CLC4 268

Timing Diagrams
BOR and Master Clear Reset Characteristics 391
CANx I/O 426
External Clock 388
High-Speed PWMx Fault Characteristics 397
High-Speed PWMx Module Characteristics 397
I/O Characteristics 391
I2Cx Bus Data (Master Mode) 422
I2Cx Bus Data (Slave Mode) 424
I2Cx Bus Start/Stop Bits (Master Mode) 422
I2Cx Bus Start/Stop Bits (Slave Mode) 424
Input Capture x (ICx) Characteristics 395
OCx/PWMx Characteristics 396
Output Compare x (OCx) Characteristics 396
SPI1, SPI2 and SPI3 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) 401
SPI1, SPI2 and SPI3 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) 400
SPI1, SPI2 and SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 0) 398
SPI1, SPI2 and SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 1) 399
SPI1, SPI2 and SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) 408
SPI1, SPI2 and SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) 406
SPI1, SPI2 and SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) 402
SPI1, SPI2 and SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) 404
SPI3 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) 413
SPI3 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) 412
SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 0) 410
SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 1) 411
SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) 420
SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) 418
SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) 414
SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) 416
Timer1-Timer5 External Clock Characteristics 393
UARTx I/O Characteristics 427

U

UART
Unique Device Identifier (UDID) 32
Universal Asynchronous Receiver
Transmitter (UART) 253
Control Registers 255
Helpful Tips 254
Resources 254
Universal Asynchronous Receiver Transmitter. *See* UART.
User OTP Memory 355

V

Voltage Regulator (On-Chip) 355

W

Watchdog Timer (WDT) 347, 356
Programming Considerations 356
WWW Address 474
WWW, On-Line Support 10