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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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#### Details

|                            |                                                                                                                                                                               |
|----------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Product Status             | Active                                                                                                                                                                        |
| Core Processor             | dsPIC                                                                                                                                                                         |
| Core Size                  | 16-Bit                                                                                                                                                                        |
| Speed                      | 70 MIPS                                                                                                                                                                       |
| Connectivity               | I <sup>2</sup> C, IrDA, LINbus, SPI, UART/USART                                                                                                                               |
| Peripherals                | Brown-out Detect/Reset, DMA, I <sup>2</sup> S, POR, PWM, WDT                                                                                                                  |
| Number of I/O              | 33                                                                                                                                                                            |
| Program Memory Size        | 64KB (64K x 8)                                                                                                                                                                |
| Program Memory Type        | FLASH                                                                                                                                                                         |
| EEPROM Size                | -                                                                                                                                                                             |
| RAM Size                   | 8K x 8                                                                                                                                                                        |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V                                                                                                                                                                     |
| Data Converters            | A/D 17x12b; D/A 1x12b                                                                                                                                                         |
| Oscillator Type            | Internal                                                                                                                                                                      |
| Operating Temperature      | -40°C ~ 85°C (TA)                                                                                                                                                             |
| Mounting Type              | Surface Mount                                                                                                                                                                 |
| Package / Case             | 44-VQFN Exposed Pad                                                                                                                                                           |
| Supplier Device Package    | 44-QFN (8x8)                                                                                                                                                                  |
| Purchase URL               | <a href="https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs804-i-ml">https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs804-i-ml</a> |

# dsPIC33EPXXXGS70X/80X FAMILY

## 4.5.1 PAGED MEMORY SCHEME

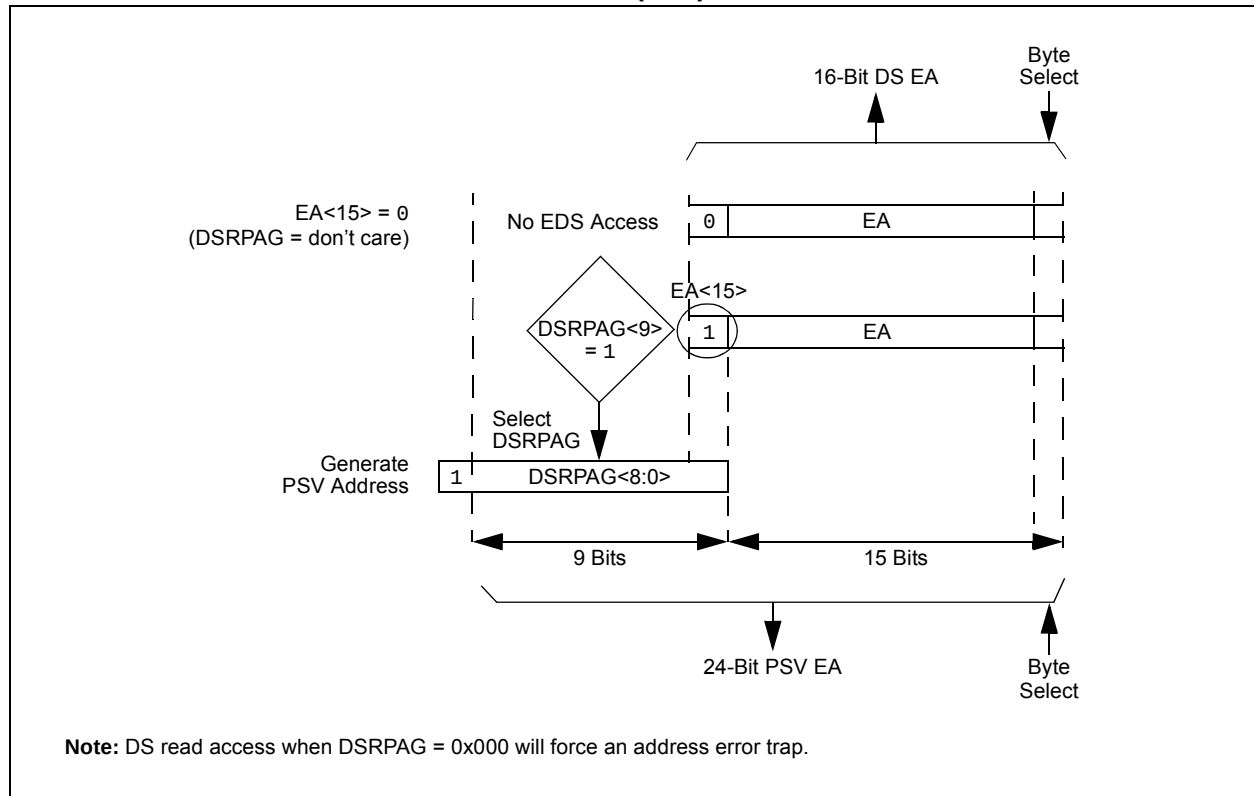
The dsPIC33EPXXXGS70X/80X family architecture extends the available Data Space through a paging scheme, which allows the available Data Space to be accessed using MOV instructions in a linear fashion for pre- and post-modified Effective Addresses (EAs). The upper half of the base Data Space address is used in conjunction with the Data Space Read Page (DSRPAG) register to form the Program Space Visibility (PSV) address.

The Data Space Read Page (DSRPAG) register is located in the SFR space. Construction of the PSV address is shown in Figure 4-7. When  $\text{DSRPAG}\langle 9 \rangle = 1$  and the base address bit,  $\text{EA}\langle 15 \rangle = 1$ , the  $\text{DSRPAG}\langle 8:0 \rangle$  bits are concatenated onto  $\text{EA}\langle 14:0 \rangle$  to form the 24-bit PSV read address.

The paged memory scheme provides access to multiple 32-Kbyte windows in the PSV memory. The Data Space Read Page (DSRPAG) register, in combination with the upper half of the Data Space address, can provide up to 8 Mbytes of PSV address space. The paged data memory space is shown in Figure 4-8.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG register.

**FIGURE 4-7: PROGRAM SPACE VISIBILITY (PSV) READ ADDRESS GENERATION**



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## 5.4 Dual Partition Flash Configuration

For dsPIC33EPXXXGS70X/80X devices operating in Dual Partition Flash Program Memory modes, the Inactive Partition can be erased and programmed without stalling the processor. The same programming algorithms are used for programming and erasing the Flash in the Inactive Partition, as described in **Section 5.2 “RTSP Operation”**. On top of the page erase option, the entire Flash memory of the Inactive Partition can be erased by configuring the NVMOP<3:0> bits in the NVMCON register.

**Note 1:** The application software to be loaded into the Inactive Partition will have the address of the Active Partition. The bootloader firmware will need to offset the address by 0x400000 in order to write to the Inactive Partition.

### 5.4.1 FLASH PARTITION SWAPPING

The Boot Sequence Number is used for determining the Active Partition at start-up and is encoded within the FBTSEQ Configuration register bits. Unlike most Configuration registers, which only utilize the lower 16 bits of the program memory, FBTSEQ is a 24-bit Configuration Word. The Boot Sequence Number (BSEQ) is a 12-bit value and is stored in FBTSEQ twice. The true value is stored in bits, FBTSEQ<11:0>, and its complement is stored in bits, FBTSEQ<23:12>. At device Reset, the sequence numbers are read and the partition with the lowest sequence number becomes the Active Partition. If one of the Boot Sequence Numbers is invalid, the device will select the partition with the valid Boot Sequence Number, or default to Partition 1 if both sequence numbers are invalid. See **Section 27.0 “Special Features”** for more information.

The BOOTSWP instruction provides an alternative means of swapping the Active and Inactive Partitions (soft swap) without the need for a device Reset. The BOOTSWP must always be followed by a GOTO instruction. The BOOTSWP instruction swaps the Active and Inactive Partitions, and the PC vectors to the location specified by the GOTO instruction in the newly Active Partition.

It is important to note that interrupts should temporarily be disabled while performing the soft swap sequence and that after the partition swap, all peripherals and interrupts which were enabled remain enabled. Additionally, the RAM and stack will maintain state after the switch. As a result, it is recommended that applications using soft swaps jump to a routine that will reinitialize the device in order to ensure the firmware runs as expected. The Configuration registers will have no effect during a soft swap.

For robustness of operation, in order to execute the BOOTSWP instruction, it is necessary to execute the NVM unlocking sequence as follows:

1. Write 0x55 to NVMKEY.
2. Write 0xAA to NVMKEY.
3. Execute the BOOTSWP instruction.

If the unlocking sequence is not performed, the BOOTSWP instruction will be executed as a forced NOP and a GOTO instruction, following the BOOTSWP instruction, will be executed, causing the PC to jump to that location in the current operating partition.

The SFTSWP and P2ACTIV bits in the NVMCON register are used to determine a successful swap of the Active and Inactive Partitions, as well as which partition is active. After the BOOTSWP and GOTO instructions, the SFTSWP bit should be polled to verify the partition swap has occurred and then cleared for the next panel swap event.

### 5.4.2 DUAL PARTITION MODES

While operating in Dual Partition mode, the dsPIC33EPXXXGS70X/80X family devices have the option for both partitions to have their own defined security segments, as shown in Figure 27-4. Alternatively, the device can operate in Protected Dual Partition mode, where Partition 1 becomes permanently erase/write-protected. Protected Dual Partition mode allows for a “Factory Default” mode, which provides a fail-safe backup image to be stored in Partition 1.

dsPIC33EPXXXGS70X/80X family devices can also operate in Privileged Dual Partition mode, where additional security protections are implemented to allow for protection of intellectual property when multiple parties have software within the device. In Privileged Dual Partition mode, both partitions place additional restrictions on the FBSLIM register. These prevent changes to the size of the Boot Segment and General Segment, ensuring that neither segment will be altered.

## 5.5 Flash Memory Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 5.5.1 KEY RESOURCES

- “Dual Partition Flash Program Memory” (DS70005156) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

# dsPIC33EPXXXGS70X/80X FAMILY

## REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

|                      |     |     |     |     |     |     |       |
|----------------------|-----|-----|-----|-----|-----|-----|-------|
| R/S-0                | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0   |
| FORCE <sup>(1)</sup> | —   | —   | —   | —   | —   | —   | —     |
| bit 15               |     |     |     |     |     |     | bit 8 |

|         |         |         |         |         |         |         |         |
|---------|---------|---------|---------|---------|---------|---------|---------|
| R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   | R/W-0   |
| IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 |
| bit 7   |         |         |         |         |         |         | bit 0   |

|                   |                      |
|-------------------|----------------------|
| <b>Legend:</b>    | S = Settable bit     |
| R = Readable bit  | W = Writable bit     |
| -n = Value at POR | '1' = Bit is set     |
|                   | '0' = Bit is cleared |
|                   | x = Bit is unknown   |

|          |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| bit 15   | <b>FORCE:</b> Force DMA Transfer bit <sup>(1)</sup><br>1 = Forces a single DMA transfer (Manual mode)<br>0 = Automatic DMA transfer initiation by DMA request                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| bit 14-8 | <b>Unimplemented:</b> Read as '0'                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
| bit 7-0  | <b>IRQSEL&lt;7:0&gt;:</b> DMA Peripheral IRQ Number Select bits<br>01000111 = CAN2 – TX data request<br>01000110 = CAN1 – TX data request<br>00110111 = CAN2 – RX data ready<br>00100110 = IC4 – Input Capture 4<br>00100101 = IC3 – Input Capture 3<br>00100010 = CAN1 – RX data ready<br>00011111 = UART2TX – UART2 transmitter<br>00011110 = UART2RX – UART2 receiver<br>00011100 = TMR5 – Timer5<br>00011011 = TMR4 – Timer4<br>00011010 = OC4 – Output Compare 4<br>00011001 = OC3 – Output Compare 3<br>00001100 = UART1TX – UART1 transmitter<br>00001011 = UART1RX – UART1 receiver<br>00001000 = TMR3 – Timer3<br>00000111 = TMR2 – Timer2<br>00000110 = OC2 – Output Compare 2<br>00000101 = IC2 – Input Capture 2<br>00000010 = OC1 – Output Compare 1<br>00000001 = IC1 – Input Capture 1<br>00000000 = INT0 – External Interrupt 0 |

**Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

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## REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

|        |     |     |     |     |     |     |       |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0    | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0   |
| —      | —   | —   | —   | —   | —   | —   | —     |
| bit 15 |     |     |     |     |     |     | bit 8 |

|       |     |     |     |        |        |        |        |
|-------|-----|-----|-----|--------|--------|--------|--------|
| U-0   | U-0 | U-0 | U-0 | R-0    | R-0    | R-0    | R-0    |
| —     | —   | —   | —   | RQCOL3 | RQCOL2 | RQCOL1 | RQCOL0 |
| bit 7 |     |     |     |        |        |        | bit 0  |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

# dsPIC33EPXXXGS70X/80X FAMILY

## REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)

bit 4-0 **PLLPRE<4:0>**: PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)  
11111 = Input divided by 33  
.  
.  
.  
00001 = Input divided by 3  
00000 = Input divided by 2 (default)

- Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.
- 2:** This bit is cleared when the ROI bit is set and an interrupt occurs.
- 3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

## REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER

|        |     |     |     |     |     |     |         |
|--------|-----|-----|-----|-----|-----|-----|---------|
| U-0    | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0   |
| —      | —   | —   | —   | —   | —   | —   | PLLDIV8 |
| bit 15 |     |     |     |     |     |     | bit 8   |

|             |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0       | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| PLLDIV<7:0> |       |       |       |       |       |       |       |
| bit 7       |       |       |       |       |       |       | bit 0 |

### Legend:

|                   |                  |                                    |
|-------------------|------------------|------------------------------------|
| R = Readable bit  | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared               |
|                   |                  | x = Bit is unknown                 |

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>**: PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)  
11111111 = 513  
.  
.  
.  
000110000 = 50 (default)  
.  
.  
.  
000000010 = 4  
000000001 = 3  
000000000 = 2

**TABLE 11-10: PORTE REGISTER MAP<sup>(1)</sup>**

| File Name | Bit 15      | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|-----------|-------------|--------|--------|--------|--------|--------|-------|-------|-------|-------|-------|-------|-------|-------|-------|-------|
| TRISE     | TRISE<15:0> |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| PORTE     | RE<15:0>    |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| LATE      | LATE<15:0>  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ODCE      | ODCE<15:0>  |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| CNENE     | CNIEE<15:0> |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| CNPUE     | CNPUE<15:0> |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| CNPDE     | CNPDE<15:0> |        |        |        |        |        |       |       |       |       |       |       |       |       |       |       |
| ANSELE    | —           | —      | —      | —      | —      | —      | —     | —     | —     | —     | —     | —     | —     | —     | —     | —     |

**Legend:** — = unimplemented, read as '0'.

**Note 1:** Refer to Table 11-5 for bit availability on each pin count variant.

# dsPIC33EPXXXGS70X/80X FAMILY

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6. The Peripheral Pin Select (PPS) pin mapping rules are as follows:

- a) Only one “output” function can be active on a given pin at any time, regardless if it is a dedicated or remappable function (one pin, one output).
- b) It is possible to assign a “remappable output” function to multiple pins and externally short or tie them together for increased current drive.
- c) If any “dedicated output” function is enabled on a pin, it will take precedence over any remappable “output” function.
- d) If any “dedicated digital” (input or output) function is enabled on a pin, any number of “input” remappable functions can be mapped to the same pin.
- e) If any “dedicated analog” function(s) are enabled on a given pin, “digital input(s)” of any kind will all be disabled, although a single “digital output”, at the user’s cautionary discretion, can be enabled and active as long as there is no signal contention with an external analog input signal. For example, it is possible for the ADC to convert the digital output logic level, or to toggle a digital output on a comparator or ADC input, provided there is no external analog input, such as for a built-in self-test.
- f) Any number of “input” remappable functions can be mapped to the same pin(s) at the same time, including to any pin with a single output from either a dedicated or remappable “output”.
- g) The TRISx registers control *only* the digital I/O output buffer. Any other dedicated or remappable active “output” will automatically override the TRISx setting. The TRISx register *does not* control the digital logic “input” buffer. Remappable digital “inputs” do not automatically override TRISx settings, which means that the TRISx bit must be set to input for pins with only remappable input function(s) assigned.
- h) All analog pins are enabled by default after any Reset and the corresponding digital input buffer on the pin has been disabled. Only the Analog Pin Select x (ANSELx) registers control the digital input buffer, *not* the TRISx register. The user must disable the analog function on a pin using the Analog Pin Select x registers in order to use any “digital input(s)” on a corresponding pin, no exceptions.

## 11.8 I/O Ports Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 11.8.1 KEY RESOURCES

- “**I/O Ports**” (DS70000598) in the “*dsPIC33/PIC24 Family Reference Manual*”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “*dsPIC33/PIC24 Family Reference Manual*” Sections
- Development Tools

# dsPIC33EPXXXGS70X/80X FAMILY

**REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER**

|        |     |        |          |       |                     |                        |                        |
|--------|-----|--------|----------|-------|---------------------|------------------------|------------------------|
| R/W-0  | U-0 | R/W-0  | R-0, HSC | R/W-0 | R/W-0               | R/W-0                  | R/W-0                  |
| PTEN   | —   | PTSIDL | SESTAT   | SEIEN | EIPU <sup>(1)</sup> | SYNCPOL <sup>(1)</sup> | SYNCOEN <sup>(1)</sup> |
| bit 15 |     |        |          |       |                     | bit 8                  |                        |

|                       |                         |                         |                         |                        |                        |                        |                        |
|-----------------------|-------------------------|-------------------------|-------------------------|------------------------|------------------------|------------------------|------------------------|
| R/W-0                 | R/W-0                   | R/W-0                   | R/W-0                   | R/W-0                  | R/W-0                  | R/W-0                  | R/W-0                  |
| SYNCEN <sup>(1)</sup> | SYNCSRC2 <sup>(1)</sup> | SYNCSRC1 <sup>(1)</sup> | SYNCSRC0 <sup>(1)</sup> | SEVTPS3 <sup>(1)</sup> | SEVTPS2 <sup>(1)</sup> | SEVTPS1 <sup>(1)</sup> | SEVTPS0 <sup>(1)</sup> |
| bit 7                 |                         |                         |                         |                        |                        | bit 0                  |                        |

|                   |                                       |                                    |                    |
|-------------------|---------------------------------------|------------------------------------|--------------------|
| <b>Legend:</b>    | HSC = Hardware Settable/Clearable bit |                                    |                    |
| R = Readable bit  | W = Writable bit                      | U = Unimplemented bit, read as '0' |                    |
| -n = Value at POR | '1' = Bit is set                      | '0' = Bit is cleared               | x = Bit is unknown |

- bit 15      **PTEN:** PWMx Module Enable bit  
1 = PWMx module is enabled  
0 = PWMx module is disabled
- bit 14      **Unimplemented:** Read as '0'
- bit 13      **PTSIDL:** PWMx Time Base Stop in Idle Mode bit  
1 = PWMx time base halts in CPU Idle mode  
0 = PWMx time base runs in CPU Idle mode
- bit 12      **SESTAT:** Special Event Interrupt Status bit  
1 = Special event interrupt is pending  
0 = Special event interrupt is not pending
- bit 11      **SEIEN:** Special Event Interrupt Enable bit  
1 = Special event interrupt is enabled  
0 = Special event interrupt is disabled
- bit 10      **EIPU:** Enable Immediate Period Updates bit<sup>(1)</sup>  
1 = Active Period register is updated immediately  
0 = Active Period register updates occur on PWMx cycle boundaries
- bit 9        **SYNCPOL:** Synchronize Input and Output Polarity bit<sup>(1)</sup>  
1 = SYNCIx/SYNCO1 polarity is inverted (active-low)  
0 = SYNCIx/SYNCO1 is active-high
- bit 8        **SYNCOEN:** Primary Time Base Synchronization Enable bit<sup>(1)</sup>  
1 = SYNCO1 output is enabled  
0 = SYNCO1 output is disabled
- bit 7        **SYNCEN:** External Time Base Synchronization Enable bit<sup>(1)</sup>  
1 = External synchronization of primary time base is enabled  
0 = External synchronization of primary time base is disabled
- bit 6-4      **SYNCSRC<2:0>:** Synchronous Source Selection bits<sup>(1)</sup>  
111 = Reserved  
101 = Reserved  
100 = Reserved  
011 = PTG Trigger Output 17  
010 = PTG Trigger Output 16  
001 = SYNCI2  
000 = SYNCI1

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCIx feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

# dsPIC33EPXXXGS70X/80X FAMILY

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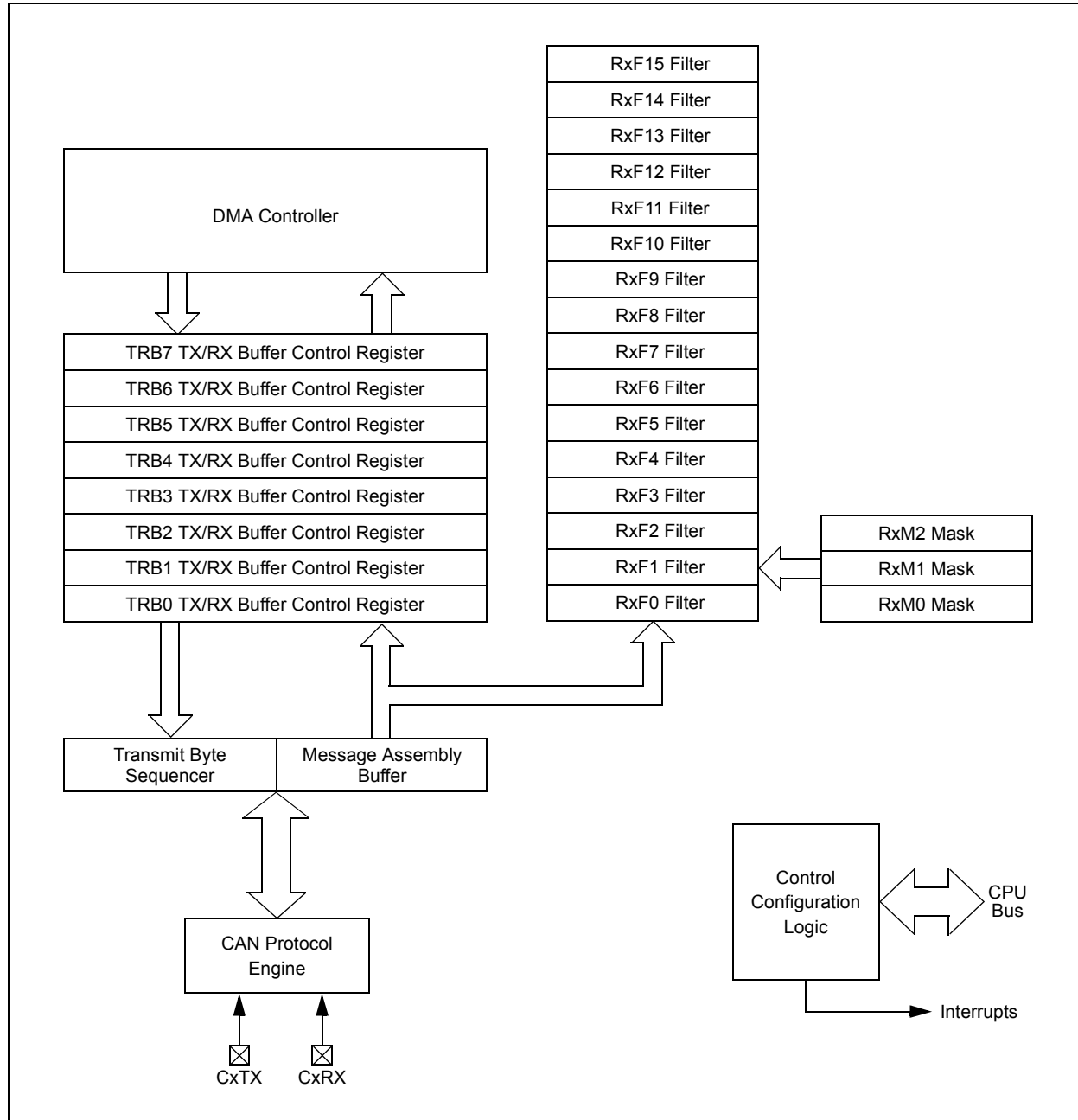
## REGISTER 22-26: ADTRIGxL: ADC CHANNEL TRIGGER x SELECTION REGISTER LOW (x = 0 to 5) (CONTINUED)

bit 4-0      **TRGSRC(4x)<4:0>**: Trigger Source Selection for Corresponding Analog Inputs bits

11111 = ADTRG31  
11110 = PTG Trigger Output 30  
11101 = PWM Generator 6 current-limit trigger  
11100 = PWM Generator 5 current-limit trigger  
11011 = PWM Generator 4 current-limit trigger  
11010 = PWM Generator 3 current-limit trigger  
11001 = PWM Generator 2 current-limit trigger  
11000 = PWM Generator 1 current-limit trigger  
10111 = Output Compare 2 trigger  
10110 = Output Compare 1 trigger  
10101 = CLC2 output  
10100 = PWM Generator 6 secondary trigger  
10011 = PWM Generator 5 secondary trigger  
10010 = PWM Generator 4 secondary trigger  
10001 = PWM Generator 3 secondary trigger  
10000 = PWM Generator 2 secondary trigger  
01111 = PWM Generator 1 secondary trigger  
01110 = PWM secondary Special Event Trigger  
01101 = Timer2 period match  
01100 = Timer1 period match  
01011 = CLC1 output  
01010 = PWM Generator 6 primary trigger  
01001 = PWM Generator 5 primary trigger  
01000 = PWM Generator 4 primary trigger  
00111 = PWM Generator 3 primary trigger  
00110 = PWM Generator 2 primary trigger  
00101 = PWM Generator 1 primary trigger  
00100 = PWM Special Event Trigger  
00011 = Reserved  
00010 = Level software trigger  
00001 = Common software trigger  
00000 = No trigger is enabled

# dsPIC33EPXXXGS70X/80X FAMILY

**FIGURE 23-1: CANx MODULE BLOCK DIAGRAM**



## 23.2 Modes of Operation

The CANx module can operate in one of several operation modes selected by the user. These modes include:

- Initialization mode
- Disable mode
- Normal Operation mode
- Listen Only mode
- Listen All Messages mode
- Loopback mode

Modes are requested by setting the REQOP<2:0> bits (CxCTRL1<10:8>). Entry into a mode is Acknowledged by monitoring the OPMODE<2:0> bits (CxCTRL1<7:5>). The module does not change the mode and the OPMODEx bits until a change in mode is acceptable, generally during bus Idle time, which is defined as at least 11 consecutive recessive bits.

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## REGISTER 23-2: CxCTRL2: CANx CONTROL REGISTER 2

|        |     |     |     |     |     |       |     |
|--------|-----|-----|-----|-----|-----|-------|-----|
| U-0    | U-0 | U-0 | U-0 | U-0 | U-0 | U-0   | U-0 |
| —      | —   | —   | —   | —   | —   | —     | —   |
| bit 15 |     |     |     |     |     | bit 8 |     |

|       |     |     |            |     |     |       |     |
|-------|-----|-----|------------|-----|-----|-------|-----|
| U-0   | U-0 | U-0 | R-0        | R-0 | R-0 | R-0   | R-0 |
| —     | —   | —   | DNCNT<4:0> |     |     |       |     |
| bit 7 |     |     |            |     |     | bit 0 |     |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-5

**Unimplemented:** Read as '0'

bit 4-0

**DNCNT<4:0>:** DeviceNet™ Filter Bit Number bits

10010-11111 = Invalid selection

10001 = Compare up to Data Byte 3, bit 6 with EID<17>

•

•

•

00001 = Compare up to Data Byte 1, bit 7 with EID<0>

00000 = Do not compare data bytes

# dsPIC33EPXXXGS70X/80X FAMILY

**REGISTER 23-16: CxRXFnSID: CANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)**

|        |       |       |       |       |       |       |       |
|--------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x  | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| SID10  | SID9  | SID8  | SID7  | SID6  | SID5  | SID4  | SID3  |
| bit 15 |       |       |       |       |       |       | bit 8 |
| R/W-x  | R/W-x | R/W-x | U-0   | R/W-x | U-0   | R/W-x | R/W-x |
| SID2   | SID1  | SID0  | —     | EXIDE | —     | EID17 | EID16 |
| bit 7  |       |       |       |       |       |       | bit 0 |

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-5      **SID<10:0>**: Standard Identifier bits  
1 = Message address bit, SIDx, must be '1' to match filter  
0 = Message address bit, SIDx, must be '0' to match filter
- bit 4      **Unimplemented**: Read as '0'
- bit 3      **EXIDE**: Extended Identifier Enable bit  
If MIDE = 1:  
1 = Matches only messages with Extended Identifier addresses  
0 = Matches only messages with Standard Identifier addresses  
If MIDE = 0:  
Ignores EXIDE bit.
- bit 2      **Unimplemented**: Read as '0'
- bit 1-0      **EID<17:16>**: Extended Identifier bits  
1 = Message address bit, EIDx, must be '1' to match filter  
0 = Message address bit, EIDx, must be '0' to match filter

**REGISTER 23-17: CxRXFnEID: CANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

|           |       |       |       |       |       |       |       |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x     | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID<15:8> |       |       |       |       |       |       |       |
| bit 15    |       |       |       |       |       |       | bit 8 |
| R/W-x     | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| EID<7:0>  |       |       |       |       |       |       |       |
| bit 7     |       |       |       |       |       |       | bit 0 |

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
-n = Value at POR                      '1' = Bit is set                      '0' = Bit is cleared                      x = Bit is unknown

- bit 15-0      **EID<15:0>**: Extended Identifier bits  
1 = Message address bit, EIDx, must be '1' to match filter  
0 = Message address bit, EIDx, must be '0' to match filter

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## BUFFER 21-5: CANx MESSAGE BUFFER WORD 4

|              |       |       |       |       |       |       |       |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x        | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| Byte 3<15:8> |       |       |       |       |       |       |       |
| bit 15       |       |       |       | bit 8 |       |       |       |

|             |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x       | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| Byte 2<7:0> |       |       |       |       |       |       |       |
| bit 7       |       |       |       | bit 0 |       |       |       |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8      **Byte 3<15:8>**: CANx Message Byte 3 bits

bit 7-0      **Byte 2<7:0>**: CANx Message Byte 2 bits

## BUFFER 21-6: CANx MESSAGE BUFFER WORD 5

|              |       |       |       |       |       |       |       |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x        | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| Byte 5<15:8> |       |       |       |       |       |       |       |
| bit 15       |       |       |       | bit 8 |       |       |       |

|             |       |       |       |       |       |       |       |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x       | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| Byte 4<7:0> |       |       |       |       |       |       |       |
| bit 7       |       |       |       | bit 0 |       |       |       |

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8      **Byte 5<15:8>**: CANx Message Byte 5 bits

bit 7-0      **Byte 4<7:0>**: CANx Message Byte 4 bits

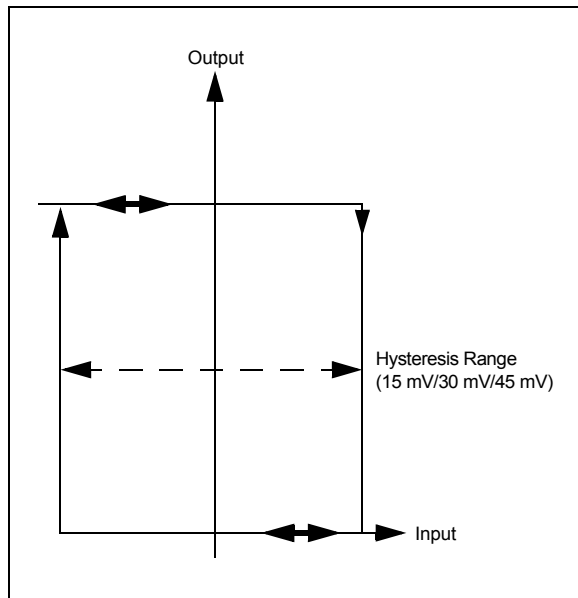
# dsPIC33EPXXXGS70X/80X FAMILY

## 24.6 Hysteresis

An additional feature of the module is hysteresis control. Hysteresis can be enabled or disabled and its amplitude can be controlled by the HYSSEL<1:0> bits in the CMPxCON register. Three different values are available: 15 mV, 30 mV and 45 mV. It is also possible to select the edge (rising or falling) to which hysteresis is to be applied.

Hysteresis control prevents the comparator output from continuously changing state because of small perturbations (noise) at the input (see Figure 24-2).

**FIGURE 24-2: HYSTERESIS CONTROL**



## 24.7 Analog Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 24.7.1 KEY RESOURCES

- **“High-Speed Analog Comparator Module”** (DS70005128) in the *“dsPIC33/PIC24 Family Reference Manual”*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *“dsPIC33/PIC24 Family Reference Manual”* Sections
- Development Tools

# dsPIC33EPXXXGS70X/80X FAMILY

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## REGISTER 24-1: CMPxCON: COMPARATOR x CONTROL REGISTER (CONTINUED)

- bit 5      **EXTREF:** Enable External Reference bit  
1 = External source provides reference to DACx (maximum DAC voltage is determined by the external voltage source)  
0 = AVDD provides reference to DACx (maximum DAC voltage is AVDD)
- bit 4      **HYSPOL:** Comparator Hysteresis Polarity Select bit  
1 = Hysteresis is applied to the falling edge of the comparator output  
0 = Hysteresis is applied to the rising edge of the comparator output
- bit 3      **CMPSTAT:** Comparator Current State bit  
Reflects the current output state of Comparator x, including the setting of the CMPPOL bit.
- bit 2      **ALTINP:** Alternate Input Select bit  
1 = INSEL<1:0> bits select alternate inputs  
0 = INSEL<1:0> bits select comparator inputs
- bit 1      **CMPPOL:** Comparator Output Polarity Control bit  
1 = Output is inverted  
0 = Output is non-inverted
- bit 0      **RANGE:** DACx Output Voltage Range Select bit  
1 = AVDD is the maximum DACx output voltage  
0 = Unimplemented, do not use

**Note 1:** DACOUTx can be associated only with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DACx output by setting their respective DACOE bit.

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Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSBs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In

these cases, the execution takes multiple instruction cycles, with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

**Note:** For more details on the instruction set, refer to the "16-bit MCU and DSC Programmer's Reference Manual" (DS70157).

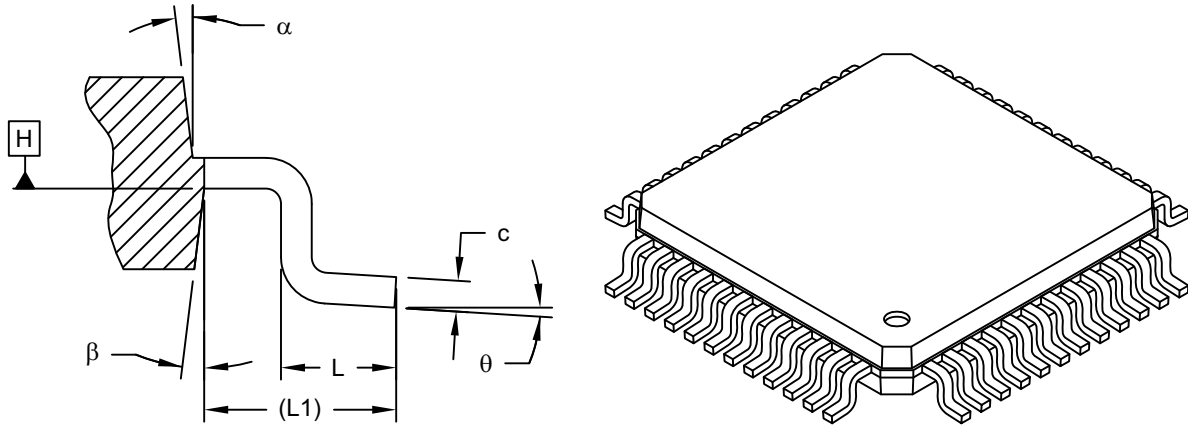
**TABLE 28-1: SYMBOLS USED IN OPCODE DESCRIPTIONS**

| Field               | Description                                                                                 |
|---------------------|---------------------------------------------------------------------------------------------|
| #text               | Means literal defined by "text"                                                             |
| (text)              | Means "content of text"                                                                     |
| [text]              | Means "the location addressed by text"                                                      |
| { }                 | Optional field or operation                                                                 |
| $a \in \{b, c, d\}$ | a is selected from the set of values b, c, d                                                |
| <n:m>               | Register bit field                                                                          |
| .b                  | Byte mode selection                                                                         |
| .d                  | Double-Word mode selection                                                                  |
| .S                  | Shadow register select                                                                      |
| .w                  | Word mode selection (default)                                                               |
| Acc                 | One of two accumulators {A, B}                                                              |
| AWB                 | Accumulator Write-Back Destination Address register $\in \{W13, [W13]+ = 2\}$               |
| bit4                | 4-bit bit selection field (used in word addressed instructions) $\in \{0...15\}$            |
| C, DC, N, OV, Z     | MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero                        |
| Expr                | Absolute address, label or expression (resolved by the linker)                              |
| f                   | File register address $\in \{0x0000...0x1FFF\}$                                             |
| lit1                | 1-bit unsigned literal $\in \{0,1\}$                                                        |
| lit4                | 4-bit unsigned literal $\in \{0...15\}$                                                     |
| lit5                | 5-bit unsigned literal $\in \{0...31\}$                                                     |
| lit8                | 8-bit unsigned literal $\in \{0...255\}$                                                    |
| lit10               | 10-bit unsigned literal $\in \{0...255\}$ for Byte mode, $\{0:1023\}$ for Word mode         |
| lit14               | 14-bit unsigned literal $\in \{0...16384\}$                                                 |
| lit16               | 16-bit unsigned literal $\in \{0...65535\}$                                                 |
| lit23               | 23-bit unsigned literal $\in \{0...8388608\}$ ; LSb must be '0'                             |
| None                | Field does not require an entry, can be blank                                               |
| OA, OB, SA, SB      | DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate                 |
| PC                  | Program Counter                                                                             |
| Slit10              | 10-bit signed literal $\in \{-512...511\}$                                                  |
| Slit16              | 16-bit signed literal $\in \{-32768...32767\}$                                              |
| Slit6               | 6-bit signed literal $\in \{-16...16\}$                                                     |
| Wb                  | Base W register $\in \{W0...W15\}$                                                          |
| Wd                  | Destination W register $\in \{Wd, [Wd], [Wd++] , [Wd--], [++Wd], [--Wd] \}$                 |
| Wdo                 | Destination W register $\in \{Wnd, [Wnd], [Wnd++] , [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] \}$ |
| Wm,Wn               | Dividend, Divisor Working register pair (Direct Addressing)                                 |

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## 48-Lead Thin Quad Flatpack (PT) - 7x7x1.0 mm Body [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



SECTION A-A

| Units                    |    | MILLIMETERS |      |      |
|--------------------------|----|-------------|------|------|
| Dimension Limits         |    | MIN         | NOM  | MAX  |
| Number of Leads          | N  | 48          |      |      |
| Lead Pitch               | e  | 0.50 BSC    |      |      |
| Overall Height           | A  | -           | -    | 1.20 |
| Standoff                 | A1 | 0.05        | -    | 0.15 |
| Molded Package Thickness | A2 | 0.95        | 1.00 | 1.05 |
| Foot Length              | L  | 0.45        | 0.60 | 0.75 |
| Footprint                | L1 | 1.00 REF    |      |      |
| Foot Angle               | φ  | 0°          | 3.5° | 7°   |
| Overall Width            | E  | 9.00 BSC    |      |      |
| Overall Length           | D  | 9.00 BSC    |      |      |
| Molded Package Width     | E1 | 7.00 BSC    |      |      |
| Molded Package Length    | D1 | 7.00 BSC    |      |      |
| Lead Thickness           | c  | 0.09        | -    | 0.16 |
| Lead Width               | b  | 0.17        | 0.22 | 0.27 |
| Mold Draft Angle Top     | α  | 11°         | 12°  | 13°  |
| Mold Draft Angle Bottom  | β  | 11°         | 12°  | 13°  |

**Notes:**

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.
- Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
REF: Reference Dimension, usually without tolerance, for information purposes only.
- Datums **A-B** and **D** to be determined at center line between leads where leads exit plastic body at datum plane **H**

Microchip Technology Drawing C04-300-PT Rev A Sheet 2 of 2

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