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### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, POR, PWM, WDT |
| Number of I/O | 33 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 17x12b; D/A 1x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs804t-i-ml |

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER**

| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R-0 | R-0 | R-0 |
|-------|-----|-------|-------|-------|-----|-----|-----|
| VAR | — | US1 | US0 | EDT[1] | DL2 | DL1 | DL0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/C-0 | R-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-----|-------|-------|
| SATA | SATB | SATDW | ACCSAT | IPL3[2] | SFA | RND | IF |
| bit 7 | | | | | | | bit 0 |

| Legend: | | C = Clearable bit | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **VAR:** Variable Exception Processing Latency Control bit
  1 = Variable exception processing is enabled
  0 = Fixed exception processing is enabled

bit 14 **Unimplemented:** Read as '0'

bit 13-12 **US<1:0>:** DSP Multiply Unsigned/Signed Control bits
  11 = Reserved
  10 = DSP engine multiplies are mixed-sign
  01 = DSP engine multiplies are unsigned
  00 = DSP engine multiplies are signed

bit 11 **EDT:** Early DO Loop Termination Control bit[1]
  1 = Terminates executing DO loop at the end of current loop iteration
  0 = No effect

bit 10-8 **DL<2:0>:** DO Loop Nesting Level Status bits
  111 = 7 DO loops are active
  •
  •
  •
  001 = 1 DO loop is active
  000 = 0 DO loops are active

bit 7 **SATA:** ACCA Saturation Enable bit
  1 = Accumulator A saturation is enabled
  0 = Accumulator A saturation is disabled

bit 6 **SATB:** ACCB Saturation Enable bit
  1 = Accumulator B saturation is enabled
  0 = Accumulator B saturation is disabled

bit 5 **SATDW:** Data Space Write from DSP Engine Saturation Enable bit
  1 = Data Space write saturation is enabled
  0 = Data Space write saturation is disabled

bit 4 **ACCSAT:** Accumulator Saturation Mode Select bit
  1 = 9.31 saturation (super saturation)
  0 = 1.31 saturation (normal saturation)

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3[2]
  1 = CPU Interrupt Priority Level is greater than 7
  0 = CPU Interrupt Priority Level is 7 or less

**Note 1:** This bit is always read as '0'.
  **2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.

**dSPIC33EPXXXGS70X/80X FAMILY**

**FIGURE 4-8:** **PAGED DATA MEMORY SPACE**



Program Space
(Instruction & Data)

Table Address Space
(TBLPAG<7:0>)

DS_Addr<15:0>

0x0000

(TBLPAG = 0x00)
lsw Using
TBLRDL/TBLWTL,
MSB Using
TBLRDH/TBLWTH

0xFFFF

Program Memory
(lsw – <15:0>)

0x00_0000

DS_Addr<14:0>

0x0000

(DSRPAG = 0x200)
No Writes Allowed

0x7FFF

PSV
Program
Memory
(lsw)

**Local Data Space**

DS_Addr<15:0>

0x7F_FFFF

0x0000

SFR Registers

0x0FFF
0x1000

0x0000

(DSRPAG = 0x2FF)
No Writes Allowed

0x7FFF

8-Kbyte
RAM

0x0000

0x7FFF
0x0000

(DSRPAG = 0x300)
No Writes Allowed

(TBLPAG = 0x7F)
lsw Using
TBLRDL/TBLWTL,
MSB Using
TBLRDH/TBLWTH

0x2FFF
0x3000
0x7FFF
0x8000

0x7FFF

0xFFFF

32-Kbyte
PSV Window

PSV
Program
Memory
(MSB)

Program Memory
(MSB – <23:16>)

0x00_0000

0xFFFF

0x0000

0x0000

(DSRPAG = 0x3FF)
No Writes Allowed

0x7FFF

0x7F_FFFF

**REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| | | | NVMADR<15:8> | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| | | | NVMADR<7:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits

Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

**REGISTER 5-3: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| | | | NVMADRU<23:16> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| T4 – Timer4 | 35 | 27 | 0x00004A | IFS1<11> T4IF | IEC1<11> T4IE | IPC6<14:12> T4IP<2:0> |
| T5 – Timer5 | 36 | 28 | 0x00004C | IFS1<12> T5IF | IEC1<12> T5IE | IPC7<2:0> T5IP<2:0> |
| INT2 – External Interrupt 2 | 37 | 29 | 0x00004E | IFS1<13> INT2IF | IEC1<13> INT2IE | IPC7<6:4> INT2IP<2:0> |
| U2RX – UART2 Receiver | 38 | 30 | 0x000050 | IFS1<14> U2RXIF | IEC1<14> U2RXIE | IPC7<10:8> U2RXIP<2:0> |
| U2TX – UART2 Transmitter | 39 | 31 | 0x000052 | IFS1<15> U2TXIF | IEC1<15> U2TXIE | IPC7<14:12> U2TXIP<2:0> |
| SPI2TX – SPI2 Transfer Done | 40 | 32 | 0x000054 | IFS2<0> SPI2TXIF | IEC2<0> SPI2TXIE | IPC8<2:0> SPI2TXIP<2:0> |
| SPI2RX – SPI2 Receive Done | 41 | 33 | 0x000056 | IFS2<1> SPI2RXIF | IEC2<1> SPI2RXIE | IPC8<6:4> SPI2RXIP<2:0> |
| C1RX – CAN1 RX Data Ready | 42 | 34 | 0x000058 | IFS2<2> C1RXIF | IEC2<2> C1RXIE | IPC8<10:8> C1RXIP<2:0> |
| C1 – CAN1 Combined Error | 43 | 35 | 0x000059 | IFS2<3> C1IF | IEC2<3> C1IE | IPC8<14:12> C1IP<2:0> |
| DMA3 – DMA Channel 3 | 44 | 36 | 0x00005A | IFS2<4> DMA3IF | IEC2<4> DMA3IE | IPC9<2:0> DMA3IP<2:0> |
| IC3 – Input Capture 3 | 45 | 37 | 0x00005E | IFS2<5> IC3IF | IEC2<5> IC3IE | IPC9<6:4> IC3IP<2:0> |
| IC4 – Input Capture 4 | 46 | 38 | 0x000060 | IFS2<6> IC4IF | IEC2<6> IC4IE | IPC9<10:8> IC4IP<2:0> |
| Reserved | 47-56 | 39-48 | 0x000062-0x000074 | — | — | — |
| SI2C2 – I2C2 Slave Event | 57 | 49 | 0x000076 | IFS3<1> SI2C2IF | IEC3<1> SI2C2IE | IPC12<6:4> SI2C2IP<2:0> |
| MI2C2 – I2C2 Master Event | 58 | 50 | 0x000078 | IFS3<2> MI2C2IF | IEC3<2> MI2C2IE | IPC12<10:8> MI2C2IP<2:0> |
| Reserved | 59-61 | 51-53 | 0x00007A-0x00007E | — | — | — |
| INT4 – External Interrupt 4 | 62 | 54 | 0x000080 | IFS3<6> INT4IF | IEC3<6> INT4IE | IPC13<10:8> INT4IP<2:0> |
| C2RX – CAN2 RX Data Ready | 63 | 55 | 0x000082 | IFS3<7> C2RXIF | IEC3<7> C2RXIE | IPC13<14:12> C2RXIP<2:0> |
| C2 – CAN 2 Combined Error | 64 | 56 | 0x000083 | IFS3<8> C2IF | IEC3<8> C2IE | IPC14<2:0> C2IP<2:0> |
| PSEM – PWM Special Event Match | 65 | 57 | 0x000086 | IFS3<9> PSEMIF | IEC3<9> PSEMIE | IPC14<6:4> PSEMIP<2:0> |
| Reserved | 66-72 | 58-64 | 0x000088-0x000094 | — | — | — |
| U1E – UART1 Error Interrupt | 73 | 65 | 0x000096 | IFS4<1> U1EIF | IEC4<1> U1EIE | IPC16<6:4> U1EIP<2:0> |
| U2E – UART2 Error Interrupt | 74 | 66 | 0x000098 | IFS4<2> U2EIF | IEC4<2> U2EIE | IPC16<10:8> U2EIP<2:0> |
| Reserved | 75-77 | 67-69 | 0x00009A-0x0000A2 | — | — | — |
| C1TX – CAN1 TX Data Request | 78 | 70 | 0x0000A0 | IFS4<6> C1TXIF | IEC4<6> C1TXIE | IPC17<10:8> C1TXIP<2:0> |
| C2TX – CAN2 TX Data Request | 79 | 71 | 0x0000A | IFS4<7> C2TXIF | IEC4<7> C2TXIE | IPC17<14:12> C2TXIP<2:0> |
| Reserved | 80 | 72 | 0x0000A4 | — | — | — |

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| AN17 Conversion Done | 168 | 160 | 0x000154 | IFS10<0> AN17IF | IEC10<0> AN17IE | IPC40<2:0> AN17IP<2:0> |
| AN18 Conversion Done | 169 | 161 | 0x000156 | IFS10<1> AN18IF | IEC10<1> AN18IE | IPC40<6:4> AN18IP<2:0> |
| AN19 Conversion Done | 170 | 162 | 0x000158 | IFS10<2> AN19IF | IEC10<2> AN19IE | IPC40<10:8> AN19IP<2:0> |
| AN20 Conversion Done | 171 | 163 | 0x00015A | IFS10<3> AN20IF | IEC10<3> AN20IE | IPC40<14:12> AN20IP<2:0> |
| AN21 Conversion Done | 172 | 164 | 0x00015C | IFS10<4> AN21IF | IEC10<4> AN21IE | IPC41<2:0> AN21IP<2:0> |
| Reserved | 173-180 | 165-172 | 0x00015C-0x00016C | — | — | — |
| I2C1 – I2C1 Bus Collision | 181 | 173 | 0x00016E | IFS10<13> I2C1IF | IEC10<13> I2C1IE | IPC43<6:4> I2C1IP<2:0> |
| I2C2 – I2C2 Bus Collision | 182 | 174 | 0x000170 | IFS10<14> I2C2IF | IEC10<14> I2C2IE | IPC43<10:8> I2C2IP<2:0> |
| Reserved | 183-184 | 175-176 | 0x000172-0x000174 | — | — | — |
| ADCMP0 – ADC Digital Comparator 0 | 185 | 177 | 0x000176 | IFS11<1> ADCMP0IF | IEC11<1> ADCMP0IE | IPC44<6:4> ADCMP0IP<2:0> |
| ADCMP1 – ADC Digital Comparator 1 | 186 | 178 | 0x000178 | IFS11<2> ADCMP1IF | IEC11<2> ADCMP1IE | IPC44<10:8> ADCMP1IP<2:0> |
| ADFLTR0 – ADC Filter 0 | 187 | 179 | 0x00017A | IFS11<3> ADFLTR0IF | IEC11<3> ADFLTR0IE | IPC44<14:12> ADFLTR0IP<2:0> |
| ADFLTR1 – ADC Filter 1 | 188 | 180 | 0x00017C | IFS11<4> ADFLTR1IF | IEC11<4> ADFLTR1IE | IPC45<2:0> ADFLTR1IP<2:0> |
| Reserved | 189-253 | 181-245 | 0x00017E-0x000192 | — | — | — |

**REGISTER 8-2:** **DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER**

| R/S-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| FORCE[(1)] | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| | S = Settable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **FORCE:** Force DMA Transfer bit[(1)]

1 = Forces a single DMA transfer (Manual mode)
0 = Automatic DMA transfer initiation by DMA request

bit 14-8 **Unimplemented:** Read as '0'

bit 7-0 **IRQSEL<7:0>:** DMA Peripheral IRQ Number Select bits

01000111 = CAN2 – TX data request
01000110 = CAN1 – TX data request
00110111 = CAN2 – RX data ready
00100110 = IC4 – Input Capture 4
00100101 = IC3 – Input Capture 3
00100010 = CAN1 – RX data ready
00011111 = UART2TX – UART2 transmitter
00011110 = UART2RX – UART2 receiver
00011100 = TMR5 – Timer5
00011011 = TMR4 – Timer4
00011010 = OC4 – Output Compare 4
00011001 = OC3 – Output Compare 3
00001100 = UART1TX – UART1 transmitter
00001011 = UART1RX – UART1 receiver
00001000 = TMR3 – Timer3
00000111 = TMR2 – Timer2
00000110 = OC2 – Output Compare 2
00000101 = IC2 – Input Capture 2
00000010 = OC1 – Output Compare 1
00000001 = IC1 – Input Capture 1
00000000 = INT0 – External Interrupt 0

**Note 1:** The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER (CONTINUED)**

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)

11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

**Note 1:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

**2:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**3:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 |
|-----|-----|-----|-----|-----|-----|-----|-------|
| — | — | — | — | — | — | — | PLLDIV8 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| PLLDIV<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | |
|---------|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared    x = Bit is unknown |

bit 15-9 **Unimplemented:** Read as '0'

bit 8-0 **PLLDIV<8:0>:** PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

111111111 = 513
•
•
•
000110000 = 50 (default)
•
•
•
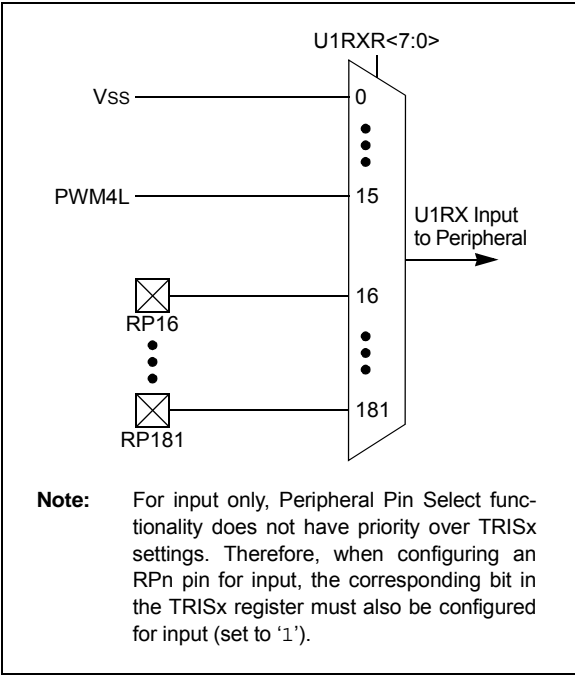000000010 = 4
000000001 = 3
000000000 = 2

## 11.6.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-9 through Register 11-32). Each register contains sets of 8-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 8-bit index value maps the RPn pin with the corresponding value, or internal signal, to that peripheral. See Table 11-11 for a list of available inputs.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

**FIGURE 11-2: REMAPPABLE INPUT FOR U1RX**



**Note:** For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

### 11.6.4.1 Virtual Connections

The dsPIC33EPXXXGS70X/80X devices support six virtual RPn pins (RP176-RP181), which are identical in functionality to all other RPn pins, with the exception of pinouts. These six pins are internal to the devices and are not connected to a physical device pin.

These pins provide a simple way for inter-peripheral connection without utilizing a physical pin. For example, the output of the analog comparator can be connected to RP176 and the PWM Fault input can be configured for RP176 as well. This configuration allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

**TABLE 11-11: REMAPPABLE SOURCES**

| Remap Index | Output Function |
|---|---|
| 0 | Vss |
| 1 | CMP1 |
| 2 | CMP2 |
| 3 | CMP3 |
| 4 | CMP4 |
| 5 | PWM4H |
| 6 | PTGO30 |
| 7 | PTGO31 |
| 8-11 | Reserved |
| 12 | REFO |
| 13 | SYNCO1 |
| 14 | SYNCO2 |
| 15 | PWM4L |
| 16-20 | RP16-RP20 |
| 21-31 | Reserved |
| 32-41 | RP32-RP41 |
| 42 | Reserved |
| 43-58 | RP43-RP58 |
| 59 | Reserved |
| 60-76 | RP60-RP76 |
| 77-175 | Reserved |
| 176-181 | RP176-RP181 |

**REGISTER 11-45: RPOR12: PERIPHERAL PIN SELECT OUTPUT REGISTER 12**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------|--------|--------|--------|--------|--------|--------|--------|
| — | RP53R6 | RP53R5 | RP53R4 | RP53R3 | RP53R2 | RP53R1 | RP53R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------|--------|--------|--------|--------|--------|--------|--------|
| — | RP52R6 | RP52R5 | RP52R4 | RP52R3 | RP52R2 | RP52R1 | RP52R0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **RP53R<6:0>:** Peripheral Output Function is Assigned to RP53 Output Pin bits
(see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **RP52R<6:0>:** Peripheral Output Function is Assigned to RP52 Output Pin bits
(see Table 11-13 for peripheral function numbers)


**REGISTER 11-46: RPOR13: PERIPHERAL PIN SELECT OUTPUT REGISTER 13**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------|--------|--------|--------|--------|--------|--------|--------|
| — | RP55R6 | RP55R5 | RP55R4 | RP55R3 | RP55R2 | RP55R1 | RP55R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|------|--------|--------|--------|--------|--------|--------|--------|
| — | RP54R6 | RP54R5 | RP54R4 | RP54R3 | RP54R2 | RP54R1 | RP54R0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **RP55R<6:0>:** Peripheral Output Function is Assigned to RP55 Output Pin bits
(see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **RP54R<6:0>:** Peripheral Output Function is Assigned to RP54 Output Pin bits
(see Table 11-13 for peripheral function numbers)

**REGISTER 11-51: RPOR18: PERIPHERAL PIN SELECT OUTPUT REGISTER 18**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP66R6 | RP66R5 | RP66R4 | RP66R3 | RP66R2 | RP66R1 | RP66R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP65R6 | RP65R5 | RP65R4 | RP65R3 | RP65R2 | RP65R1 | RP65R0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **RP66R<6:0>:** Peripheral Output Function is Assigned to RP66 Output Pin bits
(see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **RP65R<6:0>:** Peripheral Output Function is Assigned to RP65 Output Pin bits
(see Table 11-13 for peripheral function numbers)

**REGISTER 11-52: RPOR19: PERIPHERAL PIN SELECT OUTPUT REGISTER 19**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP68R6 | RP68R5 | RP68R4 | RP68R3 | RP68R2 | RP68R1 | RP68R0 |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | RP67R6 | RP67R5 | RP67R4 | RP67R3 | RP67R2 | RP67R1 | RP67R0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **RP68R<6:0>:** Peripheral Output Function is Assigned to RP68 Output Pin bits
(see Table 11-13 for peripheral function numbers)

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **RP67R<6:0>:** Peripheral Output Function is Assigned to RP67 Output Pin bits
(see Table 11-13 for peripheral function numbers)

**REGISTER 15-1:** **OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)**

bit 2-0      **OCM<2:0>:** Output Compare x Mode Select bits

111 = Center-Aligned PWM mode: Output is set high when OCxTMR = OCxR and set low when OCxTMR = OCxRS**(1)**

110 = Edge-Aligned PWM mode: Output is set high when OCxTMR = 0 and set low when OCxTMR = OCxR**(1)**

101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS

100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle

011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin

010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low

001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high

000 = Output compare channel is disabled

**Note 1:** OCxR and OCxRS are double-buffered in PWM mode only.

**REGISTER 17-2: PTGCON: PTG CONTROL REGISTER**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGCLK2 | PTGCLK1 | PTGCLK0 | PTGDIV4 | PTGDIV3 | PTGDIV2 | PTGDIV1 | PTGDIV0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| PTGPWD3 | PTGPWD2 | PTGPWD1 | PTGPWD0 | — | PTGWDT2 | PTGWDT1 | PTGWDT0 |
| bit 7 | | | | | | | bit 0 |

**Legend:**
R = Readable bit   W = Writable bit   U = Unimplemented bit, read as '0'
-n = Value at POR   '1' = Bit is set   '0' = Bit is cleared   x = Bit is unknown

bit 15-13 **PTGCLK<2:0>:** Select PTG Module Clock Source bits
111 = CLC2
110 = CLC1
101 = PTG module clock source will be T3CLK
100 = PTG module clock source will be T2CLK
011 = PTG module clock source will be T1CLK
010 = PTG module clock source will be $T_{AD}$
001 = PTG module clock source will be $F_{OSC}$
000 = PTG module clock source will be $F_P$

bit 12-8 **PTGDIV<4:0>:** PTG Module Clock Prescaler (divider) bits
11111 = Divide-by-32
11110 = Divide-by-31
•
•
•
00001 = Divide-by-2
00000 = Divide-by-1

bit 7-4 **PTGPWD<3:0>:** PTG Trigger Output Pulse-Width bits
1111 = All trigger outputs are 16 PTG clock cycles wide
1110 = All trigger outputs are 15 PTG clock cycles wide
•
•
•
0001 = All trigger outputs are 2 PTG clock cycles wide
0000 = All trigger outputs are 1 PTG clock cycle wide

bit 3 **Unimplemented:** Read as '0'

bit 2-0 **PTGWDT<2:0>:** Select PTG Watchdog Timer Time-out Count Value bits
111 = Watchdog Timer will time-out after 512 PTG clocks
110 = Watchdog Timer will time-out after 256 PTG clocks
101 = Watchdog Timer will time-out after 128 PTG clocks
100 = Watchdog Timer will time-out after 64 PTG clocks
011 = Watchdog Timer will time-out after 32 PTG clocks
010 = Watchdog Timer will time-out after 16 PTG clocks
001 = Watchdog Timer will time-out after 8 PTG clocks
000 = Watchdog Timer is disabled

## REGISTER 17-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER[1,2]

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| ADCTS4 | ADCTS3 | ADCTS2 | ADCTS1 | IC4TSS | IC3TSS | IC2TSS | IC1TSS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| OC4CS | OC3CS | OC2CS | OC1CS | OC4TSS | OC3TSS | OC2TSS | OC1TSS |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **ADCTS4:** Sample Trigger PTGO15 for ADCx bit

1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 14 **ADCTS3:** Sample Trigger PTGO14 for ADCx bit

1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 13 **ADCTS2:** Sample Trigger PTGO13 for ADCx bit

1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 12 **ADCTS1:** Sample Trigger PTGO12 for ADCx bit

1 = Generates trigger when the broadcast command is executed
0 = Does not generate trigger when the broadcast command is executed

bit 11 **IC4TSS:** Trigger/Synchronization Source for IC4 bit

1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 10 **IC3TSS:** Trigger/Synchronization Source for IC3 bit

1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 9 **IC2TSS:** Trigger/Synchronization Source for IC2 bit

1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 8 **IC1TSS:** Trigger/Synchronization Source for IC1 bit

1 = Generates trigger/synchronization when the broadcast command is executed
0 = Does not generate trigger/synchronization when the broadcast command is executed

bit 7 **OC4CS:** Clock Source for OC4 bit

1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 6 **OC3CS:** Clock Source for OC3 bit

1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

bit 5 **OC2CS:** Clock Source for OC2 bit

1 = Generates clock pulse when the broadcast command is executed
0 = Does not generate clock pulse when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

To set up the SPIx module for the Enhanced Buffer Master mode of operation:

1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the SSx pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

**FIGURE 18-2:** **SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)**
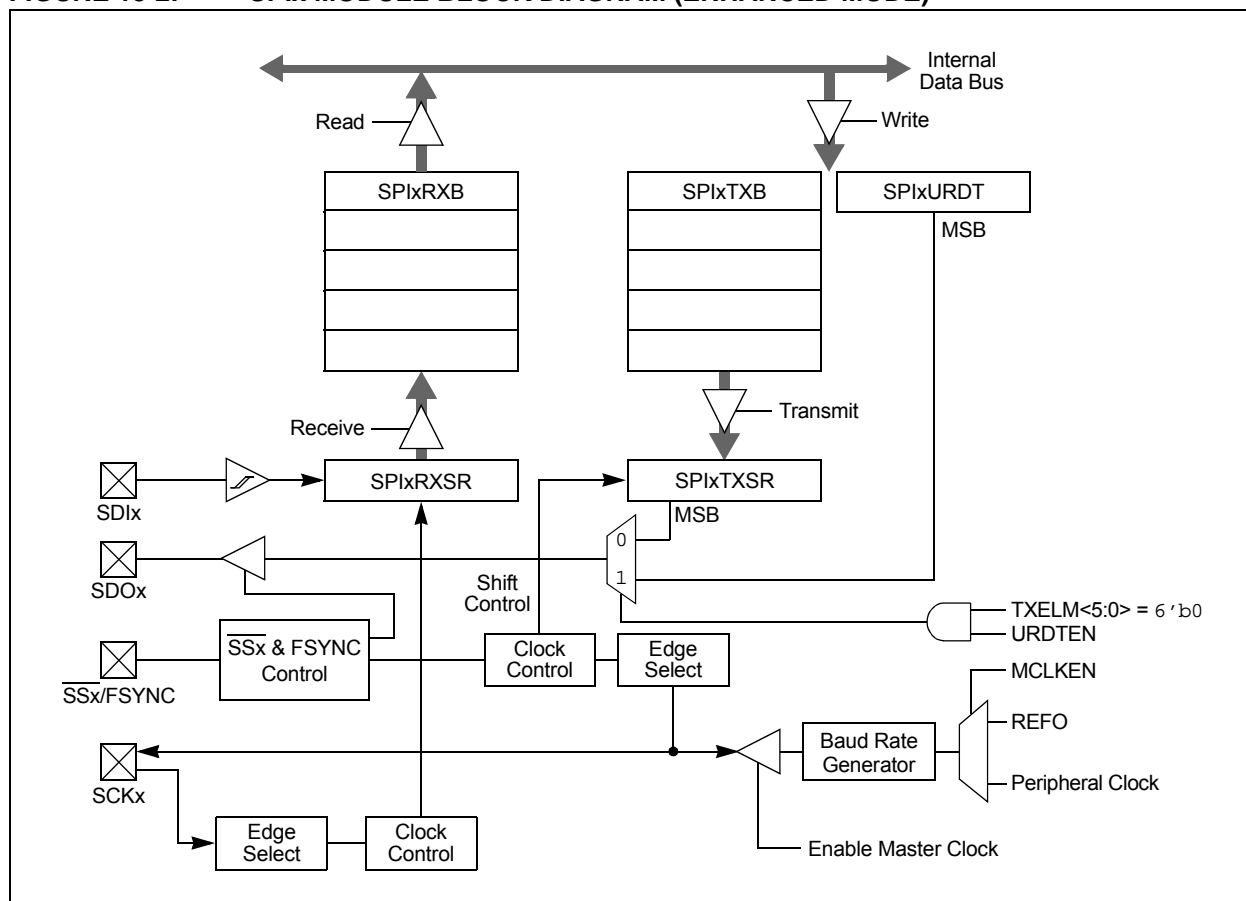
**REGISTER 22-2: ADCON1H: ADC CONTROL REGISTER 1 HIGH**

| r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 | r-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-1 | R/W-1 | r-0 | r-0 | r-0 | r-0 | r-0 |
|---|---|---|---|---|---|---|---|
| FORM | SHRRES1 | SHRRES0 | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

| Legend: | | r = Reserved bit | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-8      **Reserved:** Maintain as '0'

bit 7         **FORM:** Fractional Data Output Format bit

1 = Fractional
0 = Integer

bit 6-5       **SHRRES<1:0>:** Shared ADC Core Resolution Selection bits

11 = 12-bit resolution
10 = 10-bit resolution
01 = 8-bit resolution
00 = 6-bit resolution

bit 4-0       **Reserved:** Maintain as '0'

**REGISTER 23-11:   CxFEN1: CANx ACCEPTANCE FILTER ENABLE REGISTER 1**

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | FLTEN<15:8> | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| | | | FLTEN<7:0> | | | | |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-0    **FLTEN<15:0>:** Enable Filter n to Accept Messages bits
1 = Enables Filter n
0 = Disables Filter n


**REGISTER 23-12:   CxBUFPNT1: CANx FILTERS 0-3 BUFFER POINTER REGISTER 1**

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---------|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15-12    **F3BP<3:0>:** RX Buffer Mask for Filter 3 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8    **F2BP<3:0>:** RX Buffer Mask for Filter 2 bits (same values as bits 15-12)

bit 7-4    **F1BP<3:0>:** RX Buffer Mask for Filter 1 bits (same values as bits 15-12)

bit 3-0    **F0BP<3:0>:** RX Buffer Mask for Filter 0 bits (same values as bits 15-12)

## 24.6 Hysteresis

An additional feature of the module is hysteresis control. Hysteresis can be enabled or disabled and its amplitude can be controlled by the HYSSEL<1:0> bits in the CMPxCON register. Three different values are available: 15 mV, 30 mV and 45 mV. It is also possible to select the edge (rising or falling) to which hysteresis is to be applied.

Hysteresis control prevents the comparator output from continuously changing state because of small perturbations (noise) at the input (see Figure 24-2).

**FIGURE 24-2: HYSTERESIS CONTROL**
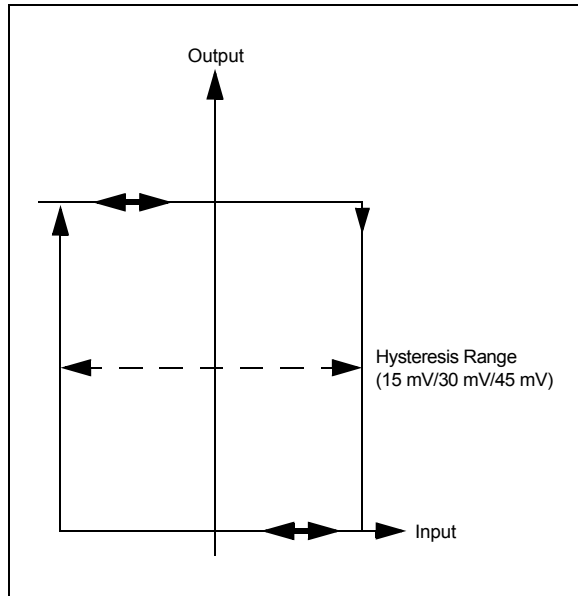


## 24.7 Analog Comparator Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

### 24.7.1 KEY RESOURCES

- **"High-Speed Analog Comparator Module"** (DS70005128) in the *"dsPIC33/PIC24 Family Reference Manual"*
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related *"dsPIC33/PIC24 Family Reference Manual"* Sections
- Development Tools

## 29.6 MPLAB X SIM Software Simulator

The MPLAB X SIM Software Simulator allows code development in a PC-hosted environment by simulating the PIC MCUs and dsPIC DSCs on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a comprehensive stimulus controller. Registers can be logged to files for further run-time analysis. The trace buffer and logic analyzer display extend the power of the simulator to record and track program execution, actions on I/O, most peripherals and internal registers.

The MPLAB X SIM Software Simulator fully supports symbolic debugging using the MPLAB XC Compilers, and the MPASM and MPLAB Assemblers. The software simulator offers the flexibility to develop and debug code outside of the hardware laboratory environment, making it an excellent, economical software development tool.

## 29.7 MPLAB REAL ICE In-Circuit Emulator System

The MPLAB REAL ICE In-Circuit Emulator System is Microchip's next generation high-speed emulator for Microchip Flash DSC and MCU devices. It debugs and programs all 8, 16 and 32-bit MCU, and DSC devices with the easy-to-use, powerful graphical user interface of the MPLAB X IDE.

The emulator is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with either a connector compatible with in-circuit debugger systems (RJ-11) or with the new high-speed, noise tolerant, Low-Voltage Differential Signal (LVDS) interconnection (CAT5).

The emulator is field upgradable through future firmware downloads in MPLAB X IDE. MPLAB REAL ICE offers significant advantages over competitive emulators including full-speed emulation, run-time variable watches, trace analysis, complex breakpoints, logic probes, a ruggedized probe interface and long (up to three meters) interconnection cables.

## 29.8 MPLAB ICD 3 In-Circuit Debugger System

The MPLAB ICD 3 In-Circuit Debugger System is Microchip's most cost-effective, high-speed hardware debugger/programmer for Microchip Flash DSC and MCU devices. It debugs and programs PIC Flash microcontrollers and dsPIC DSCs with the powerful, yet easy-to-use graphical user interface of the MPLAB IDE.

The MPLAB ICD 3 In-Circuit Debugger probe is connected to the design engineer's PC using a high-speed USB 2.0 interface and is connected to the target with a connector compatible with the MPLAB ICD 2 or MPLAB REAL ICE systems (RJ-11). MPLAB ICD 3 supports all MPLAB ICD 2 headers.

## 29.9 PICkit 3 In-Circuit Debugger/ Programmer

The MPLAB PICkit 3 allows debugging and programming of PIC and dsPIC Flash microcontrollers at a most affordable price point using the powerful graphical user interface of the MPLAB IDE. The MPLAB PICkit 3 is connected to the design engineer's PC using a full-speed USB interface and can be connected to the target via a Microchip debug (RJ-11) connector (compatible with MPLAB ICD 3 and MPLAB REAL ICE). The connector uses two device I/O pins and the Reset line to implement in-circuit debugging and In-Circuit Serial Programming™ (ICSP™).

## 29.10 MPLAB PM3 Device Programmer

The MPLAB PM3 Device Programmer is a universal, CE compliant device programmer with programmable voltage verification at $V_{DDMIN}$ and $V_{DDMAX}$ for maximum reliability. It features a large LCD display (128 x 64) for menus and error messages, and a modular, detachable socket assembly to support various package types. The ICSP cable assembly is included as a standard item. In Stand-Alone mode, the MPLAB PM3 Device Programmer can read, verify and program PIC devices without a PC connection. It can also set code protection in this mode. The MPLAB PM3 connects to the host PC via an RS-232 or USB cable. The MPLAB PM3 has high-speed communications and optimized algorithms for quick programming of large memory devices, and incorporates an MMC card for file storage and data applications.

**64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

SECTION A-A

X=A—B OR D

DETAIL 1
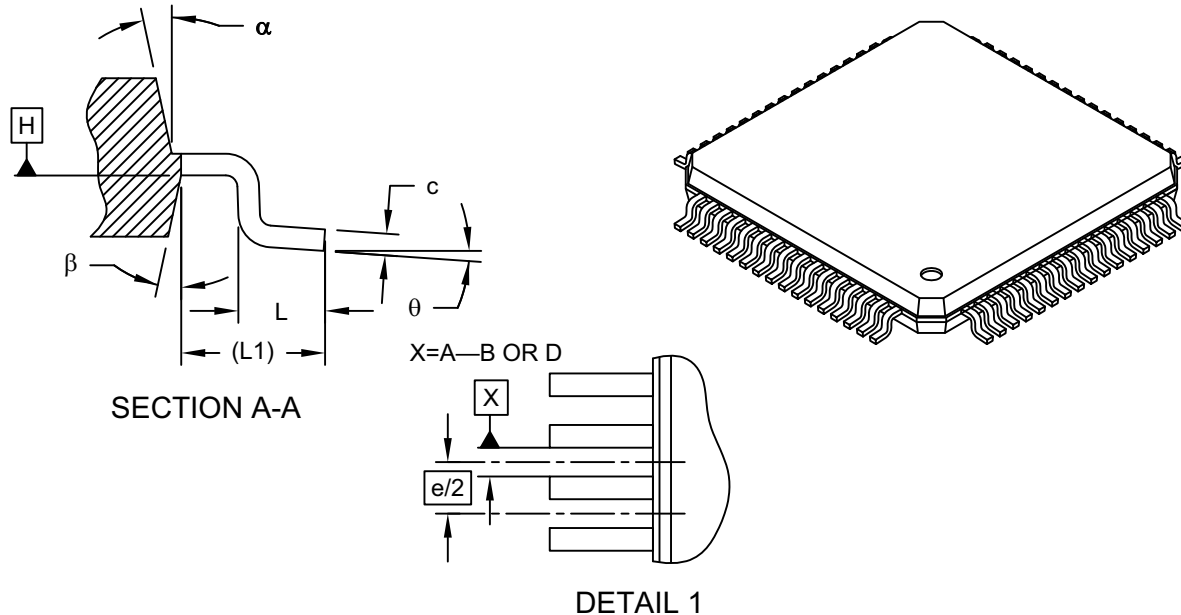
| | Units | | MILLIMETERS | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Leads | N | | 64 | |
| Lead Pitch | e | | 0.50 BSC | |
| Overall Height | A | - | - | 1.20 |
| Molded Package Thickness | A2 | 0.95 | 1.00 | 1.05 |
| Standoff | A1 | 0.05 | - | 0.15 |
| Foot Length | L | 0.45 | 0.60 | 0.75 |
| Footprint | L1 | | 1.00 REF | |
| Foot Angle | φ | 0° | 3.5° | 7° |
| Overall Width | E | | 12.00 BSC | |
| Overall Length | D | | 12.00 BSC | |
| Molded Package Width | E1 | | 10.00 BSC | |
| Molded Package Length | D1 | | 10.00 BSC | |
| Lead Thickness | c | 0.09 | - | 0.20 |
| Lead Width | b | 0.17 | 0.22 | 0.27 |
| Mold Draft Angle Top | α | 11° | 12° | 13° |
| Mold Draft Angle Bottom | β | 11° | 12° | 13° |

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing  C04-085C Sheet 2 of 2

**NOTES:**