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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	I ² C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs806-e-pt

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4.3 Data Address Space

The dsPIC33EPXXXGS70X/80X family CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory map is shown in Figure 4-6.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a base Data Space address range of 64 Kbytes or 32K words.

The lower half of the data memory space (i.e., when EA<15> = 0) is used for implemented memory addresses, while the upper half (EA<15> = 1) is reserved for the Program Space Visibility (PSV).

dsPIC33EPXXXGS70X/80X family devices implement up to 12 Kbytes of data memory. If an EA points to a location outside of this area, an all-zero word or byte is returned.

4.3.1 DATA SPACE WIDTH

The data memory space is organized in byteaddressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.3.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC[®] MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGS70X/80X family instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode, but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.3.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGS70X/80X family core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note: The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.3.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

REGISTER 8-2: DMAxREQ: DMA CHANNEL x IRQ SELECT REGISTER

R/S-0	U-0						
FORCE ⁽¹⁾	_	—	—	—	—	—	—
bit 15							bit 8

| R/W-0 |
|---------|---------|---------|---------|---------|---------|---------|---------|
| IRQSEL7 | IRQSEL6 | IRQSEL5 | IRQSEL4 | IRQSEL3 | IRQSEL2 | IRQSEL1 | IRQSEL0 |
| bit 7 | | | | | | | bit 0 |

Legend:	S = Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	1 as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	FORCE: Force DMA Transfer bit ⁽¹⁾
	1 = Forces a single DMA transfer (Manual mode)
	0 = Automatic DMA transfer initiation by DMA request
bit 14-8	Unimplemented: Read as '0'
bit 7-0	IRQSEL<7:0>: DMA Peripheral IRQ Number Select bits
	01000111 = CAN2 – TX data request
	01000110 = CAN1 – TX data request
	00110111 = CAN2 – RX data ready
	00100110 = IC4 – Input Capture 4
	00100101 = IC3 – Input Capture 3
	00100010 = CAN1 – RX data ready
	00011111 = UART2TX – UART2 transmitter
	00011110 = UART2RX – UART2 receiver
	00011100 = TMR5 – Timer5
	00011011 = TMR4 – Timer4
	00011010 = OC4 - Output Compare 4
	00011001 = OC3 – Output Compare 3
	00001100 = UART1TX – UART1 transmitter
	00001011 = UART1RX – UART1 receiver
	00001000 = TMR3 – Timer3
	00000111 = TMR2 – Timer2
	00000110 = OC2 - Output Compare 2
	00000101 = IC2 - Input Capture 2
	00000010 = OC1 - Output Compare 1
	0000001 = 101 - Input Capture 1
	00000000 = INIO - External Interrupt O

Note 1: The FORCE bit cannot be cleared by user software. The FORCE bit is cleared by hardware when the forced DMA transfer is complete or the channel is disabled (CHEN = 0).

REGISTER 11-53: RPOR20: PERIPHERAL PIN SELECT OUTPUT REGISTER 20

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
_	RP70R6	RP70R5	RP70R4	RP70R3	RP70R2	RP70R1	RP70R0	
bit 15	•					- -	bit 8	
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	RP69R6	RP69R5	RP69R4	RP69R3	RP69R2	RP69R1	RP69R0	
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is		'1' = Bit is set		'0' = Bit is cleared x		x = Bit is unknown		
bit 15	bit 15 Unimplemented: Read as '0'							

bit 14-8	RP70R<6:0>: Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-13 for peripheral function numbers)
bit 7	Unimplemented: Read as '0'
bit 6-0	RP69R<6:0>: Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 11-54: RPOR21: PERIPHERAL PIN SELECT OUTPUT REGISTER 21

U-0	R/W-0						
—	RP72R6	RP72R5	RP72R4	RP72R3	RP72R2	RP72R1	RP72R0
bit 15							bit 8
U-0	R/W-0						
—	RP71R6	RP71R5	RP71R4	RP71R3	RP71R2	RP71R1	RP71R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 Unimplemented: Read as '0'

bit 14-8	RP72R<6:0>: Peripheral Output Function is Assigned to RP72 Output Pin bits
	(see Table 11-13 for peripheral function numbers)

- bit 7 Unimplemented: Read as '0'
- bit 6-0 **RP71R<6:0>:** Peripheral Output Function is Assigned to RP71 Output Pin bits (see Table 11-13 for peripheral function numbers)

REGISTER 21-4: CLCxGLSL: CLCx GATE LOGIC INPUT SELECT LOW REGISTER (CONTINUED)

bit 3	G1D2T: Gate 1 Data Source 2 True Enable bit
	1 = Data Source 2 non-inverted signal is enabled for Gate 1
	0 = Data Source 2 non-inverted signal is disabled for Gate 1
bit 2	G1D2N: Gate 1 Data Source 2 Negated Enable bit
	 1 = Data Source 2 inverted signal is enabled for Gate 1 0 = Data Source 2 inverted signal is disabled for Gate 1
bit 1	G1D1T: Gate 1 Data Source 1 True Enable bit
	 1 = Data Source 1 non-inverted signal is enabled for Gate 1 0 = Data Source 1 non-inverted signal is disabled for Gate 1
bit 0	G1D1N: Gate 1 Data Source 1 Negated Enable bit
	1 = Data Source 1 inverted signal is enabled for Gate 1
	0 = Data Source 1 inverted signal is disabled for Gate 1

REGISTER 22-29: ADCAL0H: ADC CALIBRATION REGISTER 0 HIGH

R-0. HSC U-0 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 CAL3RDY ____ ____ ____ CAL3SKIP **CAL3DIFF** CAL3EN **CAL3RUN** bit 15 bit 8 R-0, HSC U-0 U-0 U-0 R/W-0 R/W-0 R/W-0 R/W-0 CAL2RDY CAL2SKIP CAL2DIFF CAL2EN CAL2RUN ____ ____ bit 7 bit 0 Legend: U = Unimplemented bit, read as '0' R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit -n = Value at POR x = Bit is unknown '1' = Bit is set '0' = Bit is cleared bit 15 CAL3RDY: Dedicated ADC Core 3 Calibration Status Flag bit 1 = Dedicated ADC Core 3 calibration is finished 0 = Dedicated ADC Core 3 calibration is in progress bit 14-12 Unimplemented: Read as '0' bit 11 CAL3SKIP: Dedicated ADC Core 3 Calibration Bypass bit 1 = After power-up, the dedicated ADC Core 3 will not be calibrated 0 = After power-up, the dedicated ADC Core 3 will be calibrated bit 10 CAL3DIFF: Dedicated ADC Core 3 Differential-Mode Calibration bit 1 = Dedicated ADC Core 3 will be calibrated in Differential Input mode 0 = Dedicated ADC Core 3 will be calibrated in Single-Ended Input mode bit 9 CAL3EN: Dedicated ADC Core 3 Calibration Enable bit 1 = Dedicated ADC Core 3 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software 0 = Dedicated ADC Core 3 calibration bits are disabled CAL3RUN: Dedicated ADC Core 3 Calibration Start bit bit 8 1 = If this bit is set by software, the dedicated ADC Core 3 calibration cycle is started; this bit is automatically cleared by hardware 0 = Software can start the next calibration cycle bit 7 CAL2RDY: Dedicated ADC Core 2 Calibration Status Flag bit 1 = Dedicated ADC Core 2 calibration is finished 0 = Dedicated ADC Core 2 calibration is in progress bit 6-4 Unimplemented: Read as '0' bit 3 CAL2SKIP: Dedicated ADC Core 2 Calibration Bypass bit 1 = After power-up, the dedicated ADC Core 2 will not be calibrated 0 = After power-up, the dedicated ADC Core 2 will be calibrated bit 2 CAL2DIFF: Dedicated ADC Core 2 Differential-Mode Calibration bit 1 = Dedicated ADC Core 2 will be calibrated in Differential Input mode 0 = Dedicated ADC Core 2 will be calibrated in Single-Ended Input mode bit 1 CAL2EN: Dedicated ADC Core 2 Calibration Enable bit 1 = Dedicated ADC Core 2 calibration bits (CALxRDY, CALxSKIP, CALxDIFF and CALxRUN) can be accessed by software 0 = Dedicated ADC Core 2 calibration bits are disabled CAL2RUN: Dedicated ADC Core 2 Calibration Start bit bit 0 1 = If this bit is set by software, the dedicated ADC Core 2 calibration cycle is started; this bit is automatically cleared by hardware 0 = Software can start the next calibration cycle

23.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EPXXXGS80X DEVICES ONLY)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGS70X/80X family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to "Enhanced Controller Area Network (ECAN™)" (DS70353) in the "dsPIC33/PIC24 Family Reference Manual", which is available from the Microchip web site (www.microchip.com).
 - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

23.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/ protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGS80X devices contain two CAN modules.

The CAN module is a communication controller, implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details. The CAN module features are as follows:

- Implementation of the CAN Protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0-8 Bytes of Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to 8 Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet[™] Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode supports Self-Test Operation
- Signaling via Interrupt Capabilities for All CAN Receiver and Transmitter Error States
- · Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

CAN Control Registers 23.3

bit 7

REGISTER 23-1: CxCTRL1: CANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15							bit 8
R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	_	CANCAP	_	_	WIN

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14	Unimplemented: Read as '0'
bit 13	CSIDL: CANx Stop in Idle Mode bit
	1 = Discontinues module operation when device enters Idle mode
	0 = Continues module operation in Idle mode
bit 12	ABAT: Abort All Pending Transmissions bit
	1 = Signals all transmit buffers to abort transmission
	0 = Module will clear this bit when all transmissions are aborted
bit 11	CANCKS: CANX Module Clock (FCAN) Source Select bit
	1 = FCAN is equal to 2 * FP
	U = FCAN is equal to FP
DIT 10-8	REQOP<2:0>: Request Operation Mode bits
	111 = Set Listen All Messages mode
	101 = Reserved
	100 = Set Configuration mode
	011 = Set Listen Only mode
	010 = Set Loopback mode
	0.01 = Set Disable mode
bit 7-5	OPMODE<2:0>: Operation Mode bits
	111 = Module is in Listen All Messages mode
	110 = Reserved
	101 = Reserved
	100 = Module is in Configuration mode
	011 = Module is in Listen Only mode $010 = Module is in Loopback mode$
	001 = Module is in Disable mode
	000 = Module is in Normal Operation mode
bit 4	Unimplemented: Read as '0'
bit 3	CANCAP: CANx Message Receive Timer Capture Event Enable bit
	1 = Enables input capture based on CAN message receive
	0 = Disables CAN capture
bit 2-1	Unimplemented: Read as '0'
bit 0	WIN: SFR Map Window Select bit
	1 = Uses filter window

bit 0

24.3 Module Applications

This module provides a means for the SMPS dsPIC[®] DSC devices to monitor voltage and currents in a power conversion application. The ability to detect transient conditions and stimulate the dsPIC DSC processor and/or peripherals, without requiring the processor and ADC to constantly monitor voltages or currents, frees the dsPIC DSC to perform other tasks.

The comparator module has a high-speed comparator and an associated 12-bit DAC that provides a programmable reference voltage to the inverting input of the comparator. The polarity of the comparator output is user-programmable. The output of the module can be used in the following modes:

- Generate an Interrupt
- Trigger an ADC Sample and Convert Process
- Truncate the PWMx Signal (current limit)
- Truncate the PWMx Period (current minimum)
- Disable the PWMx Outputs (Fault latch)

The output of the comparator module may be used in multiple modes at the same time, such as: 1) generate an interrupt, 2) have the ADC take a sample and convert it, and 3) truncate the PWMx output in response to a voltage being detected beyond its expected value.

The comparator module can also be used to wake-up the system from Sleep or Idle mode when the analog input voltage exceeds the programmed threshold voltage.

24.4 Digital-to-Analog Comparator (DAC)

Each analog comparator has a dedicated 12-bit DAC that is used to program the comparator threshold voltage via the CMPxDAC register. The DAC voltage reference source is selected using the EXTREF and RANGE bits in the CMPxCON register.

The EXTREF bit selects either the external voltage reference, EXTREFx, or an internal source as the voltage reference source. The EXTREFx input enables users to connect to a voltage reference that better suits their application. The RANGE bit enables AVDD as the voltage reference source for the DAC when an internal voltage reference is selected.

Note: EXTREF2 is not available on all devices.

Each DACx has an output enable bit, DACOE, in the CMPxCON register that enables the DACx reference voltage to be routed to an external output pin (DACOUTx). Refer to Figure 24-1 for connecting the DACx output voltage to the DACOUTx pins.

Note 1:	Ensure that multiple DACOE bits are not
	set in software. The output on the
	DACOUTx pin will be indeterminate if
	multiple comparators enable the DACx
	output.

2: DACOUT2 is not available on all devices.

24.5 Pulse Stretcher and Digital Logic

The analog comparator can respond to very fast transient signals. After the comparator output is given the desired polarity, the signal is passed to a pulse stretching circuit. The pulse stretching circuit has an asynchronous set function and a delay circuit that ensures the minimum pulse width is three system clock cycles wide to allow the attached circuitry to properly respond to a narrow pulse event.

The pulse stretcher circuit is followed by a digital filter. The digital filter is enabled via the FLTREN bit in the CMPxCON register. The digital filter operates with the clock specified via the FCLKSEL bit in the CMPxCON register. The comparator signal must be stable in a high or low state, for at least three of the selected clock cycles, for it to pass through the digital filter.

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
CMPON	_	CMPSIDL	HYSSEL1	HYSSEL0	FLTREN	FCLKSEL	DACOE		
bit 15			•	·			bit 8		
R/W-0	R/W-0	R/W-0	R/W-0	HC-0, HS	R/W-0	R/W-0	R/W-0		
INSEL1	INSEL0	EXTREF	HYSPOL	CMPSTAT	ALTINP	CMPPOL	RANGE		
bit 7							bit 0		
									
Legend:		HC = Hardware	e Clearable bit	HS = Hardwa	are Settable bit				
R = Readable	bit	W = Writable b	bit	U = Unimpler	nented bit, rea	d as '0'			
-n = Value at l	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown		
bit 15 CMPON: Comparator Operating Mode bit 1 = Comparator module is enabled 0 = Comparator module is disabled (reduces power consumption)									
bit 14	Unimplemer	nted: Read as 'o)'						
bit 13	CMPSIDL: C	Comparator Stop	in Idle Mode b	bit					
 1 = Discontinues module operation when device enters Idle mode. 0 = Continues module operation in Idle mode If a device has multiple comparators, any CMPSIDL bit set to '1' disables all comparators while in Idle mode 									
bit 12-11	HYSSEL<1:	0>: Comparator	Hysteresis Sel	lect bits					
	11 = 45 mV 10 = 30 mV 01 = 15 mV 00 = No hyst	hysteresis hysteresis hysteresis teresis is selecte	ed						
bit 10	FLTREN: Dig	gital Filter Enabl	e bit						
	1 = Digital fill 0 = Digital fill	ter is enabled ter is disabled							
bit 9	FCLKSEL:	Digital Filter and	Pulse Stretche	er Clock Select	bit				
	1 = Digital fill 0 = Digital fill	ter and pulse str ter and pulse str	etcher operate etcher operate	with the PWM with the syste	clock m clock				
bit 8	DACOE: DA	Cx Output Enab	le bit						
	1 = DACx an 0 = DACx an	alog voltage is o alog voltage is r	connected to the tothe t	ne DACOUTx p to the DACOU	_{bin} (1) Tx pin				
bit 7-6	INSEL<1:0>	: Input Source S	elect for Comp	parator bits					
	If ALTINP = 0 11 = Selects 10 = Selects 01 = Selects 00 = Selects If ALTINP = 1 11 = Reserve	0, Select from C CMPxD input p CMPxC input p CMPxB input pi CMPxA input pi 1, Select from A ed	omparator Inpu in in in in Iternate Inputs:	<u>uts:</u>					
	± 0 = Reserve 01 = Selects	ea PGA2 outout							
	00 = Selects	PGA1 output							

REGISTER 24-1: CMPxCON: COMPARATOR x CONTROL REGISTER

Note 1: DACOUTx can be associated only with a single comparator at any given time. The software must ensure that multiple comparators do not enable the DACx output by setting their respective DACOE bit.

27.2 Device Calibration and Identification

The PGAx and current source modules on the dsPIC33EPXXXGS70X/80X family devices require Calibration Data registers to improve performance of the module over a wide operating range. These Calibration registers are read-only and are stored in configuration memory space. Prior to enabling the module, the calibration data must be read (TBLPAG and Table Read instruction) and loaded into its respective SFR registers. The device calibration addresses are shown in Table 27-3.

The dsPIC33EPXXXGS70X/80X devices have two Identification registers near the end of configuration memory space that store the Device ID (DEVID) and Device Revision (DEVREV). These registers are used to determine the mask, variant and manufacturing information about the device. These registers are read-only and are shown in Register 27-1 and Register 27-2.

	TABLE 27-3:	DEVICE CALIBRATION ADDRESSES ⁽¹⁾
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Calibration Name	Address	Bits 23-16	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGA1CAL	800E48	_	_	_	_	—	_	_	_	_	_	_	PGA1 Calibration Data					
PGA2CAL	800E4C	_	_	-		-		-	-			-	PGA2 Calibration Data					
ISRCCAL	800E78	_	_	-		-		-	-			-	Current Source Calibration Data			ata		

Note 1: The calibration data must be copied into its respective SFR registers prior to enabling the module.

	-	-		· · ·			
Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽¹⁾	Status Flags Affected
55	NEG	NEG	Acc	Negate Accumulator	1	1	OA,OB,OAB, SA,SB,SAB
		NEG	f	$f = \overline{f} + 1$	1	1	C,DC,N,OV,Z
		NEG	f,WREG	WREG = \overline{f} + 1	1	1	C,DC,N,OV,Z
		NEG	Ws,Wd	$Wd = \overline{Ws} + 1$	1	1	C,DC,N,OV,Z
56	NOP	NOP		No Operation	1	1	None
		NOPR		No Operation	1	1	None
57	POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
		POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
		POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1)	1	2	None
		POP.S		Pop Shadow Registers	1	1	All
58	PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
		PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
		PUSH.D	Wns	Push W(ns):W(ns + 1) to Top-of-Stack (TOS)	1	2	None
		PUSH.S		Push Shadow Registers	1	1	None
59	PWRSAV	PWRSAV	#lit1	Go into Sleep or Idle mode	1	1	WDTO,Sleep
60	RCALL	RCALL	Expr	Relative Call	1	4	SFA
		RCALL	Wn	Computed Call	1	4	SFA
61	REPEAT	REPEAT	#lit15	Repeat Next Instruction lit15 + 1 times	1	1	None
		REPEAT	Wn	Repeat Next Instruction (Wn) + 1 times	1	1	None
62	RESET	RESET		Software device Reset	1	1	None
63	RETFIE	RETFIE		Return from interrupt	1	6 (5)	SFA
64	RETLW	RETLW	#lit10,Wn	Return with literal in Wn	1	6 (5)	SFA
65	RETURN	RETURN		Return from Subroutine	1	6 (5)	SFA
66	RLC	RLC	f	f = Rotate Left through Carry f	1	1	C,N,Z
		RLC	f,WREG	WREG = Rotate Left through Carry f	1	1	C,N,Z
		RLC	Ws,Wd	Wd = Rotate Left through Carry Ws	1	1	C,N,Z
67	RLNC	RLNC	f	f = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	f,WREG	WREG = Rotate Left (No Carry) f	1	1	N,Z
		RLNC	Ws,Wd	Wd = Rotate Left (No Carry) Ws	1	1	N,Z
68	RRC	RRC	f	f = Rotate Right through Carry f	1	1	C,N,Z
		RRC	f,WREG	WREG = Rotate Right through Carry f	1	1	C,N,Z
<u> </u>		RRC	Ws,Wd	Wd = Rotate Right through Carry Ws	1	1	C,N,Z
69	RRNC	RRNC	1 6	f = Rotate Right (No Carry) f	1	1	N,Z
		RRNC	I, WREG	WREG = Rotate Right (No Carry) f	1	1	N,Z
70	0.2.0	RRINC	WS,WQ	Store Accumulator	1	1	Nopo
70	SAC	SAC	Acc,#Slit4,Wdo	Store Accumulator	1	1	None
71	C.F.	SAC.R	Mg Wpd	Wnd = sign_extended Ws	1	1	
72	SETM	SETM	f	f = 0xFFFF	1	1	None
12	OF TH	SETM	± WREG	WREG = 0xFFFF	1	1	None
		SETM	Ws	Ws = 0xFFFF	1	1	None
73	SFTAC	SFTAC	Acc, Wn	Arithmetic Shift Accumulator by (Wn)	1	1	OA,OB,OAB,
		SFTAC	Acc,#Slit6	Arithmetic Shift Accumulator by Slit6	1	1	OA,OB,OAB, SA,SB,SAB

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

29.0 DEVELOPMENT SUPPORT

The PIC[®] microcontrollers (MCU) and dsPIC[®] digital signal controllers (DSC) are supported with a full range of software and hardware development tools:

- Integrated Development Environment
- MPLAB[®] X IDE Software
- Compilers/Assemblers/Linkers
 - MPLAB XC Compiler
 - MPASM[™] Assembler
 - MPLINK[™] Object Linker/ MPLIB[™] Object Librarian
 - MPLAB Assembler/Linker/Librarian for Various Device Families
- · Simulators
 - MPLAB X SIM Software Simulator
- · Emulators
 - MPLAB REAL ICE™ In-Circuit Emulator
- In-Circuit Debuggers/Programmers
 - MPLAB ICD 3
 - PICkit™ 3
- Device Programmers
 - MPLAB PM3 Device Programmer
- Low-Cost Demonstration/Development Boards, Evaluation Kits and Starter Kits
- Third-party development tools

29.1 MPLAB X Integrated Development Environment Software

The MPLAB X IDE is a single, unified graphical user interface for Microchip and third-party software, and hardware development tool that runs on Windows[®], Linux and Mac $OS^{®}$ X. Based on the NetBeans IDE, MPLAB X IDE is an entirely new IDE with a host of free software components and plug-ins for high-performance application development and debugging. Moving between tools and upgrading from software simulators to hardware debugging and programming tools is simple with the seamless user interface.

With complete project management, visual call graphs, a configurable watch window and a feature-rich editor that includes code completion and context menus, MPLAB X IDE is flexible and friendly enough for new users. With the ability to support multiple tools on multiple projects with simultaneous debugging, MPLAB X IDE is also suitable for the needs of experienced users.

Feature-Rich Editor:

- Color syntax highlighting
- Smart code completion makes suggestions and provides hints as you type
- Automatic code formatting based on user-defined rules
- · Live parsing

User-Friendly, Customizable Interface:

- Fully customizable interface: toolbars, toolbar buttons, windows, window placement, etc.
- · Call graph window
- Project-Based Workspaces:
- Multiple projects
- Multiple tools
- Multiple configurations
- · Simultaneous debugging sessions

File History and Bug Tracking:

- · Local file history feature
- Built-in support for Bugzilla issue tracker

				,				
АС СН	ARACTERIS	STICS		Standard Ope (unless other Operating tem	erating C wise sta perature	Conditions: 3.0 ited) $-40^{\circ}C \le TA \le$ $-40^{\circ}C \le TA \le$	W to 3.6 +85°C f +125°C	V or Industrial for Extended
Param No.	Symbol	Charao	cteristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
TB10	TtxH	TxCK High Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256)
TB11	TtxL	TxCK Low Time	Synchronous mode	Greater of: 20 or (Tcy + 20)/N	_	_	ns	Must also meet Parameter TB15, N = Prescale Value (1, 8, 64, 256)
TB15	TtxP	TxCK Input Period	Synchronous mode	Greater of: 40 or (2 Tcy + 40)/N	_	—	ns	N = Prescale Value (1, 8, 64, 256)
TB20	TCKEXTMRL	Delay from Clock Edge Increment	External TxCK to Timer	0.75 Tcy + 40		1.75 Tcy + 40	ns	

TABLE 30-25: TIMER2 AND TIMER4 (TYPE B TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

Note 1: These parameters are characterized but not tested in manufacturing.

TABLE 30-26: TIMER3 AND TIMER5 (TYPE C TIMER) EXTERNAL CLOCK TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Ope (unless other Operating tem	erating (wise sta perature	Conditions: 3.0 ated) $e -40^{\circ}C \le TA \le -40^{\circ}C \le -40^$	0V to 3. 0 ≤ +85°C ≤ +125°0	6V for Industrial C for Extended
Param No.	Symbol	Charac	teristic ⁽¹⁾	Min.	Тур.	Max.	Units	Conditions
TC10	TtxH	TxCK High Time	Synchronous	Tcy + 20	_	—	ns	Must also meet Parameter TC15
TC11	TtxL	TxCK Low Synchronous Time		Tcy + 20	—	—	ns	Must also meet Parameter TC15
TC15	TtxP	TxCK Input Period	Synchronous with Prescaler	2 Tcy + 40	—	—	ns	N = Prescale Value (1, 8, 64, 256)
TC20	TCKEXTMRL	Delay from External TxCK Clock Edge to Timer Increment		0.75 Tcy + 40		1.75 Tcy + 40	ns	

Note 1: These parameters are characterized but not tested in manufacturing.





TABLE 30-37:SPI1, SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 1, SMP = 0)TIMING REQUIREMENTS⁽⁵⁾

			Standard Op	perating	Conditi	ons: 3.0	V to 3.6V		
		TICS	(unless otherwise stated)						
			Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
	-		-40°C \leq TA \leq +125°C for Extended						
Param.	Symbol	Characteristic ⁽¹⁾	Min. Typ. ⁽²⁾ Ma		Max.	Units	Conditions		
SP70	FscP	Maximum SCKx Input Frequency		—	15	MHz	(Note 3)		
SP72	TscF	SCKx Input Fall Time				ns	See Parameter DO32 (Note 4)		
SP73	TscR	SCKx Input Rise Time	_	_		ns	See Parameter DO31 (Note 4		
SP30	TdoF	SDOx Data Output Fall Time	—			ns	See Parameter DO32 (Note 4)		
SP31	TdoR	SDOx Data Output Rise Time				ns	See Parameter DO31 (Note 4)		
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	_	6	20	ns			
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_		ns			
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	_	_	ns			
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	_		ns			
SP50	TssL2scH, TssL2scL	SSx ↓ to SCKx ↑ or SCKx ↓ Input	120			ns			
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	(Note 4)		
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 TCY + 40	_	—	ns	(Note 4)		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

5: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

TABLE 30-44:SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0)TIMING REQUIREMENTS⁽⁵⁾

			Standard Op	perating	Conditi	ons: 3.0	V to 3.6V		
	RACTERIS	TICS	(unless otherwise stated)						
			Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for Industrial						
					-40°	$C \le TA \le$	+125°C for Extended		
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Тур. ⁽²⁾	Max.	Units	Conditions		
SP70	FscP	Maximum SCK3 Input Frequency	—	—	25	MHz	(Note 3)		
SP72	TscF	SCK3 Input Fall Time	—			ns	See Parameter DO32 (Note 4)		
SP73	TscR	SCK3 Input Rise Time	—			ns	See Parameter DO31 (Note 4)		
SP30	TdoF	SDO3 Data Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)		
SP31	TdoR	SDO3 Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)		
SP35	TscH2doV, TscL2doV	SDO3 Data Output Valid after SCK3 Edge	—	6	20	ns			
SP36	TdoV2scH, TdoV2scL	SDO3 Data Output Setup to First SCK3 Edge	20	_	-	ns			
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI3 Data Input to SCK3 Edge	20	_	-	ns			
SP41	TscH2diL, TscL2diL	Hold Time of SDI3 Data Input to SCK3 Edge	15	_		ns			
SP50	TssL2scH, TssL2scL	SS3 ↓ to SCK3 ↑ or SCK3 ↓ Input	120			ns			
SP51	TssH2doZ	SS3 ↑ to SDO3 Output High-Impedance	10	_	50	ns	(Note 4)		
SP52	TscH2ssH, TscL2ssH	SS3 ↑ after SCK3 Edge	1.5 TCY + 40	—	—	ns	(Note 4)		
SP60	TssL2doV	SDO3 Data Output Valid after SS3 Edge	—	—	50	ns			

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK3 is 91 ns. Therefore, the SCK3 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI3 pins.

5: For dsPIC33EPXXXGSX06 and dsPIC33EPXXXGSX08 devices with a fixed SCK3 pin.

32.1 Package Marking Information (Continued)

44-Lead QFN (8x8 mm)



48-Lead TQFP (7x7x1.0 mm)



64-Lead TQFP (10x10x1 mm)



80-Lead TQFP (12x12x1 mm)





Example



Example



Example



28-Lead Ultra Thin Plastic Quad Flat, No Lead Package (2N) - 6x6x0.55 mm Body [UQFN] With 4.65x4.65 mm Exposed Pad and Corner Anchors

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	l Inite	Ν		\$		
	011103					
Dimension	Limits	MIN	NOM	MAX		
Number of Terminals	Ν		28			
Pitch	е		0.65 BSC			
Overall Height	Α	0.45	0.50	0.55		
Standoff	A1	0.00	0.02	0.05		
Terminal Thickness	A3	0.127 REF				
Overall Width	E	6.00 BSC				
Exposed Pad Width	E2	4.55	4.65	4.75		
Overall Length	D	6.00 BSC				
Exposed Pad Length	D2	4.55 4.65 4.75				
Exposed Pad Corner Chamfer	Р	-	0.35	-		
Terminal Width	b	0.25	0.30	0.35		
Corner Anchor Pad	b1	0.35	0.40	0.43		
Corner Pad, Metal Free Zone	b2	0.15	0.20	0.25		
Terminal Length	L	0.30	0.40	0.50		
Terminal-to-Exposed-Pad	K	0.20	-	-		

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated

3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances. REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-385B Sheet 2 of 2

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]





RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	X2			6.60
Optional Center Pad Length	Y2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Contact Pad to Contact Pad (X40)	G1	0.30		
Contact Pad to Center Pad (X44)	G2	0.28		
Thermal Via Diameter	V		0.33	
Thermal Via Pitch	EV		1.20	

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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