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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	67
Program Memory Size	64KB (64K × 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 22x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-TQFP
Supplier Device Package	80-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep64gs808t-i-pt

Email: info@E-XFL.COM

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4.6.3 MOVE AND ACCUMULATOR INSTRUCTIONS

Move instructions, and the DSP accumulator class of instructions, provide a greater degree of addressing flexibility than other instructions. In addition to the addressing modes supported by most MCU instructions, move and accumulator instructions also support Register Indirect with Register Offset Addressing mode, also referred to as Register Indexed mode.

Note: For the MOV instructions, the addressing mode specified in the instruction can differ for the source and destination EA. However, the 4-bit Wb (Register Offset) field is shared by both source and destination (but typically only used by one).

In summary, the following addressing modes are supported by move and accumulator instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-modified
- Register Indirect Pre-modified
- Register Indirect with Register Offset (Indexed)
- Register Indirect with Literal Offset
- 8-Bit Literal
- 16-Bit Literal
 - Note: Not all instructions support all the addressing modes given above. Individual instructions may support different subsets of these addressing modes.

4.6.4 MAC INSTRUCTIONS

The dual source operand DSP instructions (CLR, ED, EDAC, MAC, MPY, MPY. N, MOVSAC and MSC), also referred to as MAC instructions, use a simplified set of addressing modes to allow the user application to effectively manipulate the Data Pointers through register indirect tables.

The two-source operand prefetch registers must be members of the set {W8, W9, W10, W11}. For data reads, W8 and W9 are always directed to the X RAGU, and W10 and W11 are always directed to the Y AGU. The Effective Addresses generated (before and after modification) must therefore, be valid addresses within X Data Space for W8 and W9, and Y Data Space for W10 and W11.

Note: Register Indirect with Register Offset Addressing mode is available only for W9 (in X space) and W11 (in Y space).

In summary, the following addressing modes are supported by the MAC class of instructions:

- Register Indirect
- Register Indirect Post-Modified by 2
- Register Indirect Post-Modified by 4
- Register Indirect Post-Modified by 6
- Register Indirect with Register Offset (Indexed)

4.6.5 OTHER INSTRUCTIONS

Besides the addressing modes outlined previously, some instructions use literal constants of various sizes. For example, BRA (branch) instructions use 16-bit signed literals to specify the branch destination directly, whereas the DISI instruction uses a 14-bit unsigned literal field. In some instructions, such as ULNK, the source of an operand or result is implied by the opcode itself. Certain operations, such as a NOP, do not have any operands.

REGISTER 5-2: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMA	DR<7:0>			
bit 7							bit 0
Legend:							
R = Readable I	bit	W = Writable I	bit	U = Unimpler	mented bit, rea	d as '0'	
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits Selects the lower 16 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	_	—	_	—	_	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			NVMADR	U<23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 NVMADRU<23:16>: Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in Program Flash Memory. This register may be read or written to by the user application.

6.1 Reset Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

6.1.1 KEY RESOURCES

- "Reset" (DS70602) in the "dsPIC33/PIC24 Family Reference Manual"
- · Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
	—	—	_		—	—	—
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB<	23:16>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 Unimplemented: Read as '0'

bit 7-0 STB<23:16>: DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STB	<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STE	3<7:0>			
bit 7							bit 0
Legend:							
R = Readable b	pit	W = Writable b	oit	U = Unimplemented bit, read as '0'			
-n = Value at P	OR	'1' = Bit is set		'0' = Bit is cleared x = Bit is unknown			

bit 15-0 STB<15:0>: DMA Secondary Start Address bits (source or destination)

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER⁽¹⁾ (CONTINUED)

- bit 4 Unimplemented: Read as '0'
- bit 3 CF: Clock Fail Detect bit⁽³⁾
 - 1 = FSCM has detected a clock failure
 - 0 = FSCM has not detected a clock failure
- bit 2-1 Unimplemented: Read as '0'
- bit 0 OSWEN: Oscillator Switch Enable bit
 - 1 = Requests oscillator switch to the selection specified by the NOSC<2:0> bits
 - 0 = Oscillator switch is complete
- **Note 1:** Writes to this register require an unlock sequence.
 - 2: Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
 - **3:** This bit should only be cleared in software. Setting the bit in software (= 1) will have the same effect as an actual oscillator failure and will trigger an oscillator failure trap.

REGISTER 16-3: PTPER: PWMx PRIMARY MASTER TIME BASE PERIOD REGISTER^(1,2)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPE	R<15:8>			
bit 15							bit 8
R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
			PTPI	ER<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable	bit	U = Unimplei	mented bit, rea	ad as '0'	
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is un			x = Bit is unki	nown			

bit 15-0 **PTPER<15:0>:** Primary Master Time Base (PMTMR) Period Value bits

Note 1: The PWMx time base has a minimum value of 0x0010 and a maximum value of 0xFFF8.

2: Any period value that is less than 0x0028 must have the Least Significant 3 bits set to '0', thus yielding a period resolution at 8.32 ns (at fastest auxiliary clock rate).

REGISTER 16-4: SEVTCMP: PWMx SPECIAL EVENT COMPARE REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			SEVTCM	P<12:5>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
	S	SEVTCMP<4:0	>		—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-3 SEVTCMP<12:0>: Special Event Compare Count Value bits

bit 2-0 Unimplemented: Read as '0'

Note 1: One LSB = 1.04 ns (at fastest auxiliary clock rate); therefore, the minimum SEVTCMP resolution is 8.32 ns.

REGISTER 16-15: PHASEX: PWMx PRIMARY PHASE-SHIFT REGISTER (x = 1 to 8)^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	Ex<15:8>			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			PHAS	SEx<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable bit		U = Unimplen	nented bit, read	d as '0'	

-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 PHASEx<15:0>: PWMx Phase-Shift Value or Independent Time Base Period for the PWMx Generator bits

- **Note 1:** If PWMCONx<9> = 0, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs
 - True Independent Output mode (IOCONx<11:10> = 11); PHASEx<15:0> = Phase-shift value for PWMxH only
 - When the PHASEx/SPHASEx registers provide the phase shift with respect to the master time base; therefore, the valid range is 0x0000 through period
 - **2:** If PWMCONx<9> = 1, the following applies based on the mode of operation:
 - Complementary, Redundant and Push-Pull Output mode (IOCONx<11:10> = 00, 01 or 10); PHASEx<15:0> = Independent time base period value for PWMxH and PWMxL
 - True Independent Output mode (IOCONx<11:10> = 11); PHASEx<15:0> = Independent time base period value for PWMxH only
 - When the PHASEx/SPHASEx registers provide the local period, the valid range is 0x0000-0xFFF8

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REGISTER 17-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
—	—	—	—	—	—	—	—	
bit 15							bit 8	
U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
—	—	—			PTGQPTR<4:	0>		
bit 7							bit 0	
Legend:								
R = Readable bit W = Writable bit			bit	U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is set				'0' = Bit is cleared x = Bit is unknown				

bit 15-5 Unimplemented: Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits This register points to the currently active Step command in the Step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 17-13: PTGQUEX: PTG STEP QUEUE REGISTER x (x = 0-15)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
			STEP(2x +	· 1)<7:0> (2)			
bit 15							bit 8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0> ⁽²⁾							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read	as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8STEP(2x + 1)<7:0>: PTG Step Queue Pointer Register bits⁽²⁾
A queue location for storage of the STEP(2x +1) command byte.bit 7-0STEP(2x)<7:0>: PTG Step Queue Pointer Register bits⁽²⁾

A queue location for storage of the STEP(2x) command byte.

- **Note 1:** This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).
 - 2: Refer to Table 17-1 for the Step command encoding.
 - 3: The Step registers maintain their values on any type of Reset.

							D A 1100
U-0	U-0	U-0	R/C-0, HS	R-0, HSC	U-0	U-0	R-0, HSC
			FRMERR	SPIBUSY			SPITUR
bit 15							bit 8
R-0, HSC	C R/C-0, HS	R-1, HSC	U-0	R-1, HSC	U-0	R-0, HSC	R-0, HSC
SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF
bit 7							bit 0
			1.14			·0'	
Legend:	-1		DIT		iented, read as		
R = Readat			DIT	HSC = Hardw	are Settable/Cl	earable bit	0
-n = Value a	at POR	'1' = Bit is set		"0" = Bit is clea	ared	HS = Hardwar	e Settable bit
bit 15 12	Unimplomon	tod. Dood oo '	o'				
bit 12		Neau as the Error	Status hit				
	1 = Frame er	ror is detected	Status bit				
	0 = No frame	error is detected	ed				
bit 11	SPIBUSY: SF	Plx Activity Stat	us bit				
	1 = Module is	currently busy	with some trai	nsactions			
	0 = No ongoir	ng transactions	(at time of rea	d)			
bit 10-9	Unimplemen	ted: Read as '	0'				
bit 8	SPITUR: SPI	x Transmit Und	lerrun Status b	it(1)			
	1 = Transmit	buffer has enco	ountered a Trai	nsmit Underrun	condition		
		buffer does not	have a Transr	nit Underrun co	ondition		
bit /	SRMI: Shift F	Register Empty	Status bit				1 - 1 - 1 · · · · · · · · · ·
	\perp = No current o	r pending trans	ansactions (i.e.	, neither SPIX I	XB OF SPIXTX	SR contains da	ta to transmit)
bit 6	SPIROV: SPI	x Receive Ove	rflow Status bit				
bit 0	1 = A new by	te/half-word/wo	ord has been co	ompletelv recei	ved when the	SPIxRXB was fi	ull
	0 = No overflo	OW					
bit 5	SPIRBE: SPI	x RX Buffer En	npty Status bit				
	1 = RX buffer	is empty					
	0 = RX buffer	is not empty					
	Standard Buff	f <u>er mode:</u> sot in bardwar	o when SPIvPI	IE is road from	roading SPIv	DVR Automatic	ally cleared in
	hardware whe	en SPIx transfe	rs data from S	PIXRXSR to SF	PlxRXB.	RAD. Automatic	
	Enhanced Bu	iffer mode:					
	Indicates RXI	ELM<5:0> = 00	0000.				
bit 4	Unimplemen	ted: Read as '	0'				
Note 1.	SPITLIR is cleare	d when SPIEN	= 0 When IG		ITI IR nrovides	dynamic status	of the

Note 1: SPITUR is cleared when SPIEN = 0. When IGNTUR = 1, SPITUR provides dynamic status of the Transmit Underrun condition, but does not stop RX/TX operation and does not need to be cleared by software.

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R-0, HSC R-0. HSC R-0. HSC R-0. HSC R/C-0. HS U-0 U-0 R-0. HSC ACKSTAT ACKTIM ADD10 TRSTAT BCL GCSTAT bit 15 bit 8 R/C-0, HS R/C-0, HS R/C-0, HSC R/C-0, HSC R-0, HSC R-0, HSC R-0, HSC R-0, HSC Ρ IWCOL I2COV DΑ S RW RBF TBF bit 7 bit 0 Legend: C = Clearable bit '0' = Bit is cleared HS = Hardware Settable bit R = Readable bit W = Writable bit HSC = Hardware Settable/Clearable bit -n = Value at POR '1' = Bit is set U = Unimplemented bit, read as '0' ACKSTAT: Acknowledge Status bit (when operating as I²C master, applicable to master transmit operation) bit 15 1 = NACK was received from slave 0 = ACK was received from slave Hardware is set or clear at the end of a slave Acknowledge. **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation) bit 14 1 = Master transmit is in progress (8 bits + ACK) 0 = Master transmit is not in progress Hardware is set at the beginning of master transmission. Hardware is clear at the end of slave Acknowledge. bit 13 **ACKTIM:** Acknowledge Time Status bit (I²C Slave mode only) $1 = I^2C$ bus is an Acknowledge sequence, set on the 8th falling edge of SCLx 0 = Not an Acknowledge sequence, cleared on the 9th rising edge of SCLx bit 12-11 Unimplemented: Read as '0' bit 10 BCL: Master Bus Collision Detect bit 1 = A bus collision has been detected during a master operation 0 = No bus collision detected Hardware is set at detection of a bus collision. bit 9 GCSTAT: General Call Status bit 1 = General call address was received 0 = General call address was not received Hardware is set when address matches the general call address. Hardware is clear at Stop detection. bit 8 ADD10: 10-Bit Address Status bit 1 = 10-bit address was matched 0 = 10-bit address was not matched Hardware is set at the match of the 2nd byte of the matched 10-bit address. Hardware is clear at Stop detection. bit 7 IWCOL: I2Cx Write Collision Detect bit 1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy $0 = No \ collision$ Hardware is set at the occurrence of a write to I2CxTRN while busy (cleared by software). I2COV: I2Cx Receive Overflow Flag bit bit 6 1 = A byte was received while the I2CxRCV register was still holding the previous byte 0 = No overflowHardware is set at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software). D_A: Data/Address bit (I²C Slave mode only) bit 5 1 = Indicates that the last byte received was data 0 = Indicates that the last byte received was a device address Hardware is clear at a device address match. Hardware is set by reception of a slave byte.

20.1 UART Helpful Tips

- In multi-node, direct connect UART networks, UART receive inputs react to the complementary logic level defined by the URXINV bit (UxMODE<4>), which defines the Idle state, the default of which is logic high (i.e., URXINV = 0). Because remote devices do not initialize at the same time, it is likely that one of the devices, because the RX line is floating, will trigger a Start bit detection and will cause the first byte received, after the device has been initialized, to be invalid. To avoid this situation, the user should use a pullup or pull-down resistor on the RX pin depending on the value of the URXINV bit.
 - a) If URXINV = 0, use a pull-up resistor on the UxRX pin.
 - b) If URXINV = 1, use a pull-down resistor on the UxRX pin.
- 2. The first character received on a wake-up from Sleep mode, caused by activity on the UxRX pin of the UARTx module, will be invalid. In Sleep mode, peripheral clocks are disabled. By the time the oscillator system has restarted and stabilized from Sleep mode, the baud rate bit sampling clock, relative to the incoming UxRX bit timing, is no longer synchronized, resulting in the first character being invalid; this is to be expected.

20.2 UART Resources

Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page contains the latest updates and additional information.

20.2.1 KEY RESOURCES

- "Universal Asynchronous Receiver Transmitter (UART)" (DS70000582) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- Application Notes
- · Software Libraries
- · Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 22-4: ADCON2H: ADC CONTROL REGISTER 2 HIGH

R-0, HSC	R-0, HSC	r-0	r-0	r-0	r-0	R/W-0	R/W-0
REFRDY	REFERR	—	—	—	—	SHRSAMC9	SHRSAMC8
bit 15				•			bit 8

| R/W-0 |
|----------|----------|----------|----------|----------|----------|----------|----------|
| SHRSAMC7 | SHRSAMC6 | SHRSAMC5 | SHRSAMC4 | SHRSAMC3 | SHRSAMC2 | SHRSAMC1 | SHRSAMC0 |
| bit 7 | | | | | | | bit 0 |

Legend:	r = Reserved bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15	REFRDY: Band Gap and Reference Voltage Ready Flag bit					
	1 = Band gap is ready					
	0 = Band gap is not ready					
bit 14	REFERR: Band Gap or Reference Voltage Error Flag bit					
	 1 = Band gap was removed after the ADC module was enabled (ADON = 1) 0 = No band gap error was detected 					
bit 13-10	Reserved: Maintain as '0'					
bit 9-0	SHRSAMC<9:0>: Shared ADC Core Sample Time Selection bits					
	These bits specify the number of shared ADC Core Clock Periods (TADCORE) for the shared ADC core sample time.					
	111111111 = 1025 TADCORE					
	•					
	•					
	•					
	000000001 = 3 TADCORE					
	00000000 = 2 TADCORE					

25.2 PGA Resources

Many useful resources are provided on the main product page of the Microchip website for the devices listed in this data sheet. This product page contains the latest updates and additional information.

25.2.1 KEY RESOURCES

- "Programmable Gain Amplifier (PGA)" (DS70005146) in the "dsPIC33/PIC24 Family Reference Manual"
- Code Samples
- · Application Notes
- · Software Libraries
- Webinars
- All Related "dsPIC33/PIC24 Family Reference Manual" Sections
- Development Tools

REGISTER 25-1: PGAxCON: PGAx CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
PGAEN	PGAOEN	SELPI2	SELPI1	SELPI0	SELNI2	SELNI1	SELNI0	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	
			_	_	GAIN2	GAIN1	GAIN0	
bit 7							bit 0	
Legend:								
R = Readable	e bit	W = Writable	bit	U = Unimplei	mented bit, read	1 as '0'		
-n = Value at	POR	'1' = Bit is set	:	'0' = Bit is cleared x = Bit			it is unknown	
bit 15	PGAEN: PGA	Ax Enable bit						
	1 = PGAx mo	dule is enable	d					
	0 = PGAx mo	dule is disable	d (reduces po	ower consumpt	ion)			
bit 14	PGAOEN: PO	GAx Output En	able bit					
	1 = PGAx out	tput is connecte	ed to the DAC	OUTx pin				
	0 = PGAx out	put is not conr	nected to the I	DACOUTx pin				
bit 13-11	SELPI<2:0>:	PGAx Positive	Input Selecti	on bits				
111 = Reserved								
	110 = Reserved							
	101 = Reserv	ved						
	100 = Reserv	ved						
	011 = PGAxF	P4						
	010 = PGAxP3							

001 = PGAxP2 000 = PGAxP1

bit 10-8 **SELNI<2:0>:** PGAx Negative Input Selection bits

- 111 = Reserved 110 = Reserved
 - 101 = Reserved
 - 100 = Reserved
 - 011 = Ground (Single-Ended mode)
 - 010 = PGAxN3
 - 001 = PGAxN2
 - 000 = Ground (Single-Ended mode)
- bit 7-3 Unimplemented: Read as '0'

TABLE 27-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
CTXT4<2:0>	Alternate Working Register Set 4 Interrupt Priority Level (IPL) Select bits
	111 = Reserved
	110 = Assigned to IPL of 7
	101 = Assigned to IPL of 6
	100 = Assigned to IPL of 5
	011 = Assigned to IPL of 4
	010 = Assigned to IPL of 3
	001 = Assigned to IPL of 2
	000 = Assigned to IPL of 1
BTMODE<1:0>	Boot Mode Configuration bits
	11 = Single Partition mode
	10 = Dual Partition mode
	01 = Protected Dual Partition mode
	00 = Privileged Dual Partition mode

Note 1: The Boot Segment must be present to use the Alternate Interrupt Vector Table.

Base Instr #	Assembly Mnemonic		Assembly Syntax	Description	# of Words	# of Cycles ⁽¹⁾	Status Flags Affected
74	SL	SL	f	f = Left Shift f	1 1		C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
75	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb - lit5	1	1	C,DC,N,OV,Z
76	SUBB	SUBB	f	$f = f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = $f - WREG - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	$Wn = Wn - lit10 - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	$Wd = Wb - Ws - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	$Wd = Wb - lit5 - (\overline{C})$	1	1	C,DC,N,OV,Z
77	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
78	SUBBR	SUBBR	f	$f = WREG - f - (\overline{C})$	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	$Wd = Ws - Wb - (\overline{C})$		1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	$Wd = lit5 - Wb - (\overline{C})$	1	1	C,DC,N,OV,Z
79	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
80	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
81	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
82	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
83	TBLWTL	TBLWTL	Ws,Wd	Write Ws > 7.0 / 10 / 109 / 23.10 / 1 2 Write Ws to Prog<15:0> 1 2		None	
84	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
85	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
86	ZE	ZE	Ws, Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

TABLE 28-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Note 1: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 30-12: SPI1, SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 1) TIMING CHARACTERISTICS^(1,2)



TABLE 30-32: SPI1, SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY) TIMING REQUIREMENTS⁽⁵⁾

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$					
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾	Max.	Units	Conditions	
SP10	FscP	Maximum SCKx Frequency	_		15	MHz	(Note 3)	
SP20	TscF	SCKx Output Fall Time	_	_		ns	See Parameter DO32 (Note 4)	
SP21	TscR	SCKx Output Rise Time	-	_	_	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDOx Data Output Fall Time	—	—		ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDOx Data Output Rise Time	-	_	_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns		
SP36	TdiV2scH, TdiV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	_	ns		

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 66.7 ns. Therefore, the clock generated in Master mode must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

5: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

TABLE 30-38:SPI1, SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0)TIMING REQUIREMENTS⁽⁵⁾

AC CHA	ARACTERIS	Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}C < T_A < +85^{\circ}C$ for industrial						
		$-40^{\circ}C \le TA \le +65^{\circ}C \text{ for Extended}$						
Param.	Symbol	Characteristic ⁽¹⁾	Min.	Typ. ⁽²⁾ Max.		Units	Conditions	
SP70	FscP	Maximum SCKx Input Frequency	_	—	11	MHz	(Note 3)	
SP72	TscF	SCKx Input Fall Time	_	_	—	ns	See Parameter DO32 (Note 4)	
SP73	TscR	SCKx Input Rise Time	_	_	—	ns	See Parameter DO31 (Note 4)	
SP30	TdoF	SDOx Data Output Fall Time	—	_	—	ns	See Parameter DO32 (Note 4)	
SP31	TdoR	SDOx Data Output Rise Time	—		_	ns	See Parameter DO31 (Note 4)	
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns		
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	_	_	ns		
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	-	_	ns		
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	-	_	ns		
SP50	TssL2scH, TssL2scL	$\overline{\text{SSx}} \downarrow \text{to SCKx} \uparrow \text{or SCKx} \downarrow$	120		_	ns		
SP51	TssH2doZ	SSx ↑ to SDOx Output High-Impedance	10	—	50	ns	(Note 4)	
SP52	TscH2ssH TscL2ssH	SSx ↑ after SCKx Edge	1.5 Tcy + 40	—	_	ns	(Note 4)	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

5: Pertaining to SPI3: dsPIC33EPXXXGS702, dsPIC33EPXXXGSX04 and dsPIC33EPXXXGSX05 devices with a remappable SCK3 pin.

dsPIC33EPXXXGS70X/80X FAMILY

32.1 Package Marking Information (Continued)

44-Lead QFN (8x8 mm)



48-Lead TQFP (7x7x1.0 mm)



64-Lead TQFP (10x10x1 mm)



80-Lead TQFP (12x12x1 mm)





Example



Example



Example



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN or VQFN]





RECOMMENDED LAND PATTERN

	MILLIMETERS				
Dimension	MIN	NOM	MAX		
Contact Pitch	E	0.65 BSC			
Optional Center Pad Width	X2			6.60	
Optional Center Pad Length	Y2			6.60	
Contact Pad Spacing	C1		8.00		
Contact Pad Spacing	C2		8.00		
Contact Pad Width (X44)	X1			0.35	
Contact Pad Length (X44)	Y1			0.85	
Contact Pad to Contact Pad (X40)	G1	0.30			
Contact Pad to Center Pad (X44)	G2	0.28			
Thermal Via Diameter	V		0.33		
Thermal Via Pitch	EV		1.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

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