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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, SPI, UART/USART, USB
Peripherals	DMA, I ² S, LVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl27z128vft4

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Operating Characteristics

- Voltage range: 1.71 to 3.6 V
- Flash write voltage range: 1.71 to 3.6 V
- Temperature range: –40 to 105 °C

Packages

- 64 LQFP 10mm x 10mm, 0.5mm pitch, 1.6mm thickness
- 64 MAPBGA 5mm x 5mm, 0.5mm pitch, 1.23mm thickness
- 48 QFN 7mm x 7mm, 0.5mm pitch, 0.65mm thickness
- 32 QFN 5mm x 5mm, 0.5mm pitch, 0.65mm thickness

Security and Integrity

- 80-bit unique identification number per chip
- Advanced flash security

I/O

• Up to 50 general-purpose input/output pins (GPIO) and 6 high-drive pad

Low Power

- Down to 54uA/MHz in very low power run mode
- Down to 1.96uA in VLLS3 mode (RAM + RTC
- retained)
- · Six flexible static modes

Pro	duct	Memory		Package		IO and ADC channel		
Part number	Marking (Line1/ Line2)	Flash (KB)	SRAM (KB)	Pin count	Package	GPIOs	GPIOs (INT/HD) ¹	ADC channels (SE/DP)
MKL27Z128VFM4	M27P7V	128	32	32	QFN	23	19/6	7/0
MKL27Z256VFM4	M27P8V	256	32	32	QFN	23	19/6	7/0
MKL27Z128VFT4	M27P7V	128	32	48	QFN	36	24/6	14/1
MKL27Z256VFT4	M27P8V	256	32	48	QFN	36	24/6	14/1
MKL27Z128VLH4	MKL27Z128V//LH4	128	32	64	LQFP	50	31/6	16/2
MKL27Z256VLH4	MKL27Z256V//LH4	256	32	64	LQFP	50	31/6	16/2
MKL27Z128VMP4	M27P7V	128	32	64	MAPBGA	50	31/6	16/2
MKL27Z256VMP4	M27P8V	256	32	64	MAPBGA	50	31/6	16/2

Ordering Information

1. INT: interrupt pin numbers; HD: high drive pin numbers

Related Resources

Туре	Description	Resource
Selector Guide	The Freescale Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.	Solution Advisor
Product Brief	The Product Brief contains concise overview/summary information to enable quick evaluation of a device for design suitability.	KL2XPB ¹
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.	KL27P64M48SF6RM ¹
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.	This document.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.	KINETIS_L_1N71K ¹
Package drawing	Package dimensions are provided in package drawings.	64-LQFP: 98ASS23234W ¹ 64 MAPBGA: 98ASA00420D ¹ 32 QFN: 98ASA00615D ¹ 48 QFN: 98ASA00616D ¹

1. To find the associated resource, go to http://www.freescale.com and perform a search using this term.





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1 Ratings

1.1 Thermal handling ratings

Table 1. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T _{STG}	Storage temperature	-55	150	°C	1
T _{SDR}	Solder temperature, lead-free	_	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, High Temperature Storage Life.

2. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.2 Moisture handling ratings

Table 2. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3		1

1. Determined according to IPC/JEDEC Standard J-STD-020, Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices.

1.3 ESD handling ratings

Table 3. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V _{HBM}	Electrostatic discharge voltage, human body model	-2000	+2000	V	1
V _{CDM}	Electrostatic discharge voltage, charged-device model	-500	+500	V	2
I _{LAT}	Latch-up current at ambient temperature of 105 °C	-100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.

 Determined according to JEDEC Standard JESD22-C101, Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components.

3. Determined according to JEDEC Standard JESD78, IC Latch-Up Test.



2.2 Nonswitching electrical specifications

2.2.1 Voltage and current operating requirements Table 5. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V _{DD}	Supply voltage	1.71	3.6	V	
V _{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} - V_{DDA}$	V _{DD} -to-V _{DDA} differential voltage	-0.1	0.1	V	
$V_{SS} - V_{SSA}$	V _{SS} -to-V _{SSA} differential voltage	-0.1	0.1	V	
VIH	Input high voltage				
	• 2.7 V \leq V _{DD} \leq 3.6 V	$0.7 \times V_{DD}$	—	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$	$0.75 \times V_{DD}$	_	V	
V _{IL}	Input low voltage				
	• 2.7 V \leq V _{DD} \leq 3.6 V	_	$0.35 \times V_{DD}$	V	
	• $1.7 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}$		$0.3 \times V_{DD}$	V	
V _{HYS}	Input hysteresis	$0.06 \times V_{DD}$	_	V	
l _{icio}	IO pin negative DC injection current — single pin • V _{IN} < V _{SS} -0.3V	-3	_	mA	1
I _{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	_	mA	
V _{ODPU}	Open drain pullup voltage level	V _{DD}	V _{DD}	V	2
V _{RAM}	V _{DD} voltage required to retain RAM	1.2	—	V	

1. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD} . If V_{IN} greater than V_{IO_MIN} (= V_{SS} -0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = ($V_{IO_MIN} - V_{IN}$)/II_{CIO}I.

2. Open drain outputs must be pulled to V_{DD} .

2.2.2 LVD and POR operating requirements Table 6. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{POR}	Falling V _{DD} POR detect voltage	0.8	1.1	1.5	V	—

Table continues on the next page ...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
V _{LVDH}	Falling low-voltage detect threshold — high range (LVDV = 01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V _{LVW1H}	 Level 1 falling (LVWV = 00) 	2.62	2.70	2.78	v	
V _{LVW2H}	 Level 2 falling (LVWV = 01) 	2.72	2.80	2.88	v	
V _{LVW3H}	 Level 3 falling (LVWV = 10) 	2.82	2.90	2.98	v	
V _{LVW4H}	• Level 4 falling (LVWV = 11)	2.92	3.00	3.08	v	
V _{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range		±60	_	mV	_
V _{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	_
	Low-voltage warning thresholds — low range					1
V _{LVW1L}	 Level 1 falling (LVWV = 00) 	1.74	1.80	1.86	v	
V _{LVW2L}	 Level 2 falling (LVWV = 01) 	1.84	1.90	1.96	v	
V _{LVW3L}	 Level 3 falling (LVWV = 10) 	1.94	2.00	2.06	v	
V _{LVW4L}	• Level 4 falling (LVWV = 11)	2.04	2.10	2.16	v	
V _{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range		±40	_	mV	_
V _{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t _{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

Table 6. V_{DD} supply LVD and POR operating requirements (continued)

1. Rising thresholds are falling threshold + hysteresis voltage

2.2.3 Voltage and current operating behaviors Table 7. Voltage and current operating behaviors

Symbol	Description	Min.	Max.	Unit	Notes
V _{OH}	Output high voltage — normal drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -5 mA	V _{DD} – 0.5	_	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -1.5 \text{ mA}$	$V_{DD} - 0.5$	—	V	
V _{OH}	Output high voltage — high drive pad				1
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OH} = -18 mA	V _{DD} – 0.5	—	V	
	• $1.71 \text{ V} \le \text{V}_{\text{DD}} \le 2.7 \text{ V}, \text{ I}_{\text{OH}} = -6 \text{ mA}$	$V_{DD} - 0.5$	—	V	
I _{OHT}	Output high current total for all ports	—	100	mA	
V _{OL}	Output low voltage — normal drive pad	_	0.5	V	1

Table continues on the next page...



Symbol	Description	Min.	Max.	Unit	Notes
	• 2.7 V \leq V _{DD} \leq 3.6 V, I _{OL} = 5 mA • 1.71 V \leq V _{DD} \leq 2.7 V, I _{OL} = 1.5 mA	—	0.5	V	
V _{OL}	Output low voltage — high drive pad				1
	• 2.7 V \leq V_{DD} \leq 3.6 V, I_{OL} = 18 mA	—	0.5	V	
	• 1.71 V \leq V _{DD} \leq 2.7 V, I _{OL} = 6 mA	_	0.5	V	
I _{OLT}	Output low current total for all ports	—	100	mA	
I _{IN}	Input leakage current (per pin) for full temperature range	_	1	μA	2
I _{IN}	Input leakage current (per pin) at 25 °C	—	0.025	μA	2
I _{IN}	Input leakage current (total all pins) for full temperature range	_	64	μA	2
I _{OZ}	Hi-Z (off-state) leakage current (per pin)	—	1	μA	
R _{PU}	Internal pullup resistors	20	50	kΩ	3

1. PTB0, PTB1, PTC3, PTC4, PTD6, and PTD7 I/O have both high drive and normal drive capability selected by the associated PTx_PCRn[DSE] control bit. All other GPIOs are normal drive only.

2. Measured at $V_{DD} = 3.6$ V

3. Measured at V_{DD} supply voltage = V_{DD} min and Vinput = V_{SS}

2.2.4 Power mode transition operating behaviors

All specifications except t_{POR} and VLLSx \rightarrow RUN recovery times in the following table assume this clock configuration:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- HIRC clock mode

Table 8. Power mode transition operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{POR}	After a POR event, amount of time from the point V_{DD} reaches 1.8 V to execution of the first instruction across the operating temperature range of the chip.	_	_	300	μs	1
	• VLLS0 \rightarrow RUN	_	152	166	μs	
	• VLLS1 → RUN	_	152	166	μs	
	• VLLS3 → RUN	_	93	104	μs	

Table continues on the next page ...



Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	• at 50 °C	—	10.26	17.62		
	• at 85 °C	—	33.49	60.19	μA	
	• at 105 °C	—	102.92	162.20		
I _{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V		2.06	3.33	μA	
		—	4.72	6.85		
	• at 50 C	_	8.13	13.30		
		_	13.34	24.70		
	• at 105 °C	—	41.08	52.43		
I _{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V • at 25 °C and below		2.46	3.73	μΑ	
	• at 50 °C	_	5.12	7.25		
	• at 70 °C	_	8.53	11.78		
	• at 85 °C		13.74	18.91		
	• at 105 °C		41.48	52.83		
I _{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V • at 25 °C and below • at 50 °C		2.35 4.91 8.32 13.44 40.47 1.45 3.37 5.76	2.70 6.75 11.78 18.21 51.85 1.85 4.39 8.48	μΑ	3
	• at 70 °C		0.70	0.40		
	• at 85 °C	_	3.72	27.50		
	• at 105 °C	_	30.41	37.50		
I _{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V • at 25 °C and below • at 50 °C • at 70 °C • at 85 °C • at 105 °C		2.05 3.97 6.36 10.32 31.01	2.45 4.99 9.08 14.73 38.10	μΑ	3

 Table 9. Power consumption operating behaviors (continued)

Table continues on the next page...



Symbol	Description	Temperature (°C)				Unit		
		-40	25	50	70	85	105	
								nA
I _{CMP}	CMP peripheral adder measured by placing the device in VLLS1 mode with CMP enabled using the 6-bit DAC and a single external input for compare. Includes 6-bit DAC power consumption.	22	22	22	22	22	22	μA
I _{UART}	 UART peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source waiting for RX data at 115200 baud rate. Includes selected clock source power consumption. IRC8M (8 MHz internal reference clock) IRC2M (2 MHz internal reference clock) 	114 34	114 34	114 34	114 34	114 34	114 34	μΑ
I _{TPM}	 TPM peripheral adder measured by placing the device in STOP or VLPS mode with selected clock source configured for output compare generating 100 Hz clock signal. No load is placed on the I/O generating the clock signal. Includes selected clock source and I/O switching currents. IRC8M (8 MHz internal reference clock) IRC2M (2 MHz internal reference clock) 	147 42	147 42	147 42	147 42	147 42	147 42	μΑ
I _{BG}	Bandgap adder when BGEN bit is set and device is placed in VLPx or VLLSx mode.	45	45	45	45	45	45	μA
I _{ADC}	ADC peripheral adder combining the measured values at V_{DD} and V_{DDA} by placing the device in STOP or VLPS mode. ADC is configured for low power mode using the internal clock and continuous conversions.	330	330	330	330	330	330	μA

2.2.5.1 Diagram: Typical IDD_RUN operating behavior

The following data was measured under these conditions:

- MCG-Lite in HIRC for run mode, and LIRC for VLPR mode
- USB regulator disabled
- No GPIOs toggled
- Code execution from flash
- For the ALLOFF curve, all peripheral clocks are disabled except FTFA



of Electromagnetic Emissions, 150 kHz to 1 GHz Part 2: Measurement of Radiated Emissions—TEM Cell and Wideband TEM Cell Method. Measurements were made while the microcontroller was running basic application code. The reported emission level is the value of the maximum measured emission, rounded up to the next whole number, from among the measured orientations in each frequency range.

- 2. $V_{DD} = 3.3 \text{ V}, \text{ T}_{A} = 25 \text{ °C}, \text{ } f_{OSC} = IRC48M, \text{ } f_{SYS} = 48 \text{ } \text{MHz}, \text{ } f_{BUS} = 24 \text{ } \text{MHz}$
- 3. Specified according to Annex D of IEC Standard 61967-2, Measurement of Radiated Emissions TEM Cell and Wideband TEM Cell Method

2.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

- 1. Go to www.freescale.com.
- 2. Perform a keyword search for "EMC design."

2.2.8 Capacitance attributes

Table 12. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C _{IN}	Input capacitance	—	7	pF

2.3 Switching specifications

2.3.1 Device clock specifications

Table 13. Device clock specifications

Symbol	Description	Min.	Max.	Unit
	Normal run mode			
f _{SYS}	System and core clock ¹	_	48	MHz
f _{BUS}	Bus clock ¹	_	24	MHz
f _{FLASH}	Flash clock ¹	_	24	MHz
f _{SYS_USB}	System and core clock when Full Speed USB in operation	20	—	MHz
f _{LPTMR}	LPTMR clock	_	24	MHz
	VLPR and VLPS modes ²			•
f _{SYS}	System and core clock	—	4	MHz
f _{BUS}	Bus clock	_	1	MHz
f _{FLASH}	Flash clock	_	1	MHz

Table continues on the next page...



Symbol	Description	Min.	Max.	Unit
f _{LPTMR}	LPTMR clock ³	—	24	MHz
f _{LPTMR_ERCLK}	LPTMR external reference clock	—	16	MHz
f _{osc_hi_2}	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	—	16	MHz
f _{TPM}	TPM asynchronous clock	—	8	MHz
f _{LPUART0/1}	LPUART0/1 asynchronous clock		8	MHz

Table 13. Device clock specifications (continued)

1. The maximum value of system clock, core clock, bus clock, and flash clock under normal run mode can be 3% higher than the specified maximum frequency when IRC 48MHz is used as the clock source.

 The frequency limitations in VLPR and VLPS modes here override any frequency specification listed in the timing specification for any other module. These same frequency limits apply to VLPS, whether VLPS was entered from RUN or from VLPR.

3. The LPTMR can be clocked at this speed in VLPR or VLPS only when the source is an external pin.

2.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO and UART signals.

 Table 14.
 General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
External RESET and NMI pin interrupt pulse width — Asynchronous path	100		ns	2
GPIO pin interrupt pulse width — Asynchronous path	16		ns	2
Port rise and fall time		36	ns	3

1. The synchronous and asynchronous timing must be met.

2. This is the shortest pulse that is guaranteed to be recognized.

3. 75 pF load

2.4 Thermal specifications



Peripheral operating requirements and behaviors

3.4.1.1 Flash timing specifications — program and erase

The following specifications represent the amount of time the internal charge pumps are active and do not include command overhead.

Table 22.	NVM program/erase timing spec	cifications
-----------	-------------------------------	-------------

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
t _{hvpgm4}	Longword Program high-voltage time	—	7.5	18	μs	—
t _{hversscr}	Sector Erase high-voltage time	—	13	113	ms	1
t _{hversblk128k}	Erase Block high-voltage time for 128 KB	—	52	452	ms	1

1. Maximum time based on expectations at cycling end-of-life.

3.4.1.2 Flash timing specifications — commands Table 23. Flash command timing specifications

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
	Read 1s Block execution time					1
t _{rd1blk128k}	• 128 KB program flash	_	_	1.7	ms	
t _{rd1sec1k}	Read 1s Section execution time (flash sector)	—	—	60	μs	1
t _{pgmchk}	Program Check execution time	—	—	45	μs	1
t _{rdrsrc}	Read Resource execution time	—	—	30	μs	1
t _{pgm4}	Program Longword execution time	—	65	145	μs	—
	Erase Flash Block execution time					2
t _{ersblk128k}	128 KB program flash	_	88	600	ms	
t _{ersscr}	Erase Flash Sector execution time	—	14	114	ms	2
t _{rd1all}	Read 1s All Blocks execution time	—	—	1.8	ms	1
t _{rdonce}	Read Once execution time	—	—	25	μs	1
t _{pgmonce}	Program Once execution time	—	65	—	μs	—
t _{ersall}	Erase All Blocks execution time	—	175	1300	ms	2
t _{vfykey}	Verify Backdoor Access Key execution time	—	—	30	μs	1
t _{ersallu}	Erase All Blocks Unsecure execution time	—	175	1300	ms	2

1. Assumes 25 MHz flash clock frequency.

2. Maximum times for erase parameters based on expectations at cycling end-of-life.



3.4.1.3 Flash high voltage current behaviors Table 24. Flash high voltage current behaviors

Symbol	Description	Min.	Тур.	Max.	Unit
I _{DD_PGM}	Average current adder during high voltage flash programming operation		2.5	6.0	mA
I _{DD_ERS}	Average current adder during high voltage flash erase operation		1.5	4.0	mA

3.4.1.4 Reliability specifications

Table 25. NVM reliability specifications

Symbol	Description	Min.	Typ. ¹	Max.	Unit	Notes	
Program Flash							
t _{nvmretp10k}	Data retention after up to 10 K cycles	5	50	—	years	_	
t _{nvmretp1k}	Data retention after up to 1 K cycles	20	100	_	years		
n _{nvmcycp}	Cycling endurance	10 K	50 K		cycles	2	

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25 °C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.

2. Cycling endurance represents number of program/erase cycles at -40 °C \leq T_i \leq 125 °C.

3.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

3.6 Analog

3.6.1 ADC electrical specifications

Using differential inputs can achieve better system accuracy than using single-end inputs.



Peripheral operating requirements and behaviors

3.6.4.2 12-bit DAC operating behaviors Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Тур.	Max.	Unit	Notes
I _{DDA_DACL} P	Supply current — low-power mode		—	250	μΑ	
I _{DDA_DACH}	Supply current — high-speed mode	_	—	900	μΑ	
t _{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	_	100	200	μs	1
t _{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	_	15	30	μs	1
t _{CCDACLP}	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	_	0.7	1	μs	1
V _{dacoutl}	DAC output voltage range low — high- speed mode, no load, DAC set to 0x000	_	—	100	mV	
V _{dacouth}	DAC output voltage range high — high- speed mode, no load, DAC set to 0xFFF	V _{DACR} -100	-	V _{DACR}	mV	
INL	Integral non-linearity error — high speed mode	_	—	±8	LSB	2
DNL	Differential non-linearity error — $V_{DACR} > 2$ V	_	_	±1	LSB	3
DNL	Differential non-linearity error — V _{DACR} = VREF_OUT	_	_	±1	LSB	4
VOFFSET	Offset error	—	±0.4	±0.8	%FSR	5
E _G	Gain error	_	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, $V_{DDA} \ge 2.4 V$	60	—	90	dB	
T _{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T _{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = $3 \text{ k}\Omega$)	—	—	250	Ω	
SR	Slew rate -80h \rightarrow F7Fh \rightarrow 80h				V/µs	
	 High power (SP_{HP}) 	1.2	1.7	—		
	• Low power (SP _{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP _{HP})	550	_	_		
	 Low power (SP_{LP}) 	40	-	—		

1. Settling within ± 1 LSB

2. The INL is measured for 0 + 100 mV to V_{DACR} –100 mV

3. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV

4. The DNL is measured for 0 + 100 mV to V_{DACR} –100 mV with V_{DDA} > 2.4 V 5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} – 100 mV

6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_CO:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device



Num.	Symbol	Description	Min.	Max.	Unit	Note
8	t _v	Data valid (after SPSCK edge)	—	52	ns	—
9	t _{HO}	Data hold time (outputs)	0	_	ns	
10	t _{RI}	Rise time input	—	t _{periph} - 25	ns	
	t _{FI}	Fall time input				
11	t _{RO}	Rise time output	—	36	ns	
	t _{FO}	Fall time output				

Table 37. SPI master mode timing on slew rate enabled pads (continued)

- 1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
- 2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 14. SPI master mode timing (CPHA = 0)



Num.	Characteristic	Min.	Max.	Unit
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	_	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	_	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	_	ns

Table 42.	I2S/SAI	master	mode	timing	(continued))
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Figure 19. I2S/SAI timing — master modes

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	_	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)		55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	_	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	_	ns

Table 43. I2S/SAI slave mode timing

Table continues on the next page ...



	1	2	3	4	5	6	7	8	
A	PTE0	PTD7	PTD4/ LLWU_P14	PTD1	PTC11	PTC8	PTC6/ LLWU_P10	PTC5/ LLWU_P9	A
в	PTE1	PTD6/ LLWU_P15	PTD3	PTC10	PTC9	PTC7	PTC2	PTC4/ LLWU_P8	в
С	PTD5	PTD2	PTD0	VSS	NC	PTC1/ LLWU_P6/ RTC_CLKIN	PTB19	PTC3/ LLWU_P7	с
D	USB0_DM	VREGIN	PTA0	PTA1	PTA3	PTB18	PTB17	PTC0	D
Е	USB0_DP	VOUT33	VSS	VDD	PTA2	PTB16	PTB2	PTB3	E
F	PTE21	PTE23	VSSA	VDDA	PTA5	PTB1	PTB0/ LLWU_P5	PTA20	F
G	PTE20	PTE22	VREFL	VREFH	PTA4	PTA13	VDD	PTA19	G
н	PTE29	PTE30	PTE31	PTE24	PTE25	PTA12	VSS	PTA18	н
	1	2	3	4	5	6	7	8	•

Figure 26. 64 MAPBGA Pinout diagram

6 Ordering parts

6.1 Determining valid orderable parts

Valid orderable part numbers are provided on the Web. To determine the orderable part numbers for this device, go to freescale.com and perform a part number search for the following device numbers:

7 Part identification



8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition			
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure:			
	 Operating ratings apply during operation of the chip. Handling ratings apply when the chip is not powered. 			
	NOTE: The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.			
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip			
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions			
Typical value	A specified value for a technical characteristic that:			
	 Lies within the range of values specified by the operating behavior Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions 			
	NOTE: Typical values are provided as design guidelines and are neither tested nor guaranteed.			



Terminology and guidelines

Examples 8.2

Operating rating:

		<u>_</u>		
Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	-0.3 LAM	1.2	V

Operating requirement:

Operating require	ment.			
Symbol	Description	Min.	Max.	Unit
V _{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a typical value:

Symbol	Description	Min.	Тур.	Max.	Unit
I _{WP}	Digital I/O weak pullup/pulldown current	10 AM	70	130	μA

Typical-value conditions 8.3

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T _A	Ambient temperature	25	°C
V _{DD}	3.3 V supply voltage	3.3	V





8.4 Relationship between ratings and operating requirements

8.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

9 Revision History

The following table provides a revision history for this document.

Rev. No.	Date	Substantial Changes
3	09 August 2014	 Initial Public release Updated Table 9 - Power consumption operating behaviors. Added a note related to 32 QFN pin package in Pinouts topic.
4	03 March 2015	Updated the features and completed the ordering information.Removed thickness dimension from package diagrams.

Table 47. Revision History

Table continues on the next page ...