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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M0+
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I²C, SPI, UART/USART, USB
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	50
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mkl27z128vlh4

Table 8. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• LLS → RUN	—	7.5	8	µs	
	• VLPS → RUN	—	7.5	8	µs	
	• STOP → RUN	—	7.5	8	µs	

1. Normal boot (FTFA_FOPT[LPBOOT]=11)

2.2.5 Power consumption operating behaviors

The maximum values stated in the following table represent characterized results equivalent to the mean plus three times the standard deviation (mean + 3 sigma).

NOTE

The while (1) test is executed with flash cache enabled.

Table 9. Power consumption operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA}	Analog supply current	—	—	See note	mA	1
I_{DD_RUNCO}	Running CoreMark in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	5.76	6.40	mA	
	• at 105 °C	—	6.04	6.68		
I_{DD_RUNCO}	Running While(1) loop in flash in compute operation mode—48M HIRC mode, 48 MHz core / 24 MHz flash, V_{DD} = 3.0 V					
	• at 25 °C	—	3.21	3.85	mA	
	• at 105 °C	—	3.49	4.13		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in Flash all peripheral clock disable 48 MHz core/24 MHz flash, V_{DD} = 3.0 V					2
	• at 25 °C	—	6.45	7.09	mA	
	• at 105 °C	—	6.75	7.39		
I_{DD_RUN}	Run mode current—48M HIRC mode, running CoreMark in flash all peripheral clock disable, 24 MHz core/12 MHz flash, V_{DD} = 3.0 V					2
		—	3.95	4.59		
		—	4.23	4.87	mA	

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	disable, 125 kHz core / 31.25 kHz flash, V_{DD} = 3.0 V • at 25 °C	—	50	131	µA	
I_{DD_VLPR}	Very-low-power run mode current—2 MHz LIRC mode, While(1) loop in SRAM all peripheral clock enable, 2 MHz core / 0.5 MHz flash, V_{DD} = 3.0 V • at 25 °C	—	208	289	µA	
I_{DD_WAIT}	Wait mode current—core disabled, 48 MHz system/24 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.81	1.89	mA	
I_{DD_WAIT}	Wait mode current—core disabled, 24 MHz system/12 MHz bus, flash disabled (flash doze enabled), all peripheral clocks disabled, MCG_Lite under HIRC mode, V_{DD} = 3.0 V	—	1.22	1.39	mA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 4 MHz system/ 1 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	172	182	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 2 MHz system/ 0.5 MHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	69	76	µA	
I_{DD_VLPW}	Very-low-power wait mode current, core disabled, 125 kHz system/ 31.25 kHz bus and flash, all peripheral clocks disabled, V_{DD} = 3.0 V	—	36	40	µA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, 12 MHz bus and flash, V_{DD} = 3.0 V	—	1.81	2.06	mA	
I_{DD_PSTOP2}	Partial Stop 2, core and system clock disabled, flash doze enabled, 12 MHz bus, V_{DD} = 3.0 V	—	1.00	1.25	mA	
I_{DD_STOP}	Stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	161.93 181.45 236.29 390.33	171.82 191.96 271.17 465.58	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 3.0 V • at 25 °C and below • at 50 °C • at 85 °C • at 105 °C	— — — —	3.31 10.43 34.14 104.38	5.14 17.68 61.06 164.44	µA	
I_{DD_VLPS}	Very-low-power stop mode current at 1.8 V • at 25 °C and below	—	3.21	5.22		

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• at 50 °C	—	10.26	17.62		
	• at 85 °C	—	33.49	60.19	µA	
	• at 105 °C	—	102.92	162.20		
I_{DD_LLS}	Low-leakage stop mode current, all peripheral disable, at 3.0 V					
	• at 25 °C and below	—	2.06	3.33	µA	
	• at 50 °C	—	4.72	6.85		
	• at 70 °C	—	8.13	13.30		
	• at 85 °C	—	13.34	24.70		
	• at 105 °C	—	41.08	52.43		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 3.0 V					
	• at 25 °C and below	—	2.46	3.73	µA	
	• at 50 °C	—	5.12	7.25		
	• at 70 °C	—	8.53	11.78		
	• at 85 °C	—	13.74	18.91		
	• at 105 °C	—	41.48	52.83		
I_{DD_LLS}	Low-leakage stop mode current with RTC current, at 1.8 V					3
	• at 25 °C and below	—	2.35	2.70	µA	
	• at 50 °C	—	4.91	6.75		
	• at 70 °C	—	8.32	11.78		
	• at 85 °C	—	13.44	18.21		
	• at 105 °C	—	40.47	51.85		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current, all peripheral disable, at 3.0 V					
	• at 25 °C and below	—	1.45	1.85	µA	
	• at 50 °C	—	3.37	4.39		
	• at 70 °C	—	5.76	8.48		
	• at 85 °C	—	9.72	14.30		
	• at 105 °C	—	30.41	37.50		
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 3.0 V					3
	• at 25 °C and below	—	2.05	2.45	µA	
	• at 50 °C	—	3.97	4.99		
	• at 70 °C	—	6.36	9.08		
	• at 85 °C	—	10.32	14.73		
	• at 105 °C	—	31.01	38.10		

Table continues on the next page...

Table 9. Power consumption operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_VLLS3}	Very-low-leakage stop mode 3 current with RTC current, at 1.8 V				µA	3
	• at 25 °C and below	—	1.96	2.36		
	• at 50 °C	—	3.86	5.67		
	• at 70 °C	—	6.23	8.53		
	• at 85 °C	—	10.21	13.37		
	• at 105 °C	—	30.25	37.02		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current all peripheral disabled at 3.0 V				µA	
	• at 25 °C and below	—	0.66	0.80		
	• at 50°C	—	1.78	3.87		
	• at 70°C	—	2.55	4.26		
	• at 85°C	—	4.83	6.64		
	• at 105 °C	—	16.42	20.49		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 3.0 V				µA	3
	• at 25 °C and below	—	1.26	1.40		
	• at 50°C	—	2.38	4.47		
	• at 70°C	—	3.15	4.86		
	• at 85°C	—	5.43	7.24		
	• at 105 °C	—	17.02	21.09		
I_{DD_VLLS1}	Very-low-leakage stop mode 1 current RTC enabled at 1.8 V				µA	3
	• at 25 °C and below	—	1.16	1.30		
	• at 50°C	—	1.96	2.28		
	• at 70°C	—	2.78	3.37		
	• at 85°C	—	4.85	6.88		
	• at 105 °C	—	15.78	18.81		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 0) at 3.0 V				µA	
	• at 25 °C and below	—	0.35	0.47		
	• at 50 °C	—	1.25	1.44		
	• at 70 °C	—	2.53	3.24		
	• at 85 °C	—	4.40	5.24		
	• at 105 °C	—	16.09	19.29		
I_{DD_VLLS0}	Very-low-leakage stop mode 0 current all peripheral disabled (SMC_STOPCTRL[PORPO] = 1) at 3 V					

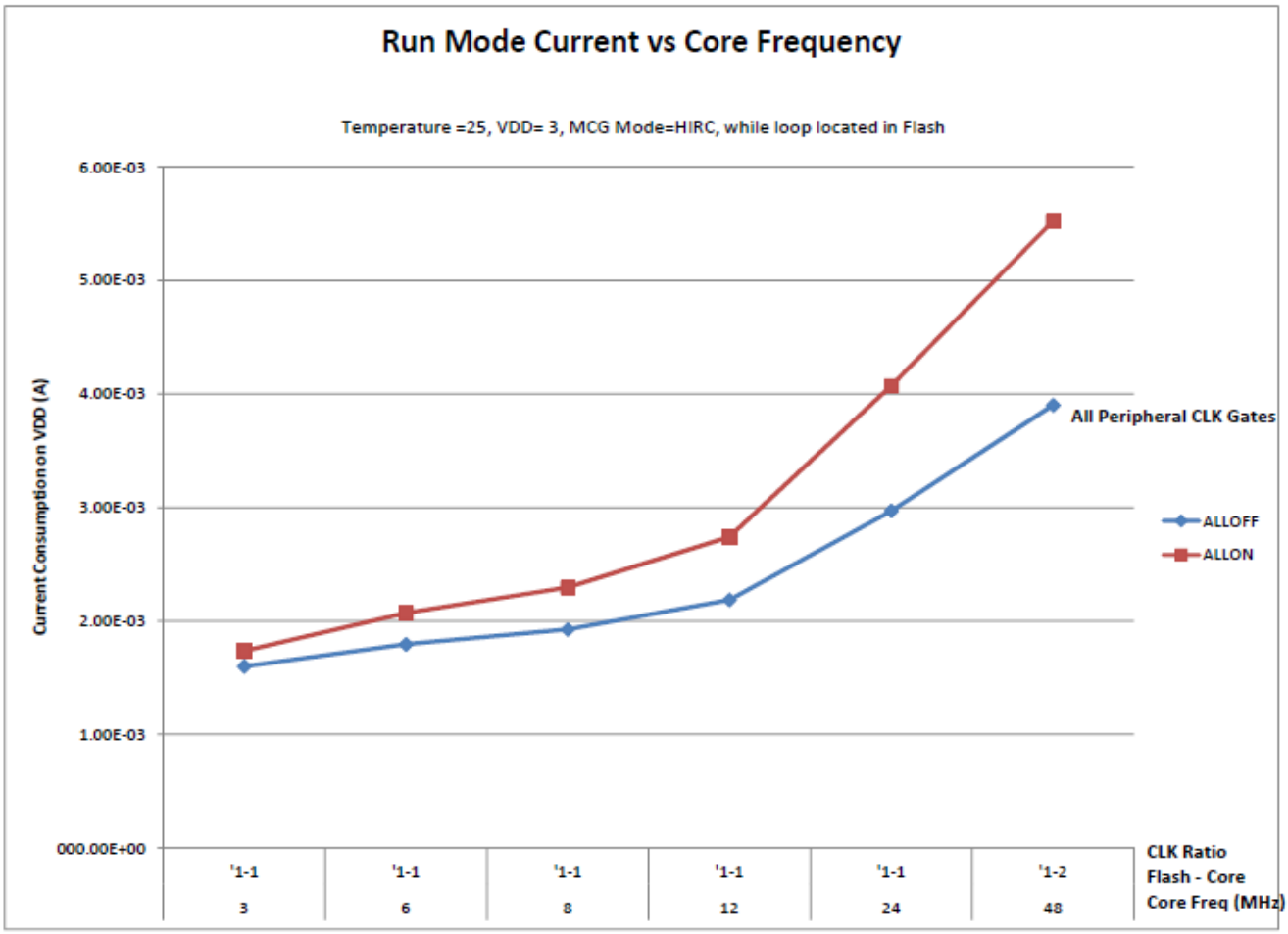
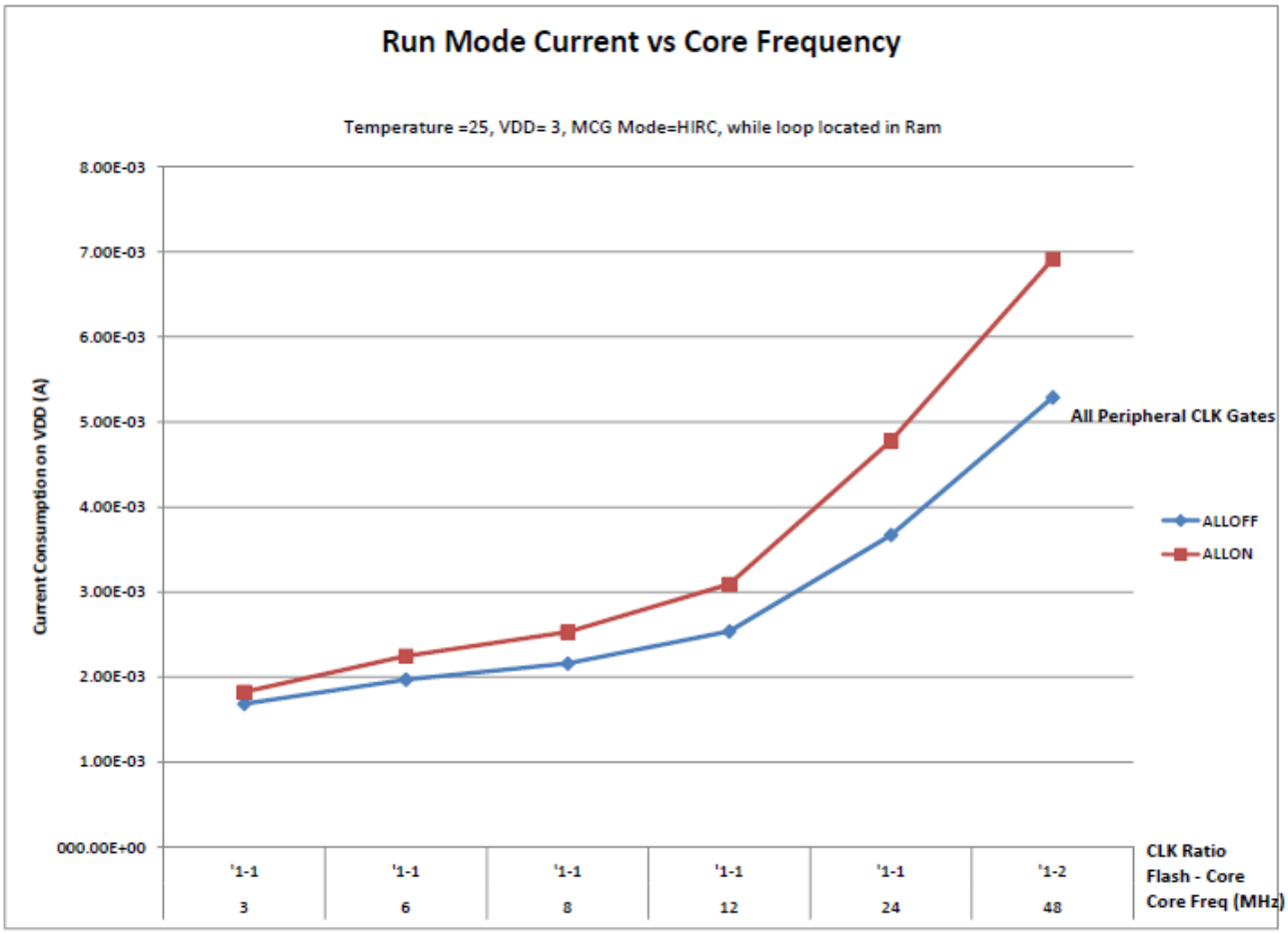


Figure 2. Run mode supply current vs. core frequency


Run Mode Current vs Core Frequency
Temperature =25, VDD= 3, MCG Mode=HIRC, while loop located in Ram
Current Consumption on VDD (A)
8.00E-03
7.00E-03
6.00E-03
5.00E-03
4.00E-03
3.00E-03
2.00E-03
1.00E-03
000.00E+00
All Peripheral CLK Gates
ALLOFF
ALLON
'1-1
3
'1-1
6
'1-1
8
'1-1
12
'1-1
24
'1-2
48
CLK Ratio
Flash - Core
Core Freq (MHz)

2.4.1 Thermal operating requirements

Table 15. Thermal operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

2.4.2 Thermal attributes

Table 16. Thermal attributes

Board type	Symbol	Description	48 QFN	32 QFN	64 LQFP	64 MAPBGA	Unit	Notes
Single-layer (1S)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	86	101	70	50.3	°C/W	1
Four-layer (2s2p)	$R_{\theta JA}$	Thermal resistance, junction to ambient (natural convection)	29	33	51	42.9	°C/W	
Single-layer (1S)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	71	84	58	41.4	°C/W	
Four-layer (2s2p)	$R_{\theta JMA}$	Thermal resistance, junction to ambient (200 ft./min. air speed)	24	28	45	38.0	°C/W	
—	$R_{\theta JB}$	Thermal resistance, junction to board	12	13	33	39.6	°C/W	2
—	$R_{\theta JC}$	Thermal resistance, junction to case	1.7	1.7	20	27.3	°C/W	3
—	Ψ_{JT}	Thermal characterization parameter, junction to package top outside center (natural convection)	2	3	4	0.4	°C/W	4
—	Ψ_{JB}	Thermal characterization parameter, junction to package bottom (natural convection)	-	-	-	12.6	°C/W	5

1. Determined according to JEDEC Standard JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions—Natural Convection (Still Air)*, or EIA/JEDEC Standard JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions—Forced Convection (Moving Air)*.
2. Determined according to JEDEC Standard JESD51-8, *Integrated Circuit Thermal Test Method Environmental Conditions—Junction-to-Board*.
3. Determined according to Method 1012.1 of MIL-STD 883, *Test Method Standard, Microcircuits*, with the cold plate temperature used for the case temperature. The value includes the thermal resistance of the interface material between the top of the package and the cold plate.

3. C_x,C_y can be provided by using the integrated capacitors when the low frequency oscillator (RANGE = 00) is used. For all other cases external capacitors must be used.
4. When low power mode is selected, R_F is integrated and must not be attached externally.
5. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

3.3.2.2 Oscillator frequency specifications

Table 21. Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal or resonator frequency — low-frequency mode (MCG_C2[RANGE]=00)	32	—	40	kHz	
$f_{osc\_hi\_1}$	Oscillator crystal or resonator frequency — high-frequency mode (low range) (MCG_C2[RANGE]=01)	3	—	8	MHz	
$f_{osc\_hi\_2}$	Oscillator crystal or resonator frequency — high frequency mode (high range) (MCG_C2[RANGE]=1x)	8	—	32	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	48	MHz	1, 2
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal startup time — 32 kHz low-frequency, low-power mode (HGO=0)	—	750	—	ms	3, 4
	Crystal startup time — 32 kHz low-frequency, high-gain mode (HGO=1)	—	250	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), low-power mode (HGO=0)	—	0.6	—	ms	
	Crystal startup time — 8 MHz high-frequency (MCG_C2[RANGE]=01), high-gain mode (HGO=1)	—	1	—	ms	

1. Other frequency limits may apply when external clock is being used as a reference for the FLL
2. When transitioning from FEI or FBI to FBE mode, restrict the frequency of the input clock so that, when it is divided by FRDIV, it remains within the limits of the DCO input clock frequency.
3. Proper PC board layout procedures must be followed to achieve specifications.
4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

3.4 Memories and memory interfaces

3.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

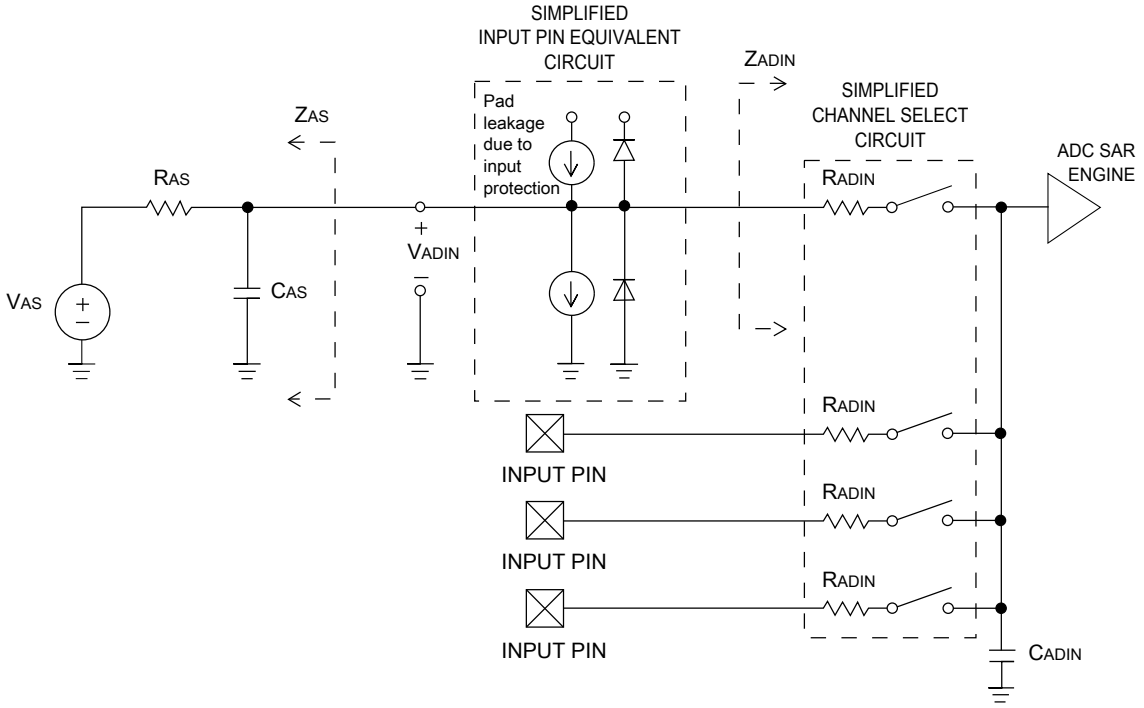


Figure 7. ADC input impedance equivalency diagram

3.6.1.2 16-bit ADC electrical characteristics

Table 27. 16-bit ADC characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ.[2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current		0.215	—	1.7	mA	3
f_{ADACK}	ADC asynchronous clock source	• ADLPC = 1, ADHSC = 0	1.2	2.4	3.9	MHz	t_{ADACK} = $1/f_{ADACK}$
		• ADLPC = 1, ADHSC = 1	2.4	4.0	6.1	MHz	
		• ADLPC = 0, ADHSC = 0	3.0	5.2	7.3	MHz	
		• ADLPC = 0, ADHSC = 1	4.4	6.2	9.5	MHz	
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit modes	—	±4	±6.8	LSB[4]	5
		• <12-bit modes	—	±1.4	±2.1		
DNL	Differential non-linearity	• 12-bit modes	—	±0.7	–1.1 to +1.9	LSB[4]	5
		• <12-bit modes	—	±0.2	–0.3 to 0.5		
INL	Integral non-linearity	• 12-bit modes	—	±1.0	–2.7 to +1.9	LSB[4]	5

Table continues on the next page...

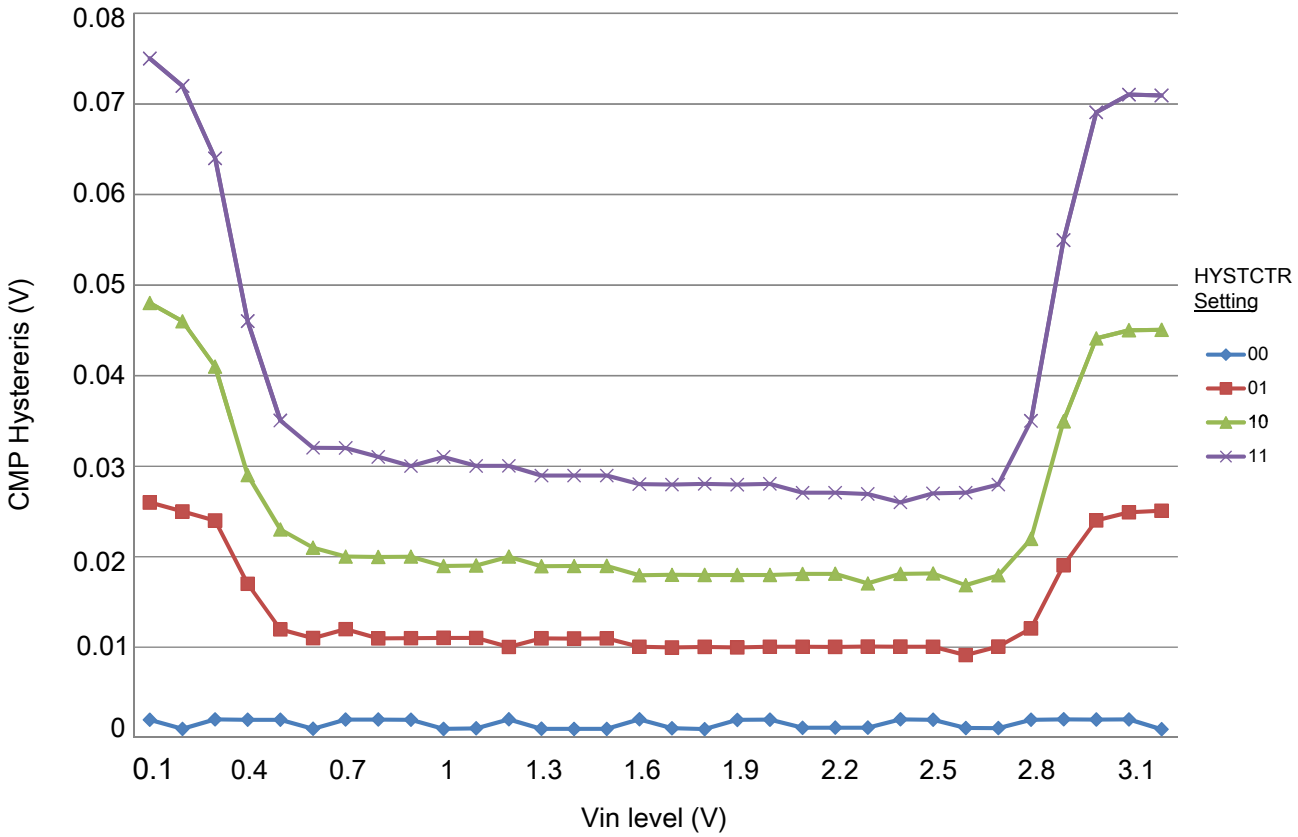


Figure 10. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 0)

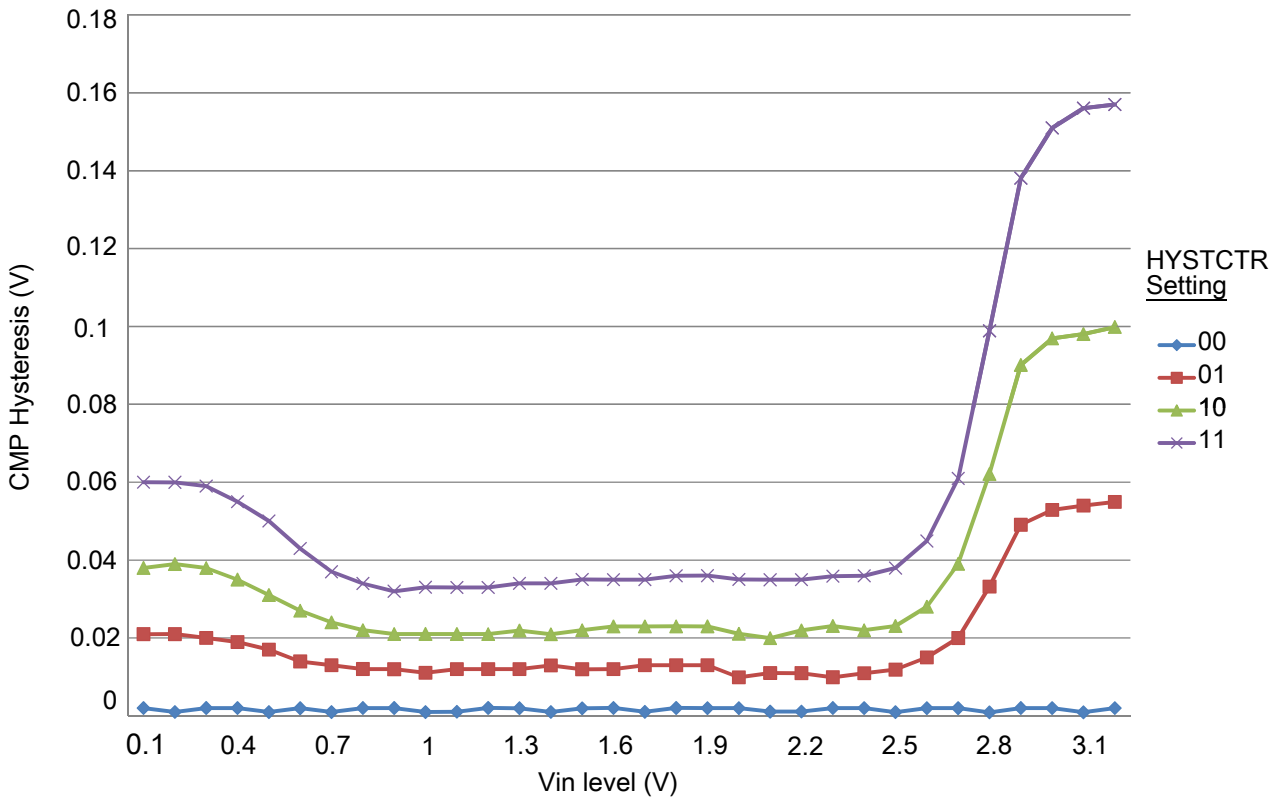


Figure 11. Typical hysteresis vs. Vin level (VDD = 3.3 V, PMODE = 1)

3.6.4 12-bit DAC electrical characteristics

3.6.4.1 12-bit DAC operating requirements

Table 33. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage		3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REFH}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

3.6.4.2 12-bit DAC operating behaviors

Table 34. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	μA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	μA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	μs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	μs	1
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	μs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	μV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h • High power (SP_{HP}) • Low power (SP_{LP})	 1.2 0.05	 1.7 0.12	 — —	V/μs	
BW	3dB bandwidth • High power (SP_{HP}) • Low power (SP_{LP})	 550 40	 — —	 — —	kHz	

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

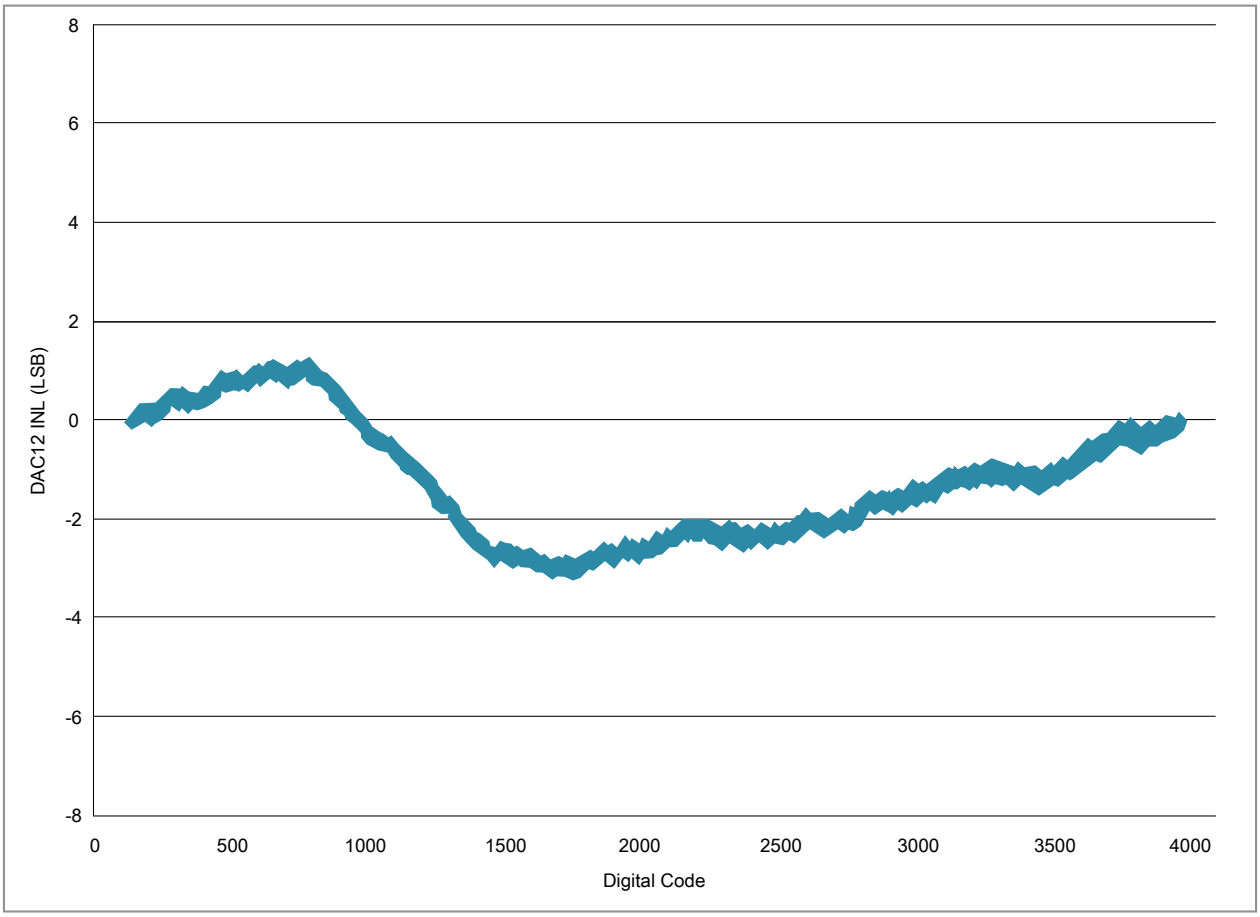


Figure 12. Typical INL error vs. digital code

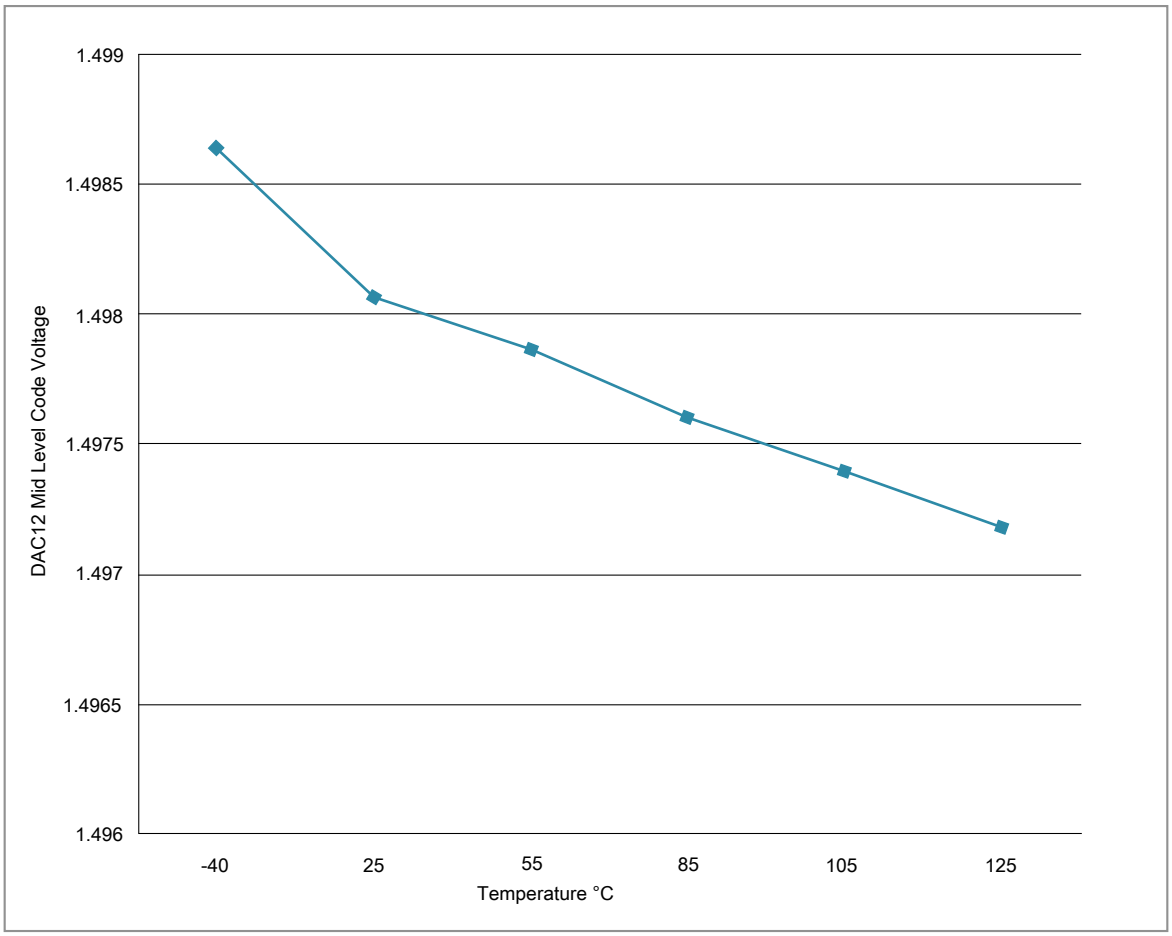


Figure 13. Offset at half scale vs. temperature

3.7 Timers

See General switching specifications.

3.8 Communication interfaces

3.8.1 USB electrical specifications

The USB electricals for the USB On-the-Go module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit usb.org .

Table 39. SPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. For SPI0 f_{periph} is the bus clock (f_{BUS}). For SPI1 f_{periph} is the system clock (f_{SYS}).
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

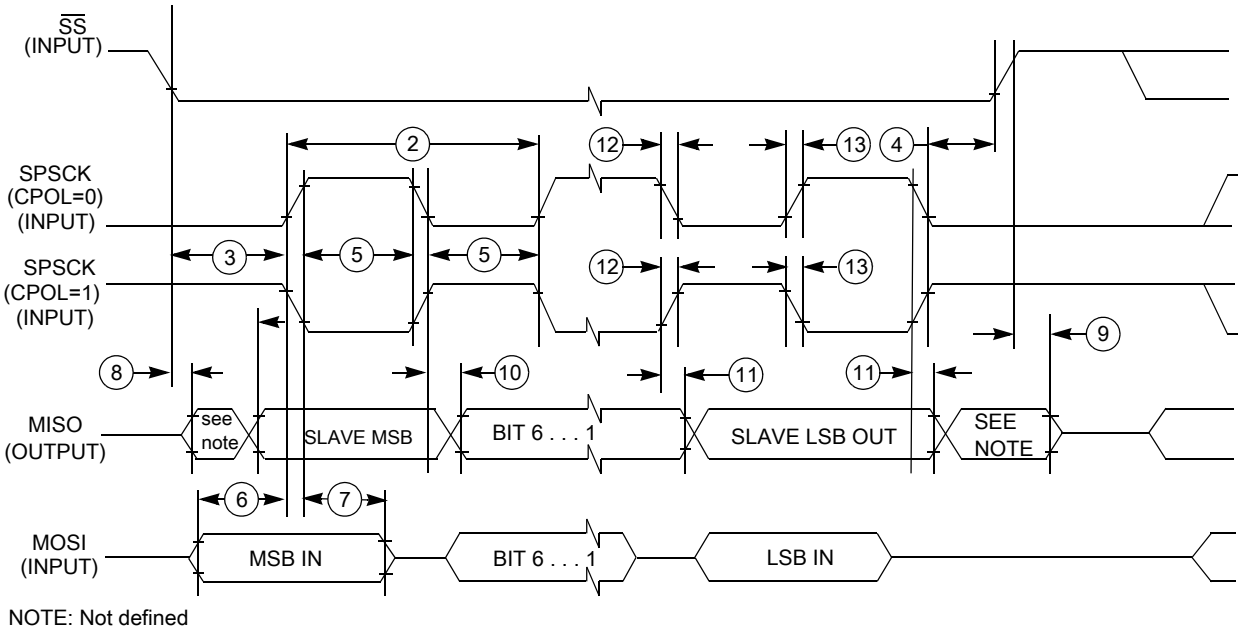


Figure 16. SPI slave mode timing (CPHA = 0)

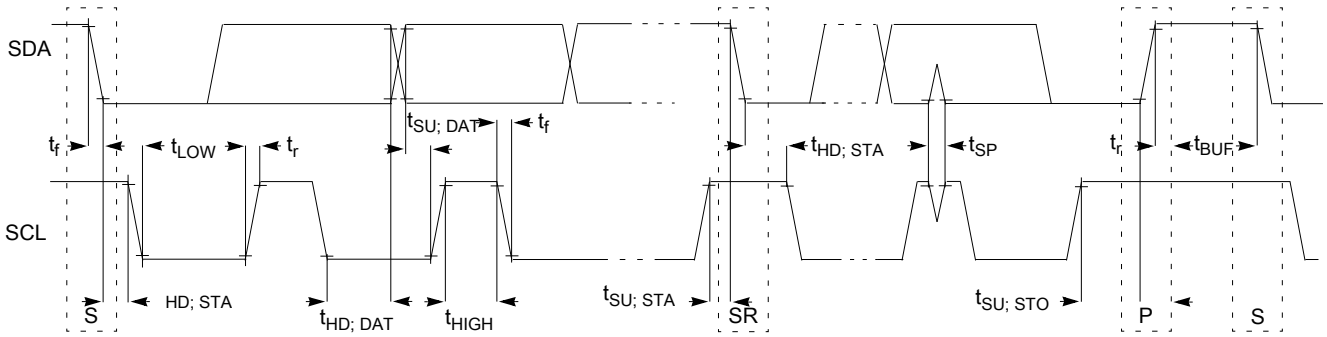


Figure 18. Timing definition for devices on the I²C bus

3.8.5 UART

See General switching specifications.

3.8.6 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

3.8.6.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 42. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns

Table continues on the next page...

Table 44. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

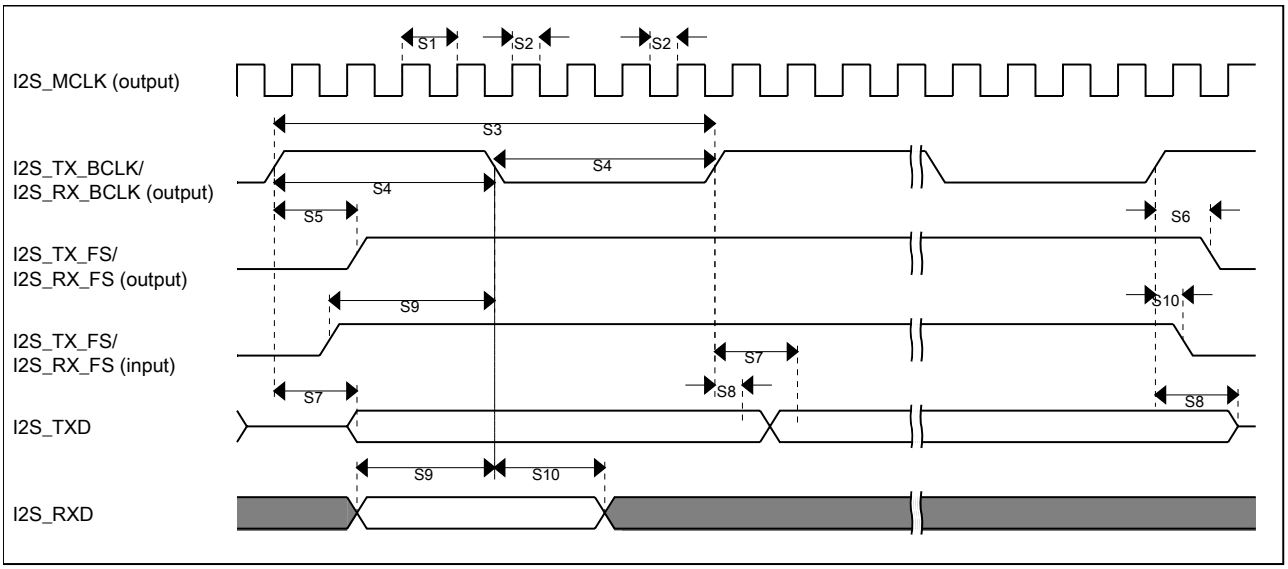


Figure 21. I2S/SAI timing — master modes

Table 45. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	87	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

8 Terminology and guidelines

8.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

Table 47. Revision History (continued)

Rev. No.	Date	Substantial Changes

		• Updated Related Resources table to include Chip Errata resource name and Package Drawing part numbers in the respective rows. Also updated Product Brief resource references.
		• Updated Table 7. Voltage and current operating behaviors.
		  • Specified correct max. value for I_{IN}.
		• Updated Table - 9 Power consumption operating behaviors.
		  • Rows added for IDD for reset pin hold low ($I_{DD\_RESET\_LOW}$) at 1.7V and 3V.
		  • Measurement unit updated for I_{DD_VLLS1} from nA to µA.
		  • Footnote 1 was moved in the beginning of the table as text.
		• Added Table - 11 EMC radiated emissions operating behaviors for 64-pin LQFP package under section 2.2.6.
		• Updated Table - 18 (IRC48M specification) and Table - 19 (IRC8M/2M specification) under section 3.3.1 - 'MCG-Lite specifications'.
		  • Removed supply voltage (V_{DD}), temperature range (T), untrimmed (f_{IRC_UT}), trim function (Δf_{IRC_C}, Δf_{IRC_F}) data from Table - 18 (IRC48M specification).
		  • Removed supply voltage (V_{DD}), temperature range (T) data from Table - 19 (IRC8M/2M specification).
		• Added Figure 6. IRC8M Frequency Drift vs Temperature curve after Table - 19 (IRC8M/2M specification).
		• Updated Table 29. VREF full-range operating behaviors.
		  • Removed A_c(Aging coefficient) row.
		  • Added $T_{chop\_osc\_stup}$ parameter.
		• Added tables: "I2C timing" and "I2C 1Mbit/s timing" under section - I^2C.
		• Added VREF specifications (V_{REFH} and V_{REFL}) to Table 26. 16-bit ADC operating conditions.
		• Removed note: “This device does not have the USB_CLKIN signal available.”

5	12 August 2015	• In Table 9. Power consumption operating behaviors:
		  • Updated Max. values of I_{DD_WAIT}, I_{DD_VLPW}, I_{DD_STOP}, I_{DD_VLPS}, I_{DD_LLS}, I_{DD_VLLS3}, I_{DD_VLLS1}, I_{DD_VLLS0}.
		  • Modified unit of I_{DD_VLLS0} from nA to µA.
		  • Removed $I_{DD\_RESET\_LOW}$ information.
		• In Table 13. Device clock specifications, added a footnote for normal run mode.
		• In Table 15. Thermal operating requirements, modified the footnote for Ambient temperature.
		• In Table 18. IRC48M specification, removed f_{IRC_T} data and added $\Delta f_{irc48m\_of\_lv}$ and $\Delta f_{irc48m\_of\_hv}$ specifications.
		• In Table 26. 16-bit ADC operating conditions, updated Max. value of f_{ADCK} and C_{rate}.

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